STANDARD MICROSYSTEMS CORPORATION

COM 9064
PRELIMINARY

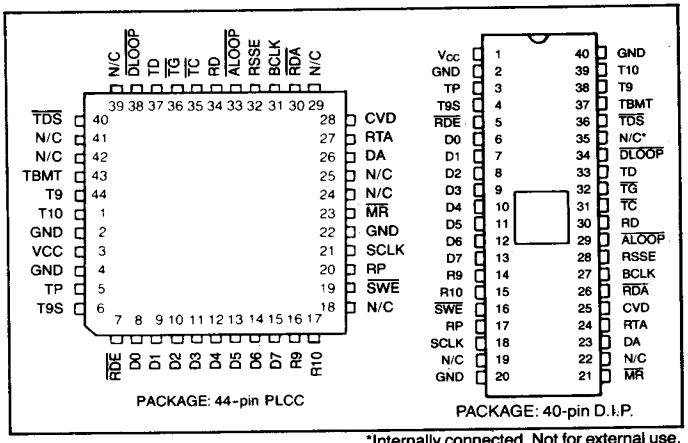
IBM® 3274/3276 Compatible COAX Receiver/Transmitter

SECTION III

FEATURES

- ☐ Conforms to the IBM® 3270 Interface Display System Standard
- ☐ Transmits and Receives Manchester II Code
- ☐ Detects and Generates Line Quiesce, Code Violation, Sync, Parity, and Ending Sequence (Mini Code Violation)
- ☐ Multi Byte or Single Byte Transfers
- ☐ Double Buffer Receiver and Transmitter
- ☐ Separate Data and Status Select
- ☐ Operates at 2.3587 MHz
- ☐ TTL Compatible Inputs and Outputs
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Single +5 Volt power supply

PIN CONFIGURATION



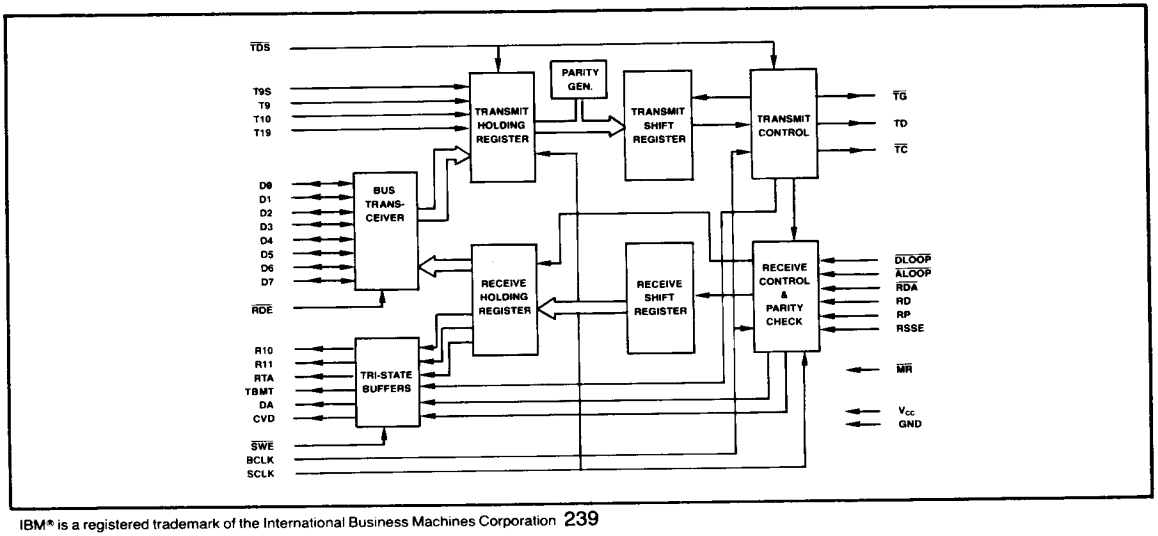
*Internally connected. Not for external use.

GENERAL DESCRIPTION

The COM 9064 is an MOS/LSI circuit which may be used to facilitate high speed data transmission. The COM 9064 is fabricated using SMC's patented COPLAMOS® technology and may be used to implement an interface between IBM® 3274/3276 compatible control units and 3278/3287/3289 compatible terminal units. The receiver and transmitter sections of the COM 9064 are separate and may be used independently of each other.

The COM 9064 generates and detects the line quiesce, code violation, parity, and mini code violation bit patterns.

The on-chip parity logic is capable of generating and checking either even or odd parity for the entire 10 bit data word. In addition, parity may be generated for the least significant 8 bits of the data word (this parity bit would replace the ninth data bit).



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ORGANIZATION

The COM 9064 is organized into 9 major sections. Communication between each section is achieved via internal data and control busses.

Transmitter Holding Register

The transmit holding register is a 12 bit latch. This latch is loaded with the transmit data and parity generation information from the system bus.

Tri-State Buffers

These buffers allow gating of the COM 9064's status word onto the system data bus.

Bus Transceiver

The bus transceiver allows bi-directional data transfer between the system data bus and the transmit and receive holding registers.

Parity Generator

This logic determines and generates the correct parity for the data in the transmitter holding register.

Transmitter Control

This logic generates signals required to enable external transmit circuitry. It also generates the Line Quiesce, Code Violation, sync bits and Mini Code Violation patterns.

Transmitter Shift Register

The transmitter shift register is an 11 bit parallel to serial shift register. It accepts data from the transmitter holding register and the parity generation logic and converts it into serial form for transmission.

Receive Control/Parity Check

This logic checks the received character for the specified parity and ensures that no Transmit Check conditions occurred. It also handles the self test mode and generates a strobe when the complete data word is received.

Receiver Shift Register

This logic is a serial to parallel shift register that converts the received information into a 10 bit data word and RTA status bit.

Receiver Holding Register

This register holds the assembled data word until it is read by the processor.

DESCRIPTION OF PIN FUNCTIONS
Processor Related Signals

PIN NO.	NAME	SYMBOL	FUNCTION
6-13	Transmit/ Receive Data Bits	D0-D7	Bidirectional: 8 bit, three state data port used to transfer data between the COM 9064 and the processor. D0 is the first bit transmitted.
4	Transmit Bit 9 Select	T9S	Input: A low level on this pin enables T9 to be transmitted as bit 9. A high level on this pin causes T9 to determine the type of parity bit generated for bits D0-D7.
38	Transmit Bit 9	T9	Input: If T9S is low, this supplies transmit bit 9. If T9S is high, then T9 low forces odd parity and T9 high forces even parity to be generated for D0-D7. In this case the parity bit generated is transmit bit 9.
39	Transmit Bit 10	T10	Input: This pin supplies transmit bit 10.
3	Transmit Parity	TP*	Input: This input controls the parity bit for transmit bits 1-10. A low level on this pin causes odd parity and a high level on this pin causes even parity to be generated for bits 1-10. The parity bit generated is transmit bit 11.
18	System Clock	SCLK	Input: This signal is used to synchronize the COM 9064. The transmitter is loaded and started on the low to high transition of SCLK if TDS is low. DA is reset on the low to high transition of SCLK if RDA is low.
36	Transmitter Data Strobe	$\overline{TDS}$	Input: This input and SCLK are used to load the transmitter holding register and start the transmit sequence. Code Violation Detect (CVD) is reset at this time.
26	Reset Data Available	$\overline{RDA}$	Input: This input and SCLK are used to reset DA.
16	Status Word Enable	$\overline{SWE}$	Input: A low level at this pin enables the status word buffer outputs (DA, CVD, TBMT, R9, R10, and RTA). A high level on $\overline{SWE}$ places the status word buffer outputs in a high impedance state.
23	Receive Data Available	DA	This three-state output signal is at a high level when an entire word has been received and transferred into the receiver buffer register. It is only set if a Transmit Check Condition did not occur.
25	Code Violation Detected	CVD	This three-state output signal is at a high level if a valid Code Violation was detected at the receiver since the last time the transmitter was loaded. It is reset when the transmitter is loaded.
37	Transmit Buffer Empty	TBMT	This three-state output signal is at a high level when the transmit holding register may be loaded with new data.
14	Receive Bit 9	R9	This three-state output signal is receiver data bit 9.
15	Receive Bit 10	R10	This three-state output signal is receiver data bit 10.
24	Recever Turn-around	RTA	This three-state output signal is set to a high level when a valid Mini Code Violation is detected. It is only set if a Transmit Check did not occur. It is reset when the transmitter is loaded.
5	Receive Data Enable	$\overline{RDE}$	Input: A low level enables the outputs of the receive data register D0-D7.
17	Receiver Parity	RP*	Input: This input determines whether the entire received word will be checked for even or odd parity. A low at this pin will cause a check for odd parity and a high at this pin will cause a check for even parity. This input has an internal pull-up resistor.

*The SYNC bit is included in parity checking.

DESCRIPTION OF PIN FUNCTIONS (cont.)

PIN NO.	NAME	SYMBOL	FUNCTION
29	Analog Loopback	$\overline{ALOOP}$	Input: A low level on this pin disables the receiver except when the transmitter is active. A high level on this pin and $\overline{DLOOP}$ will cause the receiver to be disabled while the transmitter is active. $\overline{ALOOP}$ is used to allow loop-back through the line drivers and receivers. This input has an internal pull-up resistor.
34	Digital Loopback	$\overline{DLOOP}$	Input: A low level on this pin disables the receiver except when the transmitter is active. $\overline{TG}$ is forced to a high level to disable the external coax driver. Data input to the receiver is internally wrapped from the transmitter data output. This input has an internal pull-up resistor.
21	Master Reset	$\overline{MR}$	Input: This input should be pulsed low after power-on. This signal resets DA to a low level and sets $\overline{TG}$ and TBMT to a high level. This input has an internal pull-up.
1	Supply Voltage	V_{cc}	+5 volt supply
19, 22, 35		N/C	No Connection
2, 20, 40	Ground	GND	GROUND

Device Related Signals

PIN NO.	NAME	SYMBOL	FUNCTION
27	Baud Rate Clock	BCLK	This input is a clock whose frequency is 8 times the desired transmitter and receiver baud rate (typically 18.8696 MHz for 3274/3276 operation). This input is not TTL compatible.
33	Transmit Data	TD	Output: Serial data from the transmitter. This signal is a biphase Manchester II encoded bit stream. This output is low when no data is being transmitted.
31	Transmit Clock	$\overline{TC}$	The Transmit Clock output is ½ the frequency of BCLK. It is synchronized with TD and used to provide external pre-distortion timing.
30	Receive Data	RD	Input: Accepts the serial biphase Manchester II encoded bit stream.
32	Transmit Gate	$\overline{TG}$	Output: This signal is low during the time that the transmit data is valid. TG is used to turn on the external transmit circuitry.
28	Receive Single Shot Enable	RSSE	Input: A high level on this pin enables an internal digital single shot on RD. This limits a high level on RD to 3 clock times. Also when high it will cause the receiver not to detect a valid Code Violation. A low level disables the single shot causing no reshaping of the RD input signal.

COM 9064 OPERATION

The COM 9064 consists of a receiver section that converts Manchester II phase encoded serial data to parallel data and a transmitter section that converts parallel data to Manchester II phase encoded serial data.

Receiver

Message transfers must conform to the IBM 3270 protocol in order for the COM 9064 to acknowledge them.

The received message is checked for the Code Violation sequence (start sequence) bit pattern, preceding the first data word, and Mini Code Violation (end sequence) following the last data word.

The data word consists of 10 data bits, a sync bit and a parity bit. Receiving data in multiple byte format is functional only when even parity is selected.

The data word along with the first bit of the next word or ending zero (bit 13) is shifted into a shift register. Once it is assembled it is transferred and held in the holding register until another data word is assembled. The 13th bit is inverted and presented to the bus or RTA (receiver turn-around). Therefore RTA is set high on the last word of a message and is reset when the transmitter is loaded with the response.

Once the data word is in the holding register and parity is correct the data available (DA) status signal is set high.

The Code Violation Detect signal (CVD) goes active high after a line Quiesce, Code Violation and sync bit have been detected by the receiver. It is reset when the transmitter of the COM 9064 is asserted. By examining this signal, the processor can determine whether a timeout or Transmit Check condition caused a receiver error.

The receive input is sampled at 8 times the data rate. The receiver logic is brought into bit synchronization during the Line Quiesce pattern. Once the Code Violation following the Line Quiesce is detected, the receiver is brought into bit and word synchronization. The internal receiver clock is adjusted after each transition to compensate for jitter and distortion in the received data signal.

Transmitter

The transmitter section basically consists of a 12-bit holding register, parallel to serial shift register and a parity generator. The firmware initiates a transmit sequence by strobing $\overline{TDS}$ low. The data is loaded into the holding register on the rising edge of SCLK while TDS is low. Nine bits of data (D0-D7 and T10) are transferred without change to the transmit shift register. The logic level of T9S determines whether T9 will be transmitted as parity on the preceding eight bits, or as data.

After the processor loads the transmit holding register with data, status signal TBMT is driven inactive low until the COM 9064 transfers the data from the transmit holding register

to the transmit shift register. After the transfer, TBMT is driven high. The processor should not try to load data into the COM 9064 while TBMT is low. When initiating a data transmission, the COM 9064 automatically transmits a Line Quiesce pattern and a Code Violation. The data is then shifted out of the shift register with a sync bit (1) inserted before the data word, and a parity bit appended after the data word.

If a new word is loaded into the COM 9064 before the parity bit of the previous word has been transmitted, a sync bit (1) followed by the new data bits is transmitted. If not, after the COM 9064 transmits the last data word (no more transmit sequences are started), a sync bit (0) and a Mini Code Violation is appended to the end of the message.

Output $\overline{TG}$ goes active low one-half bit cell time before the first Line Quiesce character is output. It is made inactive (high) during the transmission of the Mini Code Violation.

Diagnostic Modes

NORMAL OPERATION ($\overline{ALOOP}$ AND $\overline{DLOOP}$ HIGH)
Internal read data signal follows the RD input as long as the COM 9064's transmitter is off. The receiver will be disabled while the transmitter is active.

ANALOG LOOPBACK ($\overline{ALOOP}$ LOW AND $\overline{DLOOP}$ HIGH)
The internal read data signal follows the RD input as long as the COM 9064's transmitter is active.

DIGITAL LOOPBACK $\overline{ALOOP}$ HIGH AND $\overline{DLOOP}$ LOW)
The internal read data signal follows an internally generated and latched valid transmit signal (only when the transmitter is active.) The output $\overline{TG}$ is disabled in digital loopback mode.

DISABLE RECEIVER ($\overline{ALOOP}$ AND $\overline{DLOOP}$ LOW)
The internal read data signal is held low and output $\overline{TG}$ is disabled.

MESSAGE FORMATS

Single Byte Transmission

COAX IDLE	LINE QUIESCE	CODE VIOLATION	SYNC BIT	DATA (10 BITS)	PARITY BIT	ENDING SEQUENCE	COAX IDLE

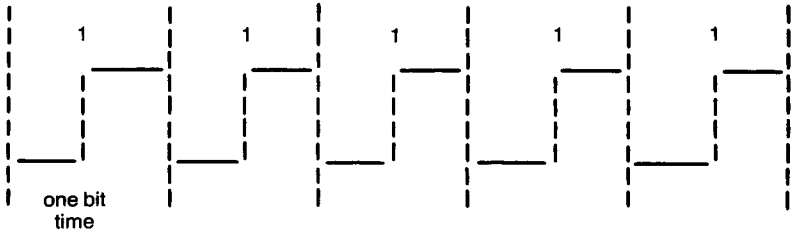
Multiple Byte Transmission

COAX IDLE	LINE QUIESCE	CODE VIOLATION	SYNC BIT	DATA 1 (10 BITS)	PARITY BIT	SYNC BIT	DATA 2 (10 BITS)

PARITY BIT	.....	SYNC BIT	DATA N (10 BITS)	PARITY BIT	ENDING SEQUENCE	COAX IDLE

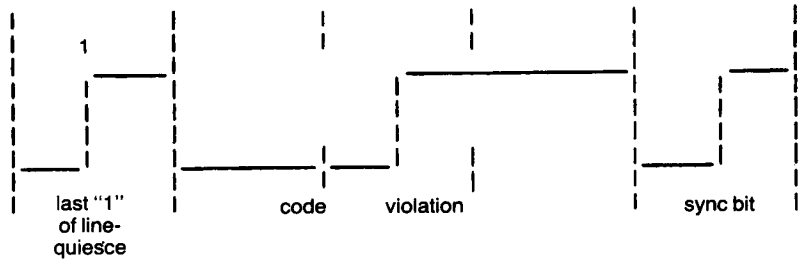
Bits on the coax appear as positive and negative going pulses. A positive pulse to negative pulse transition in the middle of the bit cell is interpreted as a logical '0'. A negative pulse to positive pulse transition in the middle of a bit cell is interpreted as a logical '1'. A predistortion pulse is generated for every pulse transition from an up to down level or a down to up level.

Line Quiesce Pattern



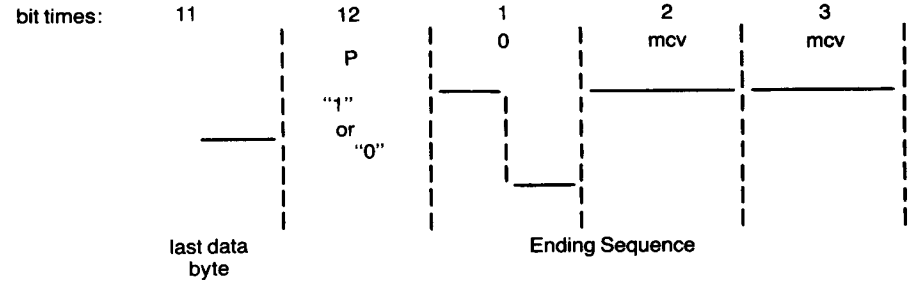
The Line Quiesce pattern consists of five contiguous logical ones. It establishes an equilibrium condition on the coax following line turnaround.

Code Violation Pattern



The Code Violation pattern is a bit sequence containing no mid-bit time level transition in two of its three bit cells. It is a unique pattern that violates the encoding rules and indicates the start of valid data.

Mini Code Violation Pattern



The Mini Code Violation (MCV) pattern is a bit sequence containing no mid-bit time level transition in either of its bit cells. It is a unique code that violates the encoding rules and indicates the end of valid transmit data.

Transmit Check

A Transmit Check is defined as follows:

1) A logical zero sync bit in the ending sequence not followed by a Mini Code Violation.
2) Loss of a level transition at the mid-bit time during other than a normal ending sequence.
3) A transmission parity error.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55° to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+8.0V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

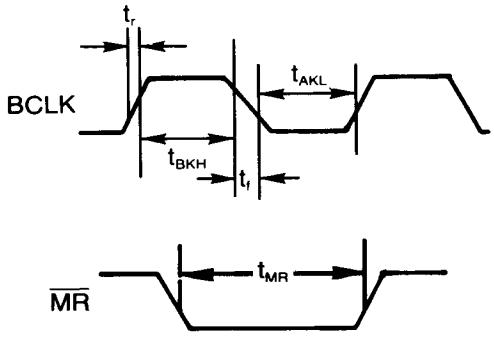
DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE					
V_{IL} Low	−0.3		.8	V	
V_{IH} High	2.0		V_{CC}	V	(Except BCLK and $\overline{MR}$)
V_{IH} High	V_{CC}−0.7		V_{CC}+.3	V	(BCLK only)
V_{IH} High	3.5		V_{CC}+.3	V	($\overline{MR}$ only)
OUTPUT VOLTAGE					
V_{OL} Low			.4		I_{OL} = 2.0 mA
V_{OH} High	2.4				I_{OH} = −.25 mA
POWER SUPPLY CURRENT					
I_{CC}		125		mA	All outputs = V_{OH}
INPUT LEAKAGE CURRENT					
All input pins			.01	mA	V_{IN} = 0 to V_{CC}
CAPACITANCE					
C_{IN}			10	pf	(Except BCLK)
C_{IN}			35	pf	(BCLK only)

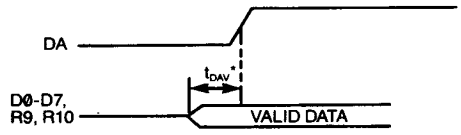
AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Clock Frequency					
B_{CLK}	7	18.8696	18.9	MHz	
S_{CLK}	DC	4.7474	5	MHz	
Clock Width					
t_{SKH} SCLK High	80			ns	
t_{SKL} SCLK Low	80			ns	
t_{BKH} BCLK High	20			ns	
t_{BKL} BCLK Low	20			ns	
t_r BCLK rise time			6	ns	
t_F BCLK fall time			6	ns	
t_{RDD} $\overline{RDE}$ to Data Valid Delay			50	ns	
t_{SDD} $\overline{SWE}$ to Data Valid Delay			50	ns	
t_{DF} Data Read to Bus Float			50	ns	
t_{DS} Data Setup Time	100			ns	
t_{DH} Data Hold Time	10			ns	
t_{DAV} DA to receive data valid delay	−100		100	ns	
t_{TC} TC clock period		106		ns	
$t_{\overline{TG}LD}$ TC to TG low delay	−53		30	ns	
$t_{\overline{TG}HD}$ TC to TG high delay			30	ns	
t_{TDS} Transmit data to TC setup time	10			ns	
t_{TDH} Transmit data to TC hold time	20			ns	
t_D TBMT active to de-active		200		ns	
t_{TDDC} TBMT cycle			3.2	µs	
t_{DD} $\overline{TBMT}$ de-activated	1		2	µs	
t_{DSS} $\overline{TDS}$ set up	100		200	ns	
t_{DSH} $\overline{TDS}$ hold	20		100	ns	
t_{MR} $\overline{MR}$ pulse width	300			ns	

MISC. TIMING

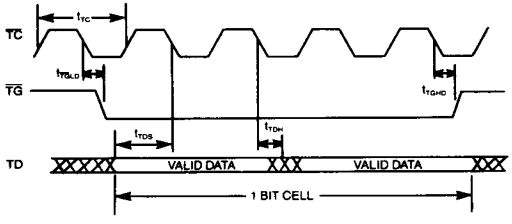


RECEIVE DATA TIMING

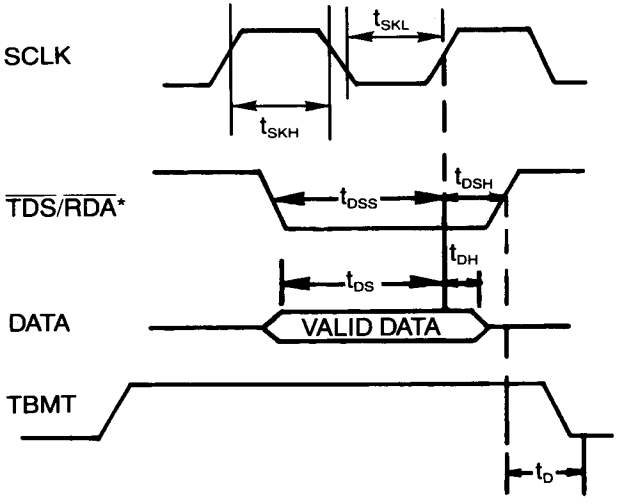


*DA may occur from 100 ns before to 100 ns after data is valid.

TRANSMITTER TIMING

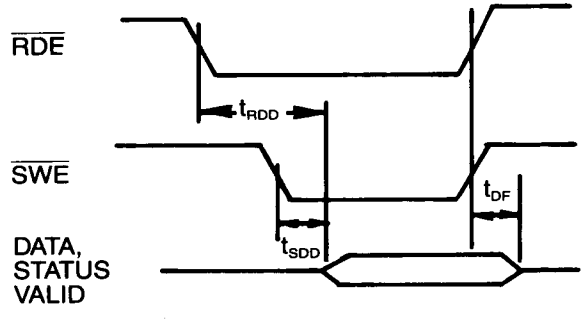


BUS INPUT TIMING

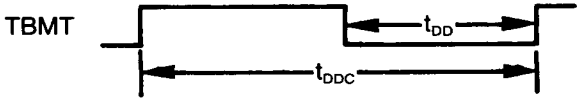


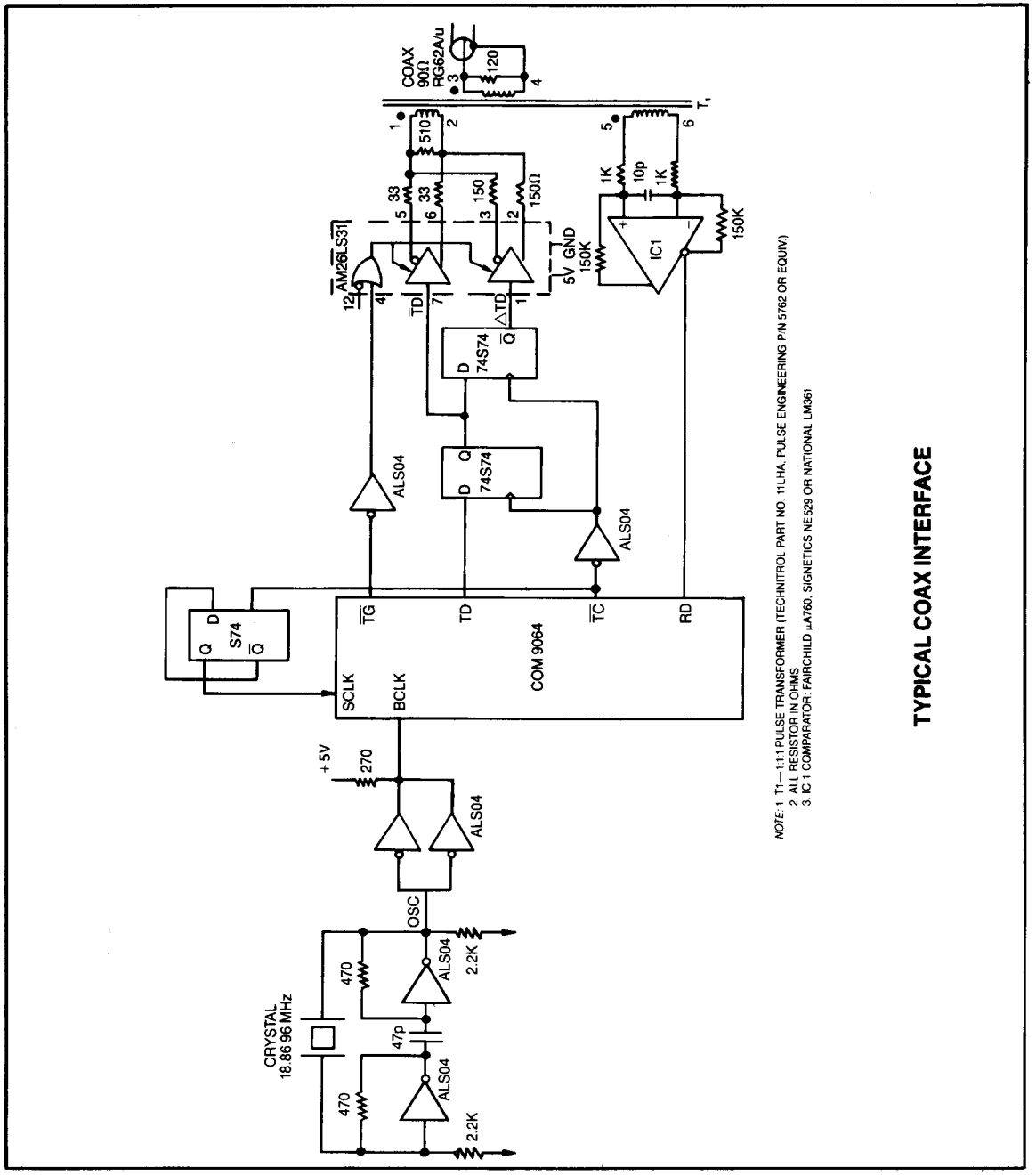
*Only one rising edge of SCLK within this pulse width.

BUS OUTPUT TIMING



TBMT CYCLE





NOTE: 1. T1—1:1:1 PULSE TRANSFORMER (TECHNITROL PART NO. 11LHA, PULSE ENGINEERING P/N 5762 OR EQUIV.)
2. ALL RESISTOR IN OHMS
3. IC 1 COMPARATOR: FAIRCHILD μA760, SIGNETICS NE529 OR NATIONAL LM361

TYPICAL COAX INTERFACE