Am27S184/185/PS185

8,192-Bit (2048 x 4) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- Ultra-fast access time "A" version (35 ns Max.) — Fast access time Standard version (50 ns Max.) — allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

GENERAL DESCRIPTION

The Am27S184/185 (2048-words by 4-bits) is a Schottky TTL Programable Read-Only Memory (PROM).

This device is available in both open-collector (Am27S184) and three-state (Am27S185) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy-word depth expansion is facilitated by an active LOW ($\overline{G}$) output enable.

This device is also offered in a low-power, three-state version, the Am27LS185, as well as a power-switched three-state version.
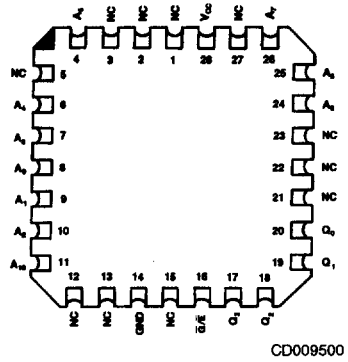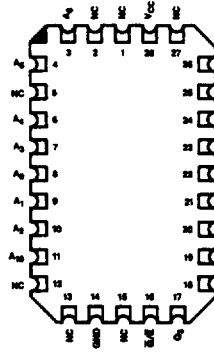
BLOCK DIAGRAM

BD006320
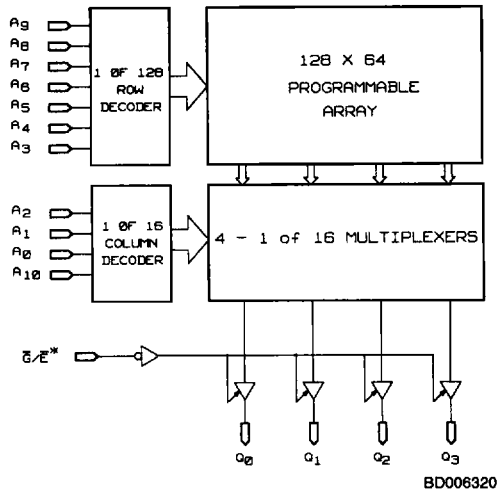
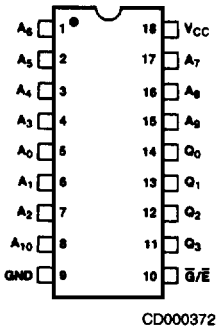### PRODUCT SELECTOR GUIDE

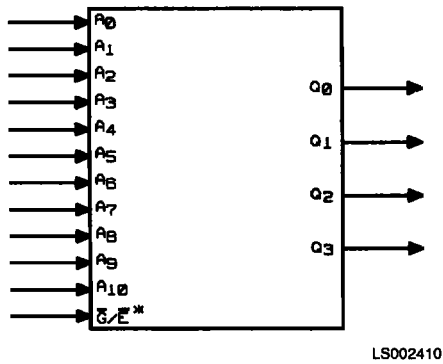| Open-Collector Part Number	27S184A		27S184					
Three-State Part Number	27S185A		27S185		27LS185		27PS185	
Address Access Time	35 ns	45 ns	50 ns	55 ns	60 ns	65 ns	50 ns	55 ns
Operating Range	C	M	C	M	C	M	C	M

Note: Pin 1 is marked for orientation.

CD000372

CD000382

CD009500
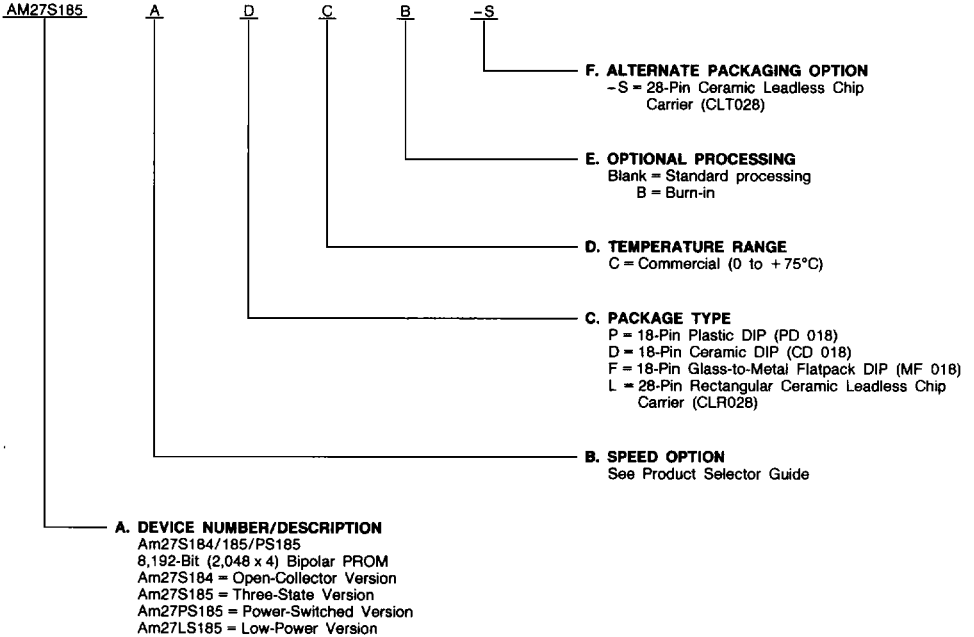
2

LOGIC SYMBOL

LS002410

*E nomenclature applies only to Am27PS power-switched versions.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option

AM27S185   A   D   C   B   –S

F. ALTERNATE PACKAGING OPTION
–S = 28-Pin Ceramic Leadless Chip Carrier (CLT028)

E. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

C. PACKAGE TYPE
P = 18-Pin Plastic DIP (PD 018)
D = 18-Pin Ceramic DIP (CD 018)
F = 18-Pin Glass-to-Metal Flatpack DIP (MF 018)
L = 28-Pin Rectangular Ceramic Leadless Chip Carrier (CLR028)

B. SPEED OPTION
See Product Selector Guide

A. DEVICE NUMBER/DESCRIPTION
Am27S184/185/PS185
8,192-Bit (2,048 x 4) Bipolar PROM
Am27S184 = Open-Collector Version
Am27S185 = Three-State Version
Am27PS185 = Power-Switched Version
Am27LS185 = Low-Power Version

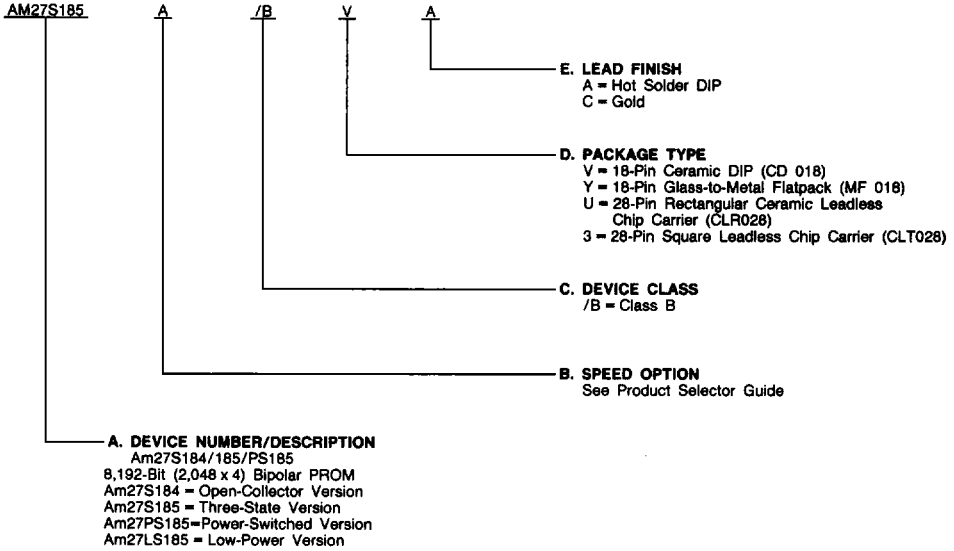| Valid Combinations	
AM27S184	PC, PCB, DC DCB, FC, FCB, LC, LCB, LC-S, LCB-S
AM27S184A	
AM27S185	
AM27S185A	
AM27PS185	PC, PCB, DC, DCB, LC, LCB, LC-S, LCB-S
AM27LS185	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
                     B. Speed Option (if applicable)
                     C. Device Class
                     D. Package Type
                     E. Lead Finish

```
AM27S185        A        /B        V        A
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E. LEAD FINISH
A = Hot Solder DIP
C = Gold

D. PACKAGE TYPE
V = 18-Pin Ceramic DIP (CD 018)
Y = 18-Pin Glass-to-Metal Flatpack (MF 018)
U = 28-Pin Rectangular Ceramic Leadless
      Chip Carrier (CLR028)
3 = 28-Pin Square Leadless Chip Carrier (CLT028)

C. DEVICE CLASS
/B = Class B

B. SPEED OPTION
See Product Selector Guide

A. DEVICE NUMBER/DESCRIPTION
Am27S184/185/PS185
8,192-Bit (2,048 x 4) Bipolar PROM
Am27S184 = Open-Collector Version
Am27S185 = Three-State Version
Am27PS185=Power-Switched Version
Am27LS185 = Low-Power Version

Valid Combinations	
AM27S184	
AM27S184A	
AM27S185	/BVA, /BYC,
AM27S185A	/BUC, /B3C,
AM27PS185	
AM27LS185	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{10}$ Address Inputs

The 11-bit field presented at the address inputs selects one of 2,048 memory locations to be read from.

$Q_0 - Q_3$ Data Output Port

The outputs whose state represents the data read from the selected memory locations.

$\overline{G}/E^*$ Output Enable

Provides direct control of the Q-output buffers. Outputs disabled forces all open-collector outputs to an OFF state and all three-state outputs to a floating or high-impedance state.

Enable = $\overline{G}/E^*$
Disable = G/E*

V_{CC} Device Power Supply Pin

The most positive of the logic power supply pins.

GND   Device Power Supply Pin

The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

Power Switching

The Am27PS185 is a power switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS185 is selected by a low level on $\overline{CS}$, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1 μf ceramic capacitor be connected from pin 18 to pin 9 at each device. (See Figure 1.)

2. Address access time (TAVQV1) can be optimized if a chip enable set-up time (TEVAV) of greater than 25 ns is observed. Negative set-up times on chip enable (TEVAV=tl0) should be avoided. (For typical and worse case characteristics see Figures 2A and 2B.)

*$\overline{E}$ Nomenclature applies only to Am27PS power-switched versions.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature with
    Power Applied .... −55 to +125°C
Supply Voltage .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
    (Except During Programming) .... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
    During Programming .... 21 V
Output Current into Outputs During
    Programming (Max. Duration of 1 sec) .... 250 mA
DC Input Voltage .... −0.5 V to +5.5 V
DC Input Current .... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
    Temperature .... 0 to +75°C
    Supply Voltage .... +4.75 V to +5.25 V
Military (M) Devices
    Temperature .... −55 to +125°C
    Supply Voltage .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

2

DC CHARACTERISTICS over operating range unless otherwise specified*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH} (Note 1)	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}				40	μA
I_{SC} (Note 1)	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0.0 V (Note 3)	STD, LS devices	−20		−90	mA
			PS devices	−15		−90	
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.	STD, PS devices			150	mA
			LS devices			125	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = Max. V_G = 2.4 V	V_O = V_{CC}			40	μA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 4)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 4)			8.0		

Notes: 1. This applies to three-state devices only.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

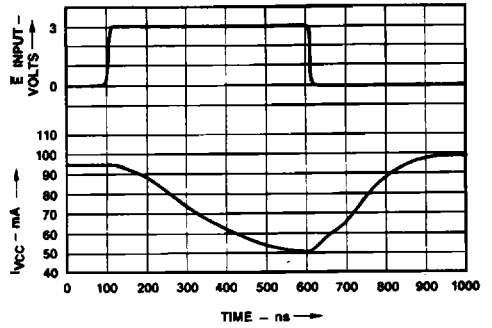*See the last page of this spec for Group A Subgroup Testing information.

TYPICAL DC and AC CHARACTERISTICS

**Typical I$_{VCC}$ Current Surge without 0.1 μF
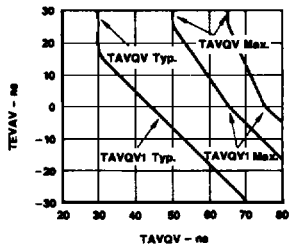(I$_{VCC}$ is Current Supplied by V$_{CC}$ Power Supply)**
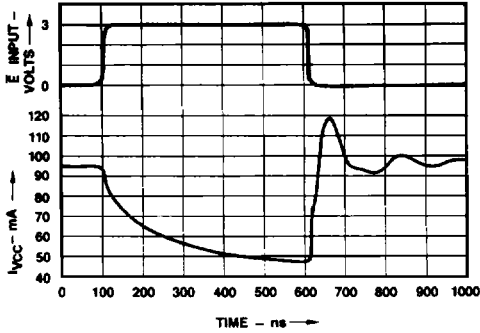
**Typical I$_{VCC}$ Current Surge without 0.1 μF
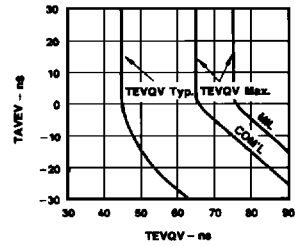(I$_{VCC}$ is Current Supplied by V$_{CC}$ Power Supply)**

OP001221

OP001231

Figure 1. I$_{CC}$ Current

OP001191

OP001201

Figure 2A. TAVQV vs TEVAV (Am27PS191/291)

Figure 2B. TEVQV vs TAVEV

SWITCHING TEST CIRCUIT
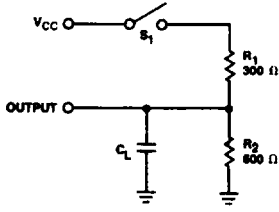
TC000171

Notes: 1. TAVQV is tested with switch S_1 closed and $C_L = 50$ pF.
2. For open-collector outputs, TGVQZ and TGVQV are tested with S_1 closed to the 1.5 V output level. $C_L = 50$ pF.
3. For three-state outputs, TGVQZ is tested with $C_L = 50$ pF to the 1.5 V level: S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. TGVQV is tested with $C_L = 5$ pF. HIGH to high-impedance tests are made to an output steady state HIGH voltage -0.5 V with S_1 open; LOW to high-impedance tests are made to the steady state LOW $+0.5$ V level with S_1 closed.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

No.	Parameter Symbol	Parameter Description	Version	27S Version				27PS Version				Units
				COM'L		MIL		COM'L		MIL		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	A		35		45					ns
			STD		50		55		50		55	
			LS		60		65					
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	A		25		30					ns
			STD		25		30		25		30	
			LS		25		30					
3	TGVQV	Delay from Output Enable Valid to Output Valid	A		25		30					ns
			STD		25		30		60		65	
			LS		25		30					
4	TAVQV1	Power Switched Address Valid to Output Valid Access Time (Am27PS Versions only)	A									ns
			STD						60		65	

See also Switching Test Circuit.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage $+0.5$ V output levels.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS
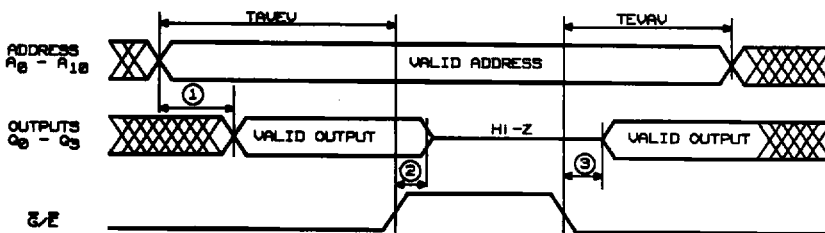
WF021620

GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	TAVQV	9, 10, 11
2	TGVQZ	9, 10, 11
3	TGVQV	9, 10, 11
4	TAVQV1	9, 10, 11
5	Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.