Shenzhen LIZE Electronic Technology Co., Ltd

SPECIFICATION

L2269

Current Mode PWM Controller

VERSION 1.0

Description

L2269 is highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyblack converter applications in sub 80W range.

PWM switching frequency at normal operation is externally programmable to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss.Lower standby power and higher conversion efficiency in thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with L2269.A large value resistor could thus be used in the startup circuit to minimize the standby power.

L2269 offers complete protection coverage with automatic self- recovery feature including Cycle-by-Cycle current limiting (OCP), over temperature protection(OTP),VDD over voltage clamp and under voltage lockout (UV LO).The Gate output is clamped to maximum 18V to protect the power MOSFET.

Features

● Proprietary frequency shuffling technology for improved EMI performance.
● External programmable PWM switching frequency.

● Leading edge Blanking on current sense input.
● Internal synchronized slope compensation .
● Extended burst mode control for improved efficiency and minimum standby power design
● Low VDD startup current and low operating current.
● Gate output maximum voltage clamp 18V.
● Cycle-by-Cycle Current Limiting, Built-in Adaptive Current Peak Regulation
● Power on Soft-start, Programmable CV and CC Regulation
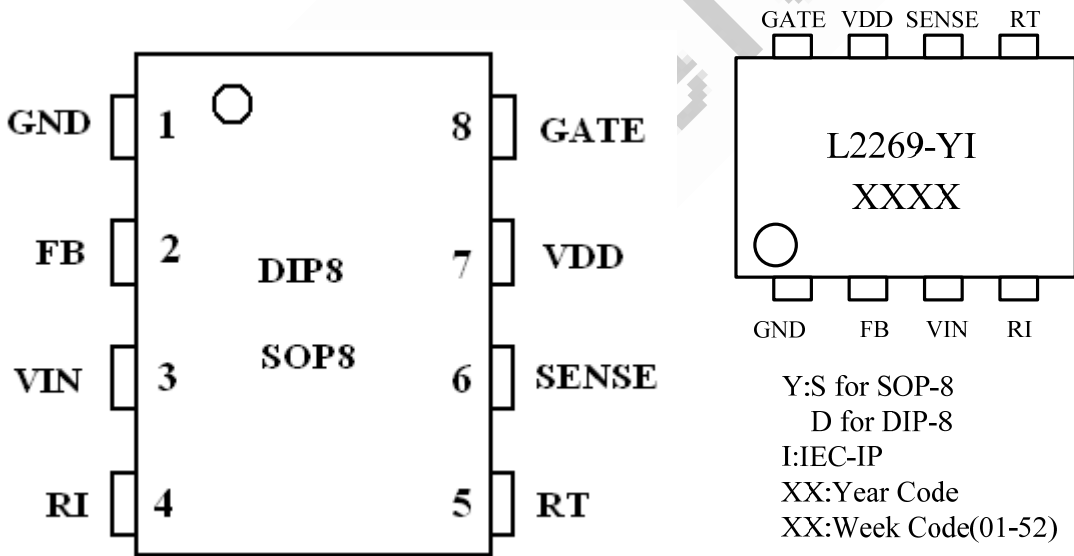● VDD Under Voltage Lockout with Hysteresis(UVLO),OVP,OCP,OLP, Clamp VDD,

Applications

● Digital Cameras Charger
● Power adaptor
● Set_top box power supplies
● Open_frame SMPS
● Battery charger

Application Circuit
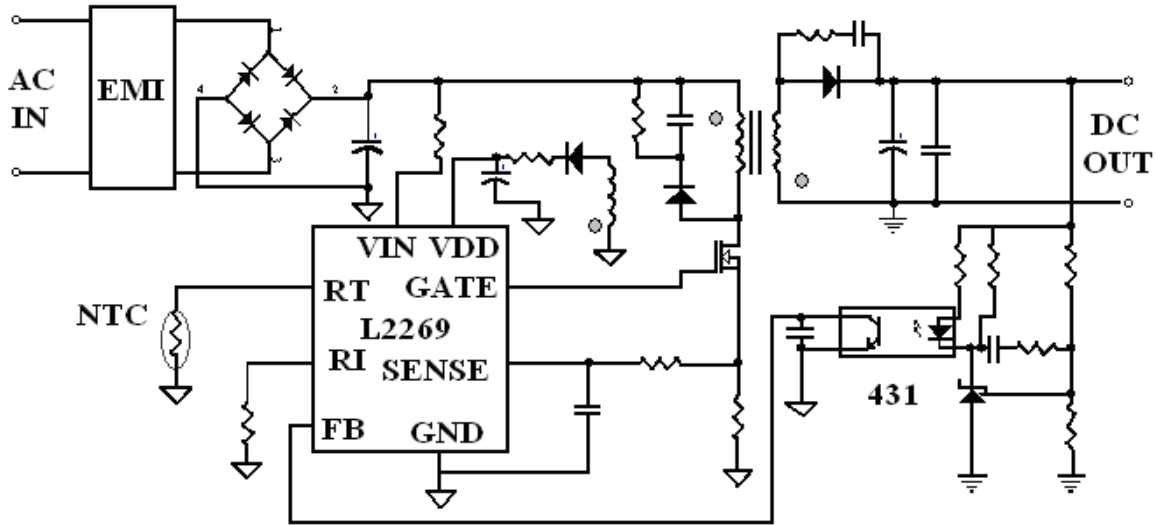
Pin Assignment & Marking Information

Y:S for SOP-8
  D for DIP-8
I:IEC-IP
XX:Year Code
XX:Week Code(01-52)

Ordering Information

Part number	Package
L2269-SI	SOP-8
L2269-DI	DIP-8

Pin Description

Pin Number	Symbol	Type	Description
1	Gnd	P	Ground.
2	FB	I	Feedback input pin.The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
3	VIN	I	Connected through a large value resistor to rectified line input for startup IC supply GND and line voltage sensing.
4	RI	I	Internal oscillator frequency setting pin.
5	RT	I	Temperature sensing intput pin,connected through a NTC resistor to GND.
6	SENSE	I	Current sense intput pin. Connected to MOSFET current resistor ode.
7	VDD	P	Chip DC power supply pin
8	GATE	O	Totem-pole gate diver output for the power MOSFET

Recommended Out Power

Product	Input:230VAC±15%	Input:85-264VAC
	Adapter	Adapter
L2269	100W	90W

Block Diagram
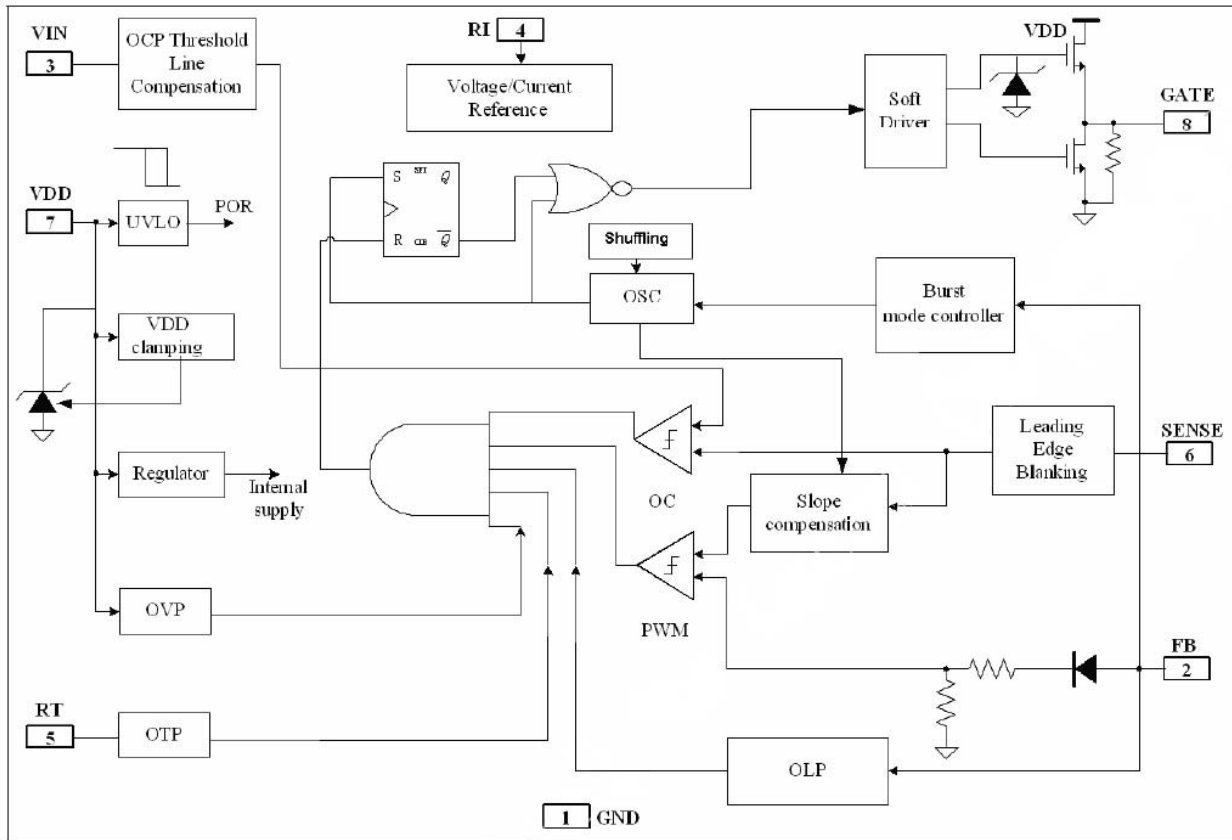
Absolute Maximum Rating

Parameter	Value	Unit
VDD/VIN supply voltage	30	V
VDD zener clamp voltage	VDD clamp +0.1	KΩ
VDD clamp continuous current	10	mA
VFB input voltage	-0.3 to 7	V
VSENSE input voltage to SENSE pin	-0.3 to 7	V
VRT input voltage to RT pin	-0.3 to 7	V
VRI input voltage to RI pin	-0.3 to 7	V
Operating ambient temperature	-20 to 85	℃
Min/Max operating junction temperature	-55 to 150	℃

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
VDD	Supply Voltage Vcc	11	29	V
RI	RI Resistor Value	24	31	Kohm
T$_A$	Operating Ambient Temperature	−20	85	℃

ESD Information

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HBM	Human BodyModel on All Pins Except VIN and VDD	MIL-STD		3		KV
MM	Machine model on All pins	JEDEC-STD		250		V

Electrical Characteristics

(T$_A$ = 25 ℃, if not otherwise noted)

Symbol	Parameter	Conditions	Value Min.	Value Typ.	Value Max.	Unit
Supply Voltage (VDD Pin)						
Idd_startup	VDD start up current	VDD=12.5V RI=24K		6	10	uA
Idd	VDD current	VDD=18V RI=24KΩ, FB=3.6V		2.3		mA
UVLO (enter)	VDD under voltage lockout enter		9.5	10.5	11.5	V
UVLO(exit)	VDD under voltage lockout exit		15.5	16.5	17.5	V
OVP(enter)	VDD over voltage protection enter		24	26.5	27.5	V
OVP(exit)	VDD over voltage protection exit		22	24	25.5	V
VDD_clamp	VDD zener clamp voltage	Idd=10mA	29	30	31	V
TD_OVP	VDD OVP debounce time			80		uS
Voltage Feedback (FB Pin)						
AVCS	PWM input gain	ΔVFB/ΔVSENSE		2.8		V/V
VFB_open	VFB open loop voltage			5.8		V
VFB_burst	Burst mode voltage			1.7		V
IFB_short	FB pin short current	Short FB pin to GND and measure current		1.2		mA
VTH_PL	Power limiting FB threshold voltage	Iout=−10mA		4.5		V

TD_PL	Power limiting debounce time			64		mS

Current Sense(CS Pin)

T_blanking	Leading edge blanking time			250		nS
ZSENSE_IN	Input impedance			30		KΩ
VTH_OC_0	Current limiting threshold voltage at no compensation	I(VIN)= 0 uA		0.9		V
VTH_OC_1	Current limiting threshold voltage at compensation	I(VIN)= 150 uA		0.81		V

Oscillator(RT Pin)

Fosc	Normal oscillation frequency	RI=24KΩ	60	65	70	Khz
Δf_temp	Frequency temperature stability	TA -20℃ to 100℃ VDD=16V,RI=24KΩ		2		%
Δf_VDD	Frequency voltage stability	VDD=12V to 25V RI=24KΩ		2		%
RI_range	Operating RI range		12	24	60	KΩ
VRI_open	RI open load voltage			2		V
Fosc_BM	Burst mode base frequency			25		Khz
DC_MAX	Maximum duty cycle	VDD=18V, FB=3V SENSE=0V		80		%
Δf_OSC	Frequency modulation range /Base frequency		-5		+5	%

Gate Drive Output(Out Pin)

VOL	Output low level	VDD=18V,IO=-20mA			0.3	V
VOH	Output high level	VDD=18V,IO=20mA	11			V
V_Clamp	output clamp voltage level			18		V
T_r	Output rising time	VDD=18V,CL=1nF		110		nS
T_f	Output falling time	VDD=18V,CL=1nF		40		nS

Over Temperature Protection

I_RT	Output current of RT pin			70		uA
V_OTP	OTP threshold voltage			0.65		V
V_OTP_off	OTP recovery threshold voltage			0.8		V
T_OTP	OTP de-bounce time			100		uS

Typical Performance Characteristics
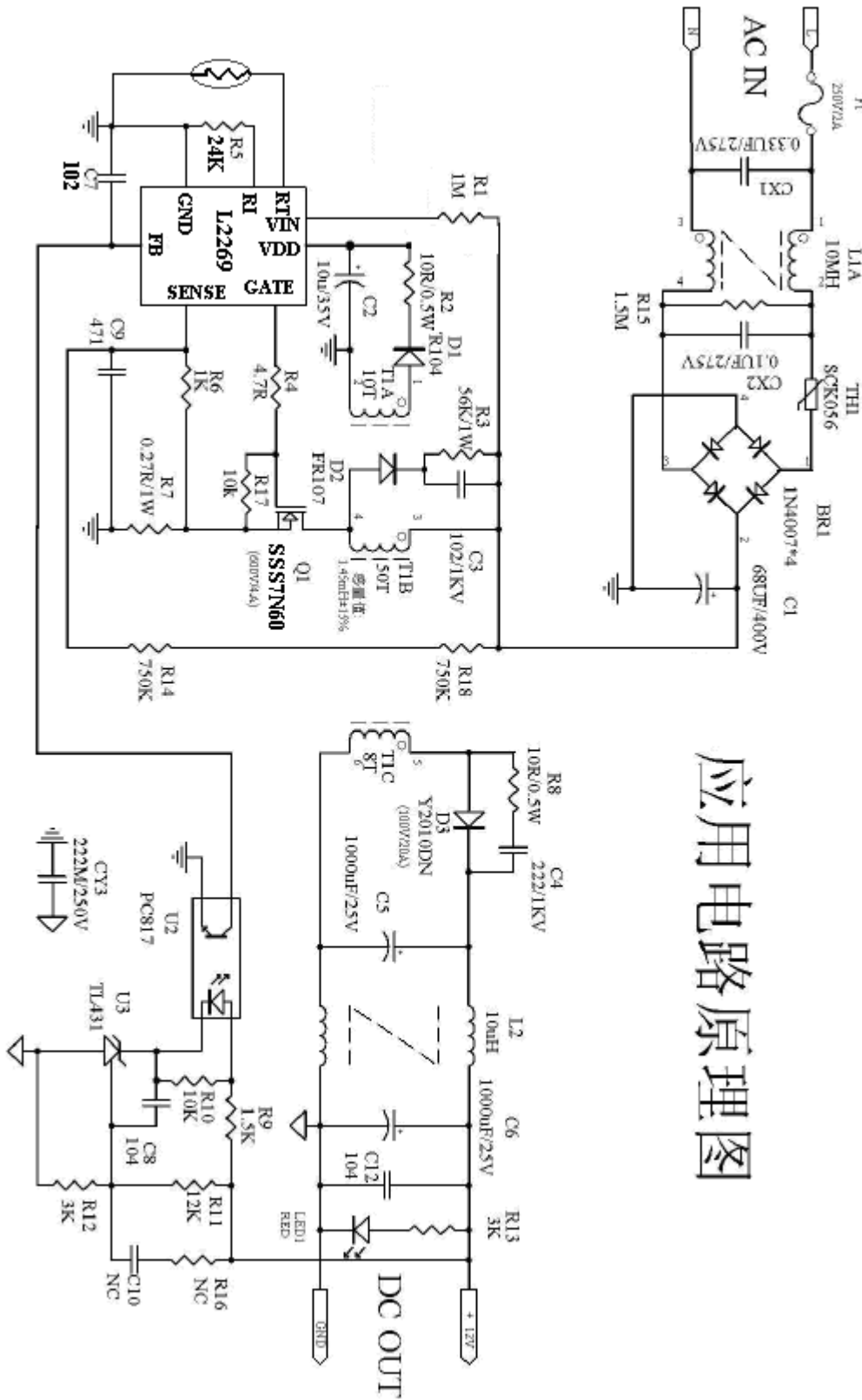
应用电路原理图

Application Information

The L2269 is a highly integrated PWM controller IC optimized for offline flyback converter applications. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of L2269 is designed to be very low so that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current

The Operating current of L2269 is low at 2.3mA. Good efficiency is achieved with L2269 low operating current together with extended burst mode control schemes.

Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in L2269. The oscillation frequency is modulated with a internally generated random source so that the tone energy is evenly spread out.The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

Burst Mode Operation

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET ransistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of swit-
-ching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy.

L2269 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device

enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off stateto minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$Fosc = 1560/RI(K\Omega) \quad (Khz)$$

Current Sensing and Leading EdgeBlanking

Cycle-by-Cycle current limiting is offered in L2269 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Over Temperature Protection

A NTC resistor in series with a regular resistor should connect between RT and GND for emperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current IRT flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the

MOSFET when the sensed input voltage is lower than VTH_OTP.

Gate Drive

L2269 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

Protection Controls

Good system reliability is achieved with L2269's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on chip VDD over voltage protection (OVP, optional) and under voltage lockout (UVLO).

The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on L2269.At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET.

Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected.L2269 resumes the operation when temperature drops below the hysteresis value.VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on startup sequence thereafter
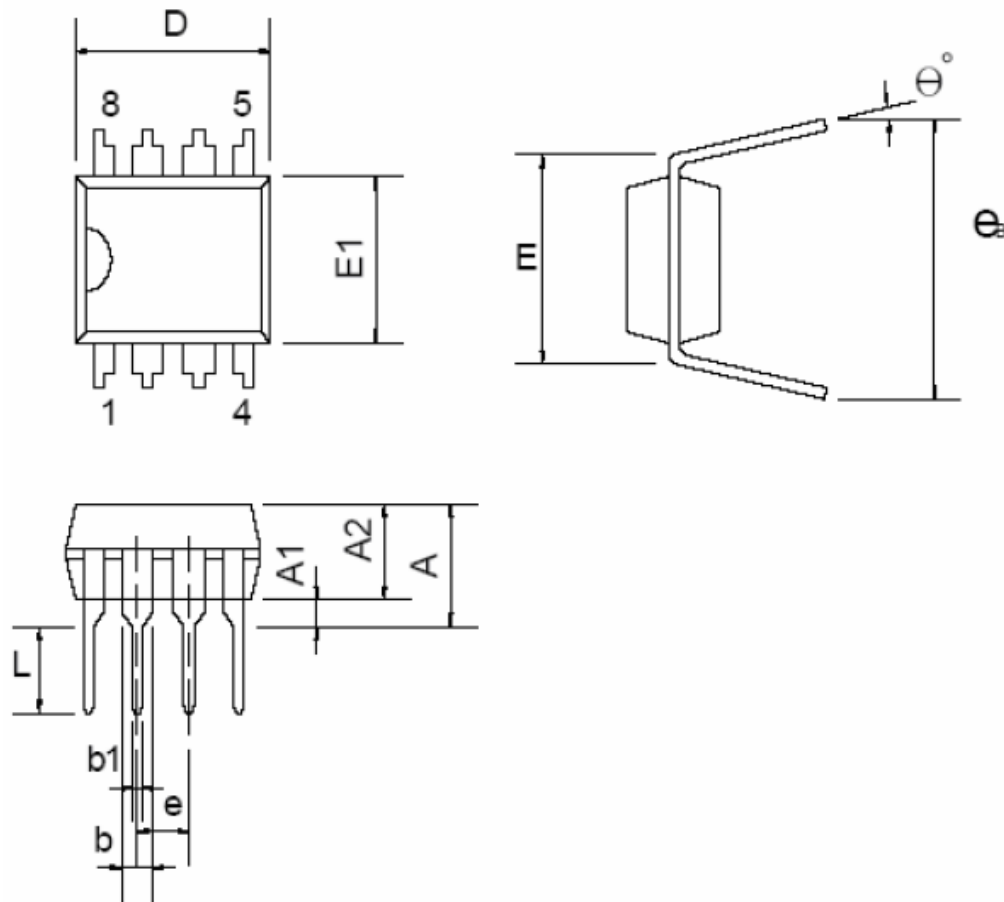
Package Information：

SOP-8
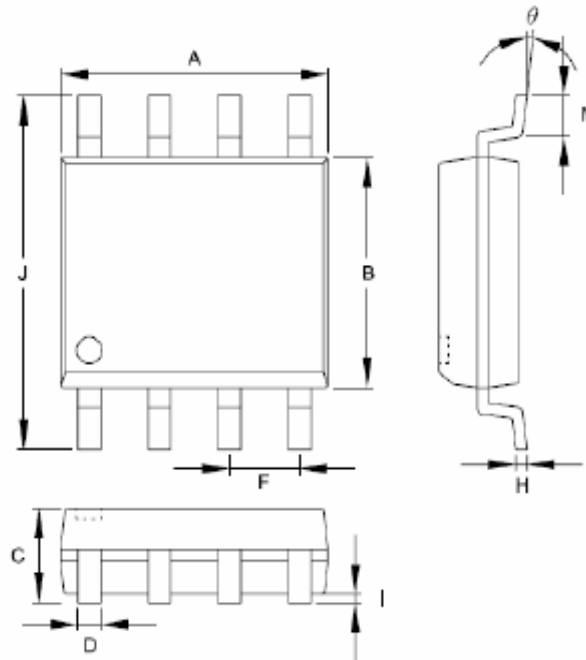
Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP-8

mensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°