

Compact, Low Power Consumption, Triple SPDT (Triple 2:1 Multiplexers)

DESCRIPTION

The DG9454 is a triple SPDT (triple 2:1 multiplexers) with enhanced performance on low power consumption, while guarantees 1.8 V logic compatible over the full operation voltage range.

The DG9454 is designed to operate from a + 2.7 V to + 13.2 V supply at V_{+} , and + 2.5 V to + 5.5 V at V_{L} .

The DG9454 is a high precision switch of low parasitic capacitance, low leakage, low charge injection, and fast switching speed.

Processed with advanced CMOS technology, the DG9454 conducts equally well in both directions, offers rail to rail analog signal handling and can be used both as multiplexers as well as de-multiplexers.

The advantages of DG9454 at size, weight, power consumption, and low voltage control capability make it ideal for portable consumer applications such as 3D glasses (3D goggles). Its precise switching, wide dynamic range, and low parasitic characters make it a high performance switch for healthcare, data acquisition, and instrument products.

The DG9454 operating temperature is specified from - 40 °C to + 85 °C and are available and the ultra compact 1.8 mm x 2.6 mm miniQFN16 packages.

As a comitted partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. DG9454 is offered in a miniQFN package. The miniQFN package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL ratings.

FEATURES

- Operates with $V_{+} = 2.7\text{ V to }13.2\text{ V}$;
 $V_{L} = 2.5\text{ V to }5.5\text{ V}$
- Guaranteed 1.8 V logic control at full V_{+} range
- Low power consumption, < 1 μA
- High bandwidth: 540 MHz
- Low charge injection over the full signal range (less than 0.9 pQ)
- Low switch capacitance ($C_{S(\text{off})}$ 2 pF typ.)
- Good isolation and crosstalk performance (typ. - 65 dB at 10 MHz)
- Compact and light miniQFN16 package (1.8 mm x 2.6 mm)
- **Compliant to RoHS Directive 2002/95/EC**
- **Halogen-free according to IEC 61249-2-21 definition**

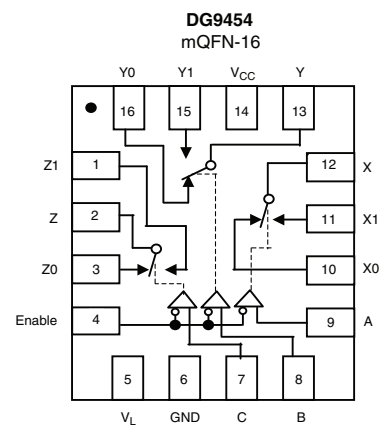


RoHS
COMPLIANT
HALOGEN
FREE

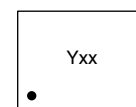
APPLICATIONS

- 3D glasses (goggles)
- Touch panels
- Data acquisition
- Medical and healthcare devices
- Control and automation equipments
- Test instruments

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View



Pin 1

Device Marking: 5xx for DG9454
(miniQFN16)

xx = Date/Lot Traceability Code



| TRUTH TABLE | | | | |
|--------------|---------------|---|---|---------------------------|
| Enable Input | Select Inputs | | | On Switches |
| | C | B | A | DG9454 |
| H | X | X | X | All Switches Open |
| L | L | L | L | X to X0, Y to Y0, Z to Z0 |
| L | L | L | H | X to X1, Y to Y0, Z to Z0 |
| L | L | H | L | X to X0, Y to Y1, Z to Z0 |
| L | L | H | H | X to X1, Y to Y1, Z to Z0 |
| L | H | L | L | X to X0, Y to Y0, Z to Z1 |
| L | H | L | H | X to X1, Y to Y0, Z to Z1 |
| L | H | H | L | X to X0, Y to Y1, Z to Z1 |
| L | H | H | H | X to X1, Y to Y1, Z to Z1 |

| ORDERING INFORMATION | | |
|--------------------------------|----------------|----------------|
| Temp. Range | Package | Part Number |
| DG9454 | | |
| - 40 °C to 125 °C ^a | 16-Pin miniQFN | DG9454EN-T1-E4 |

Notes:

a. - 40 °C to 85 °C datasheet limits apply.

| ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted) | | | |
|--|--------------------------------|---|------|
| Parameter | | Limit | Unit |
| Digital Inputs ^a , V _S , V _D , V _L | | GND - 0.3 to (V+) + 0.3 or 30 mA, whichever occurs first | V |
| V+ to GND | | 14 | |
| Continuous Current (Any terminal) | | 30 | mA |
| Peak Current, S or D (Pulsed 1 ms, 10 % duty cycle) | | 100 | |
| Storage Temperature | | - 65 to 150 | °C |
| Power Dissipation ^b | 16-Pin miniQFN ^{c, d} | 525 | mW |
| Thermal Resistance ^b | 16-Pin miniQFN ^d | 152 | °C/W |
| Latch-up (per JEDEC78) | | | mA |

Notes:

a. Signals on SX, DX, V_L or INX exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 6.6 mW/°C above 70 °C.

d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

| SPECIFICATIONS FOR UNIPOLAR SUPPLIES | | | | | | | | | |
|--------------------------------------|-----------------------|--|--------------------|-------------------|---------------------|-------------------|--------------------|-------------------|------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified V _{CC} = + 12 V, V _L = 2.7 V V _{IN(A, B, C and enable)} = 1.6 V, 0.5 V ^a | Temp. ^b | Typ. ^c | - 40 °C to + 125 °C | | - 40 °C to + 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V _{ANALOG} | | Full | | 0 | 12 | 0 | 12 | V |
| On-Resistance | R _{DS(on)} | I _S = 1 mA, V _D = 0.7 V, 6.0 V, 11.3 V | Room Full | 80 | | 120 | | 120 | Ω |
| On-Resistance Match | ΔR _{ON} | I _S = 1 mA, V _D = + 0.7 V | Room Full | 4 | | 7 | | 7 | |
| On-Resistance Flatness | R _{FLATNESS} | I _S = 1 mA, V _D = 0.7 V, 6.0 V, 11.3 V | Room Full | 32 | | 26 | | 26 | |
| | | | | | | 30 | | 28 | |

| SPECIFICATIONS FOR UNIPOLAR SUPPLIES | | | | | | | | | |
|--|---------------|---|--------------------|-------------------|---------------------|-------------------|--------------------|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_{CC} = +12\text{ V}$, $V_L = 2.7\text{ V}$ $V_{IN(A, B, C \text{ and enable})} = 1.6\text{ V}$, 0.5 V^a | Temp. ^b | Typ. ^c | - 40 °C to + 125 °C | | - 40 °C to + 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Switch Off Leakage Current | $I_{S(off)}$ | $V_+ = +13.2\text{ V}$, $V_L = 2.7\text{ V}$ $V_D = 1\text{ V}/12.2\text{ V}$, $V_S = 12.2\text{ V}/1\text{ V}$ | Room Full | ± 0.02 | - 1 | 1 | - 1 | 1 | nA |
| | $I_{D(off)}$ | | Room Full | ± 0.02 | - 1 | 1 | - 1 | 1 | |
| Channel On Leakage Current | $I_{D(on)}$ | $V_+ = +13.2\text{ V}$, $V_L = 2.7\text{ V}$ $V_D = V_S = 1\text{ V}/12.2\text{ V}$ | Room Full | ± 0.02 | - 1 | 1 | - 1 | 1 | |
| Digital Control | | | | | | | | | |
| Logic Low Input Voltage | V_{INL} | $V_L = 2.7\text{ V}$ | Full | | | 0.5 | | 0.5 | V |
| Logic High Input Voltage | V_{INH} | | Full | | 1.6 | | 1.6 | | |
| Logic Low Input Current | I_L | $V_{IN} A0, A1, A2$ and enable under test = 0.5 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | μA |
| Logic High Input current | I_H | $V_{IN} A0, A1, A2$ and enable above test = 1.6 V | Full | 0.01 | - 1 | 1 | - 1 | 1 | |
| Dynamic Characteristics | | | | | | | | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ see figure 1, 2, 3 | Room Full | 80 | | 135 | | 135 | ns |
| Enable Turn-On Time | $t_{ON(EN)}$ | | Room Full | 115 | | 180 | | 180 | |
| Enable Turn-Off Time | $t_{OFF(EN)}$ | | Room Full | 46 | | 110 | | 110 | |
| Break-Before-Make Time Delay | t_D | | Room Full | 37 | 12 | | 12 | | |
| Charge Injection ^e | Q | $C_L = 1\text{ nF}$, $R_{GEN} = 0\ \Omega$, $V_{GEN} = 0\text{ V}$ | Full | 0.86 | | | | | pC |
| Off Isolation ^e | OIRR | $f = 1\text{ MHz}$, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ | 100 kHz | Room | < - 90 | | | | dB |
| | | | 1 MHz | Room | - 80 | | | | |
| Crosstalk ^e | X_{TALK} | | 10 MHz | Room | - 61 | | | | |
| | | | 100 kHz | Room | < - 90 | | | | |
| | | | 1 MHz | Room | - 81 | | | | |
| | | | 10 MHz | Room | - 65 | | | | |
| Bandwidth, - 3dB ^e | BW | $R_L = 50\ \Omega$ | Room | 540 | | | | MHz | |
| Source Off Capacitance ^e | $C_{S(off)}$ | $f = 1\text{ MHz}$ | Room | 2 | | | | pF | |
| Drain Off Capacitance ^e | $C_{D(off)}$ | | Room | 3 | | | | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | | Room | 6 | | | | | |
| Total Harmonic Distortion ^e | THD | Signal = 1 V_{RMS} , 20 Hz to 20 kHz, $R_L = 600\ \Omega$ | Room | 0.01 | | | | | % |
| Power Supply | | | | | | | | | |
| Power Supply Range | I_+ | $V_{IN(A, B, C \text{ and enable})} = 0\text{ V}$ or + 12 V | Room Full | 0.05 | | 1 | | 1 | μA |
| Ground Current | I_{GND} | | Room Full | 0.05 | - 1 | | - 1 | | |
| Logic Supply Current | I_L | $V_L = 2.7\text{ V}$ | Room Full | 0.05 | | 1 | | 1 | |

Notes:

- V_{IN} = input voltage to perform proper function.
- Room - 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.

| SPECIFICATIONS FOR UNIPOLAR SUPPLIES | | | | | | | | | |
|---|-----------------|--|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_{CC} = +5\text{ V}$, $V_L = 2.7\text{ V}$ $V_{IN(A, B, C \text{ and enable})} = 1.5\text{ V}$, 0.6 V^a | Temp. ^b | Typ. ^c | -40 °C to +125 °C | | -40 °C to +85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | 0 | 5 | 0 | 5 | V |
| On-Resistance | R_{ON} | $I_S = 1\text{ mA}$, $V_D = 0\text{ V}$, $+3.5\text{ V}$ | Room Full | 105 | | 165 205 | | 165 194 | Ω |
| On-Resistance Match | ΔR_{ON} | $I_S = 1\text{ mA}$, $V_D = +3.5\text{ V}$ | Room Full | 3.2 | | 8 13 | | 8 10 | |
| On-Resistance Flatness | $R_{FLATNESS}$ | $I_S = 1\text{ mA}$, $V_D = 0\text{ V}$, $+3\text{ V}$ | Room Full | 17 | | 26 30 | | 26 28 | |
| Switch Off Leakage Current | $I_{S(off)}$ | $V_+ = +5.5\text{ V}$, $V_- = 0\text{ V}$ $V_D = 1\text{ V}/4.5\text{ V}$, $V_S = 4.5\text{ V}/1\text{ V}$ | Room Full | ± 0.02 | -1 -50 | 1 50 | -1 -5 | 1 5 | nA |
| | $I_{D(off)}$ | | Room Full | ± 0.02 | -1 -50 | 1 50 | -1 -5 | 1 5 | |
| Channel On Leakage Current | $I_{D(on)}$ | $V_+ = +5.5\text{ V}$, $V_- = 0\text{ V}$ $V_D = V_S = 1\text{ V}/4.5\text{ V}$ | Room Full | ± 0.02 | -1 -50 | 1 50 | -1 -5 | 1 5 | |
| Digital Control | | | | | | | | | |
| $V_{IN(A, B, C \text{ and enable})}$ Low | V_{IL} | $V_L = 2.7\text{ V}$ | Full | | | 0.6 | | 0.6 | V |
| $V_{IN(A, B, C \text{ and enable})}$ High | V_{IH} | $V_L = 2.7\text{ V}$ | Full | | 1.5 | | 1.5 | | |
| Input Current, V_{IN} Low | I_L | $V_{IN(A, B, C \text{ and enable})}$ under test = 0.6 V | Full | 0.01 | -1 | 1 | -1 | 1 | μA |
| Input Current, V_{IN} High | I_H | $V_{IN(A, B, C \text{ and enable})}$ under test = 1.5 V | Full | 0.01 | -1 | 1 | -1 | 1 | |
| Dynamic Characteristics | | | | | | | | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ see figure 1, 2, 3 | Room Full | 96 | | 175 250 | | 175 210 | ns |
| Enable Turn-On Time | t_{ON} | | Room Full | 200 | | 295 365 | | 295 330 | |
| Enable Turn-Off Time | t_{OFF} | | Room Full | 60 | | 155 225 | | 155 190 | |
| Break-Before-Make Time Delay | t_D | | Room Full | 50 | 20 | | 20 | | |
| Charge Injection ^e | Q | $V_g = 0\text{ V}$, $R_g = 0\ \Omega$, $C_L = 1\text{ nF}$ | Full | 0.4 | | | | | pC |
| Off Isolation ^e | OIRR | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 100\text{ kHz}$ | Room | < -90 | | | | | dB |
| Channel-to-Channel Crosstalk ^e | X_{TALK} | | Room | < -90 | | | | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | f = 1 MHz | Room | 2 | | | | | pF |
| Drain Off Capacitance ^e | $C_{D(off)}$ | | Room | 4 | | | | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | | Room | 7 | | | | | |
| Power Supply | | | | | | | | | |
| Power Supply Current | I_+ | $V_{IN(A, B, C \text{ and enable})} = 0\text{ V}$ or 5 V | Room Full | 0.05 | | 1 10 | | 1 10 | μA |
| Ground Current | I_{GND} | | Room Full | -0.05 | -1 -10 | | -1 -10 | | |
| Logic Supply Current | I_L | $V_L = 2.7\text{ V}$ | Room Full | 0.05 | | 1 10 | | 1 10 | |

Notes:

- a. V_{IN} = input voltage to perform proper function.
- b. Room - 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.

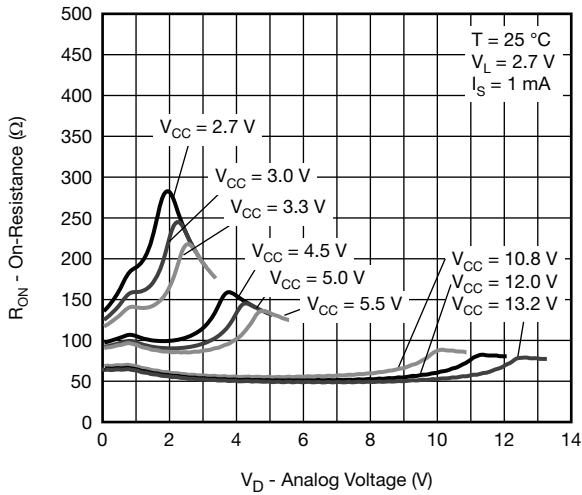
| SPECIFICATIONS FOR UNIPOLAR SUPPLIES | | | | | | | | | |
|--------------------------------------|---------------|--|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_{CC} = +3\text{ V}$, $V_L = 2.7\text{ V}$ $V_{IN(A, B, C \text{ and enable})} = 1.5\text{ V}$, 0.6 V^a | Temp. ^b | Typ. ^c | -40 °C to +125 °C | | -40 °C to +85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | 0 | 3 | 0 | 3 | V |
| On-Resistance | $R_{DS(on)}$ | $I_S = 1\text{ mA}$, $V_D = 1.5\text{ V}$ | Room Full | 171 | | 265 310 | | 265 289 | Ω |
| Switch Off Leakage Current | $I_{S(off)}$ | $V_+ = 3.3\text{ V}$, $V_L = 2.7\text{ V}$ $V_D = 0.3\text{ V}/3.0\text{ V}$, $V_S = 3.0\text{ V}/0.3\text{ V}$ | Room Full | ± 0.02 | -1 -50 | 1 50 | -1 -5 | 1 5 | nA |
| | $I_{D(off)}$ | | Room Full | ± 0.02 | -1 -50 | 1 50 | -1 -5 | 1 5 | |
| Channel On Leakage Current | $I_{D(on)}$ | $V_+ = 3.3\text{ V}$, $V_L = 2.7\text{ V}$ $V_S = V_D = 0.3\text{ V}/3.0\text{ V}$ | Room Full | ± 0.02 | -1 -50 | 1 50 | -1 -5 | 1 5 | |
| Digital Control | | | | | | | | | |
| Logic Low Input Voltage | V_{INL} | $V_L = +2.7\text{ V}$ | Full | | | 0.6 | | 0.6 | V |
| Logic High Input Voltage | V_{INH} | | Full | | 1.5 | | 1.5 | | |
| Logic Low Input Current | I_L | $V_{IN} A0, A1, A2$ and enable under test = 0.6 V | Full | 0.01 | -1 | 1 | -1 | 1 | μA |
| Logic High Input Current | I_H | $V_{IN} A0, A1, A2$ and enable above test = 1.5 V | Full | 0.01 | -1 | 1 | -1 | 1 | |
| Dynamic Characteristics | | | | | | | | | |
| Transition Time | t_{TRANS} | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ see figure 1, 2, 3 | Room Full | 151 | | 270 355 | | 270 315 | ns |
| Enable Turn-On Time | $t_{ON(EN)}$ | | Room Full | 390 | | 510 610 | | 510 565 | |
| Enable Turn-Off Time | $t_{OFF(EN)}$ | | Room Full | 90 | | 220 320 | | 220 275 | |
| Break-Before-Make Time Delay | t_D | | Room Full | 90 | 35 | | 35 | | |
| Charge Injection ^e | Q | $C_L = 1\text{ nF}$, $R_{GEN} = 0\ \Omega$, $V_{GEN} = 0\text{ V}$ | Full | 0.5 | | | | | pC |
| Off Isolation ^e | OIRR | $f = 1\text{ MHz}$, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ | Room | < -90 | | | | | dB |
| Crosstalk ^e | X_{TALK} | | Room | < -90 | | | | | |
| Source Off Capacitance ^e | $C_{S(off)}$ | $f = 1\text{ MHz}$ | Room | 2 | | | | | pF |
| Drain Off Capacitance ^e | $C_{D(off)}$ | | Room | 4 | | | | | |
| Channel On Capacitance ^e | $C_{D(on)}$ | | Room | 7 | | | | | |
| Power Supply | | | | | | | | | |
| Power Supply Range | I_+ | $V_{IN(A, B, C \text{ and enable})} = 0\text{ V or } +3\text{ V}$ | Room Full | 0.05 | | 1 10 | | 1 10 | μA |
| Ground Current | I_{GND} | | Room Full | 0.05 | -1 -10 | | -1 -10 | | |
| Logic Supply Current | I_L | $V_L = 2.7\text{ V}$ | Room Full | 0.05 | | 1 10 | | 1 10 | |

Notes:

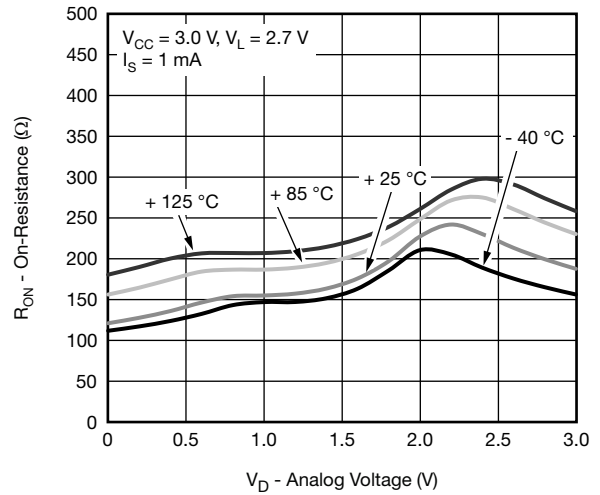
- V_{IN} = input voltage to perform proper function.
- Room - 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

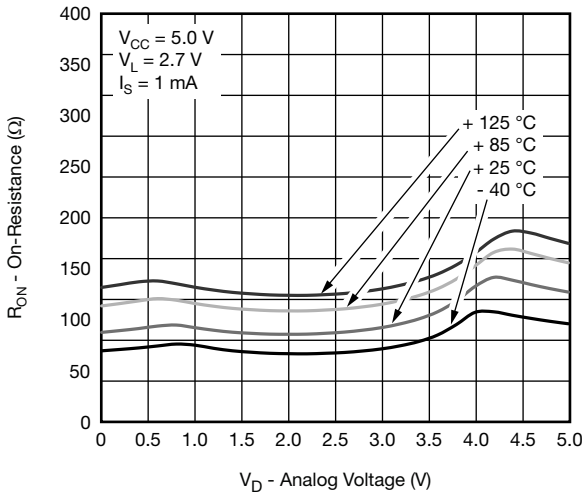
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



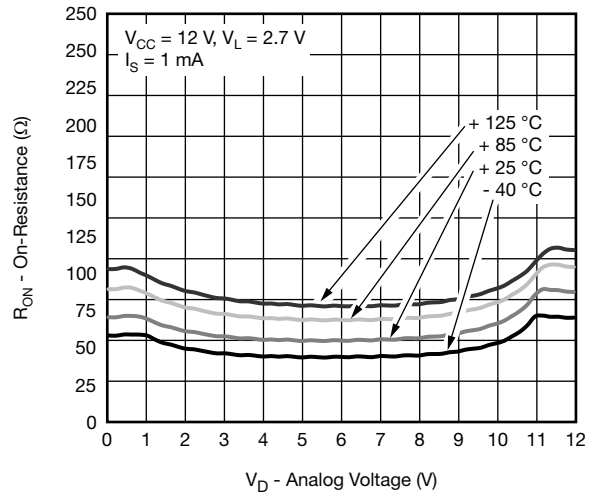
On-Resistance vs. V_D and Signal Supply Voltage



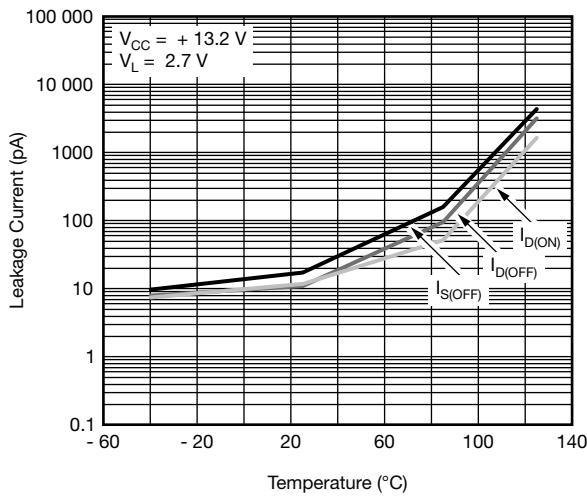
On-Resistance vs. Analog Voltage and Temperature



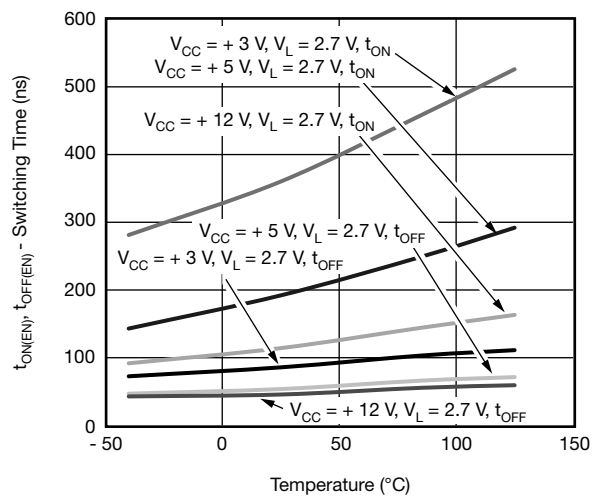
On-Resistance vs. Analog Voltage and Temperature



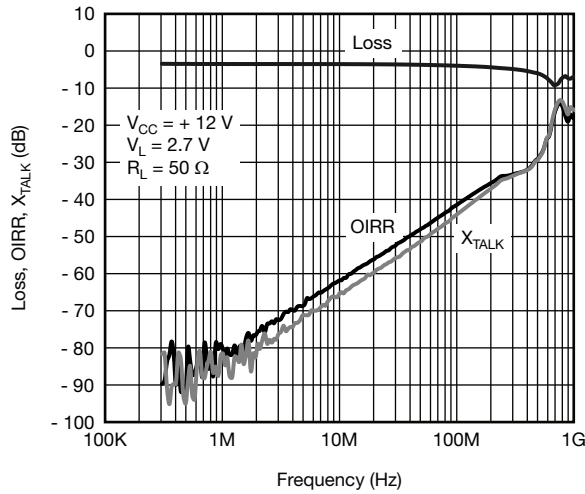
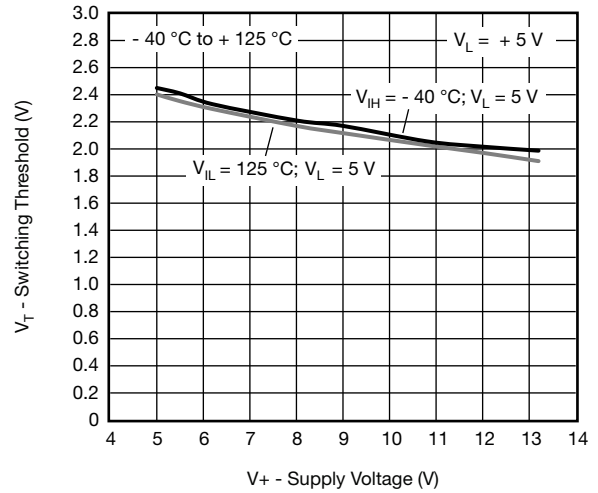
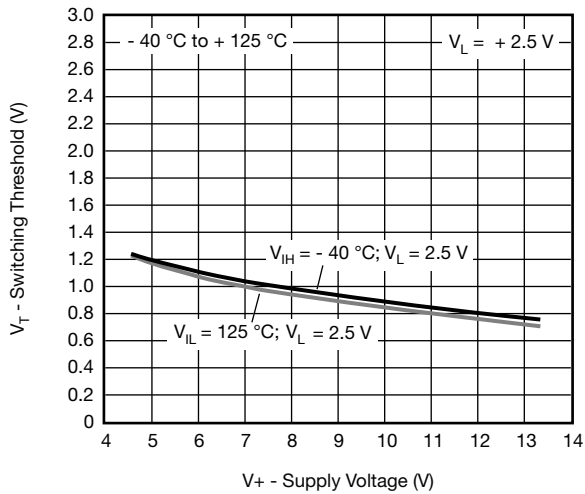
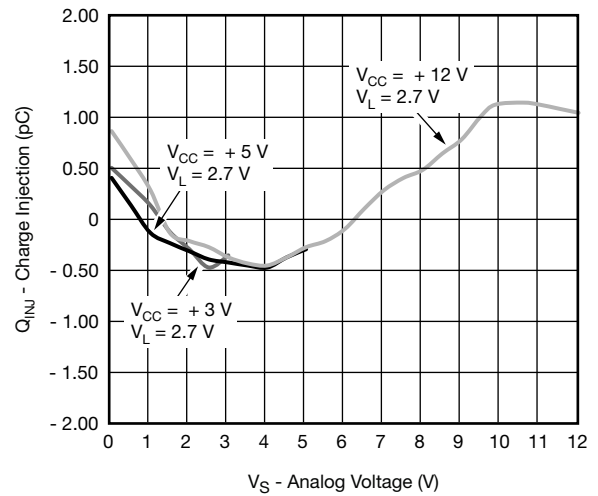
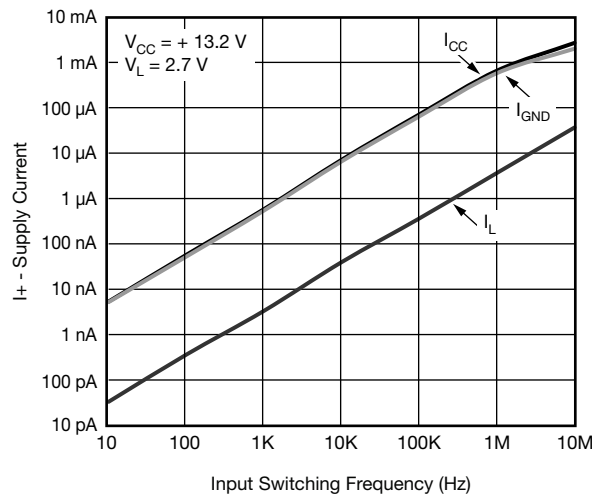
On-Resistance vs. Analog Voltage and Temperature



Leakage Current vs. Temperature



Switching Time vs. Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

Switching Threshold vs. Logic Supply Voltage

Switching Threshold vs. Logic Supply Voltage

Charge Injection vs. Analog Voltage

Current vs. Frequency

TEST CIRCUITS

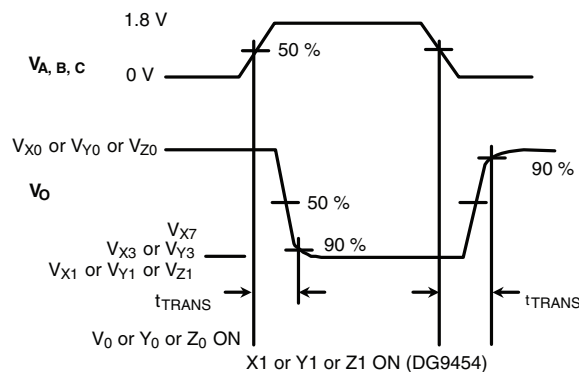
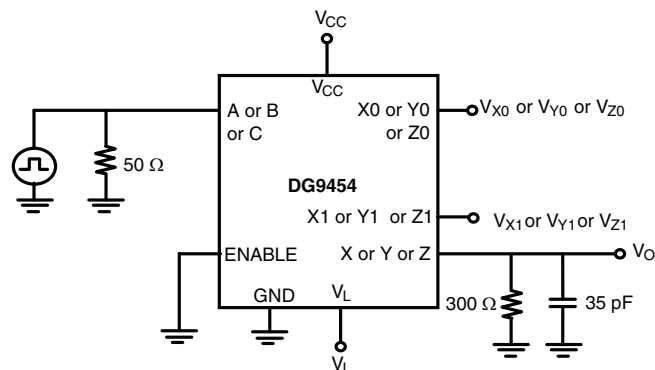


Figure 1. Transition Time

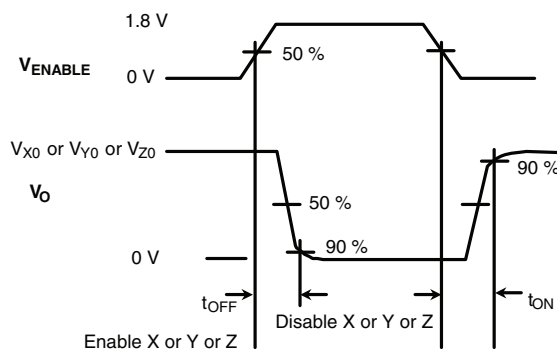
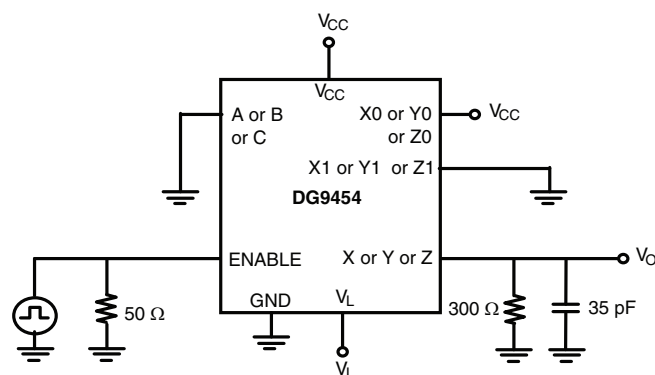


Figure 2. Enable Switching Time

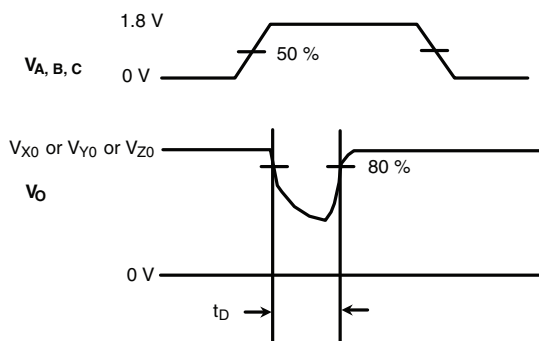
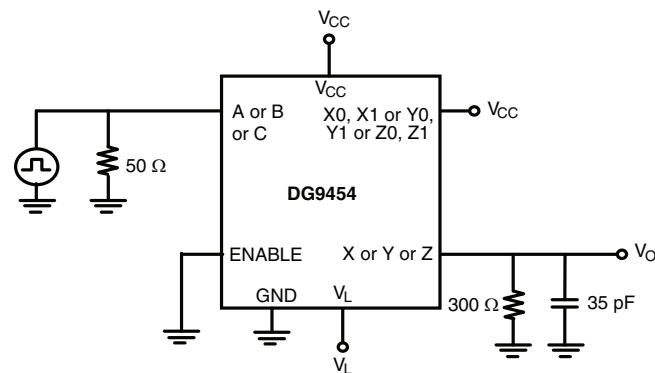
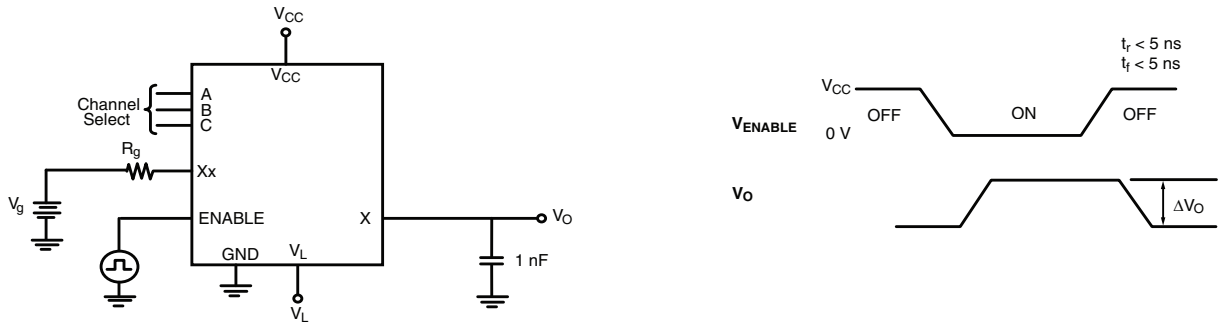
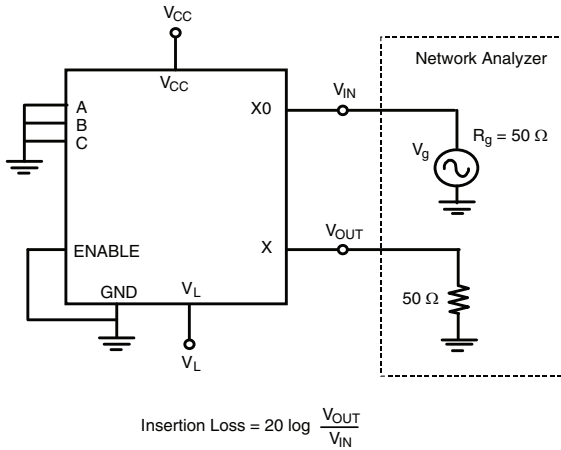
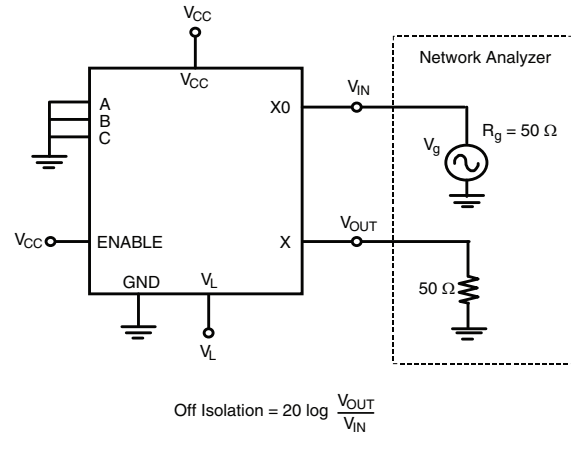
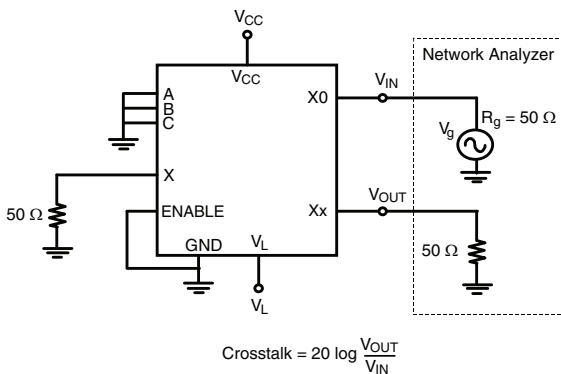
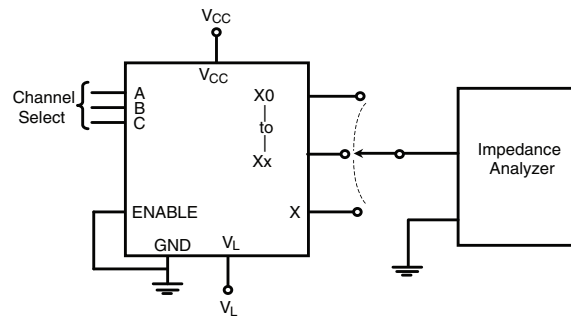


Figure 3. Break-Before-Make

TEST CIRCUITS

Figure 4. Charge Injection

Figure 5. Insertion Loss

Figure 6. Off Isolation

Figure 7. Crosstalk

Figure 8. Source, Drain Capacitance

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