



SANYO Semiconductors

# DATA SHEET

An ON Semiconductor Company

## LV8162TT — Bi-CMOS IC Fan Motor Driver Single-Phase Full-Wave Driver

### Overview

The LV8162TT is a driver IC for single-phase fan motors that achieves low-noise operation by using BTL linear output system. As it has a variable speed function in response to the external PWM input signal, it is best suited for driving CPU cooling fans in notebook PCs and other applications that require low power consumption, low noise, and a variable speed function.

### Functions

- Single-phase full-wave operating by BTL output
- Hall bias output pin
- Standby mode and quick start function
- FG (rotation speed detection) signal pin and RD (lock detection) signal pin
- Built-in thermal-shutdown (TSD) circuit
- Speed control available by PWM pin
- Built-in lock protection and automatic return circuit
- Start auxiliary function (50% duty start)

### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		7	V
Maximum output current	I <sub>OUT</sub> max		0.7	A
OUT pin output withstand voltage	V <sub>OUT</sub> max		7	V
HB pin maximum output current	I <sub>HB</sub> max		10	mA
PWM pin withstand voltage	V <sub>PWM</sub> max		7	V
FG/RD pin maximum sink current	I <sub>FG/RD</sub> max		5	mA
FG/RD pin output withstand voltage	V <sub>FG/VRD</sub> max		7	V
Allowable dissipation	Pd max1	Independent IC	200	mW
	Pd max2	With specified substrate *1	400	mW
Operating temperature	T <sub>opr</sub>	*2	-30 to +95	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

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# LV8162TT

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\* 1: Specified substrate : 20mm × 10mm × 0.8mm, Paper phenol

\* 2: Tj max=150°C must not be exceeded

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

## Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V <sub>CC</sub>		5.0	V
Operating supply voltage range	V <sub>CC op</sub>		2.0 to 6.0	V
Hall input voltage range	V <sub>ICM</sub>		0.2 to V <sub>CC</sub> -1.2	V
PWM input frequency	f <sub>PWM IN</sub>		20 to 60	kHz

## Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 5V

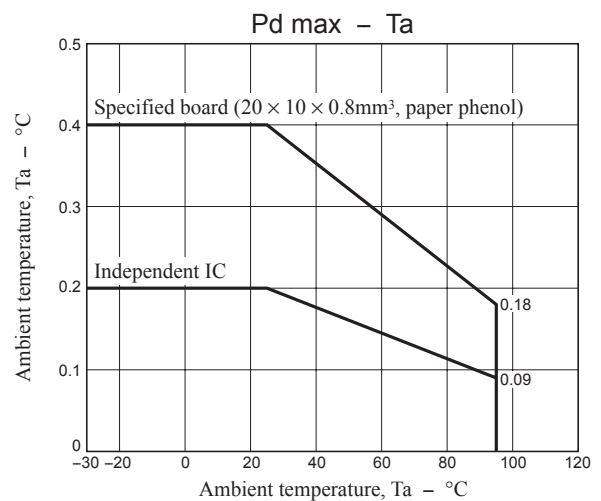
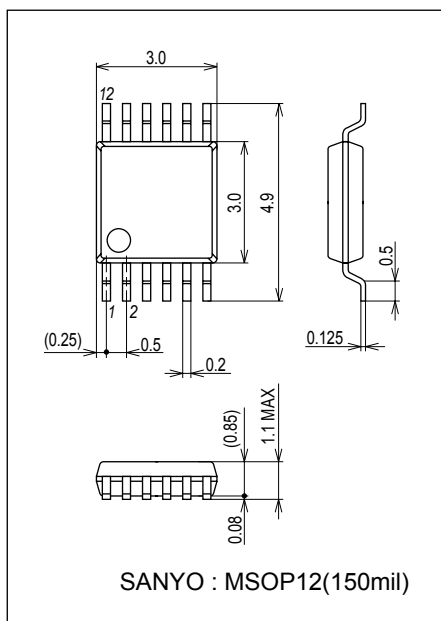
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I <sub>CC</sub>		0.95	1.3	1.6	mA
	I <sub>CC st</sub>			10	30	μA
HB pin voltage	V <sub>HB</sub>	When I <sub>REG</sub> = 5mA	0.9	1.03	1.2	V
OUT pin high voltage	V <sub>OH</sub>			0.16	0.23	V
OUT pin low voltage	V <sub>OL</sub>	I <sub>O</sub> = 250mA, source + sink		0.1	0.15	V
Hall amplifier input offset voltage	V <sub>IN OFS</sub>		-6		6	mV
Hall amplifier voltage gain	GH		44	45.5	47	dB
PWM pin input low level	V <sub>PWML</sub>	V <sub>SET</sub> = 0.5V	0		V <sub>CC</sub> ×0.2	V
PWM pin input high level	V <sub>PWMH</sub>	V <sub>SET</sub> = 0.5V	V <sub>CC</sub> ×0.8		6	V
FG/RD pin low voltage	V <sub>FG L</sub> /V <sub>RD L</sub>	ICPRTO = ICPC/ICPD			0.3	V
FG/RD pin leakage current	I <sub>FG L</sub> /I <sub>RD L</sub>				10	μA
FG comparator hysteresis width	FGHYS	V <sub>SET</sub> = 0.5V		±8	±16	sec
Lock detection output ON time	LT1		0.4	0.6	0.8	μsec
Lock detection output OFF time	LT2	I <sub>FG</sub> = 3mA	4	6	8	V
Lock detection output ON/OFF ratio	LRTO	V <sub>FG</sub> = 5V	8	10	12	
Thermal shutdown operating temperature	TSD	Design guarantee *		180		°C
Thermal shutdown hysteresis width	ΔTSD	Design guarantee *		30		°C

\* Design guaranteed value (No measurement is performed.)

## Package Dimensions

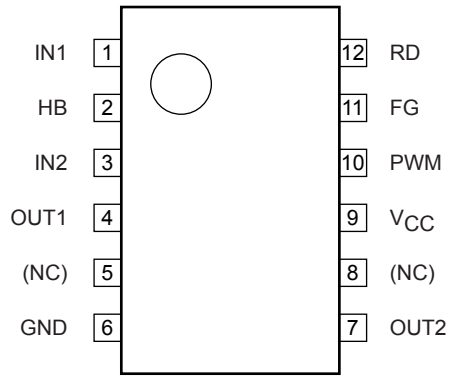
unit : mm (typ)

3375



# LV8162TT

## Pin Assignment



Top view

## Truth value table

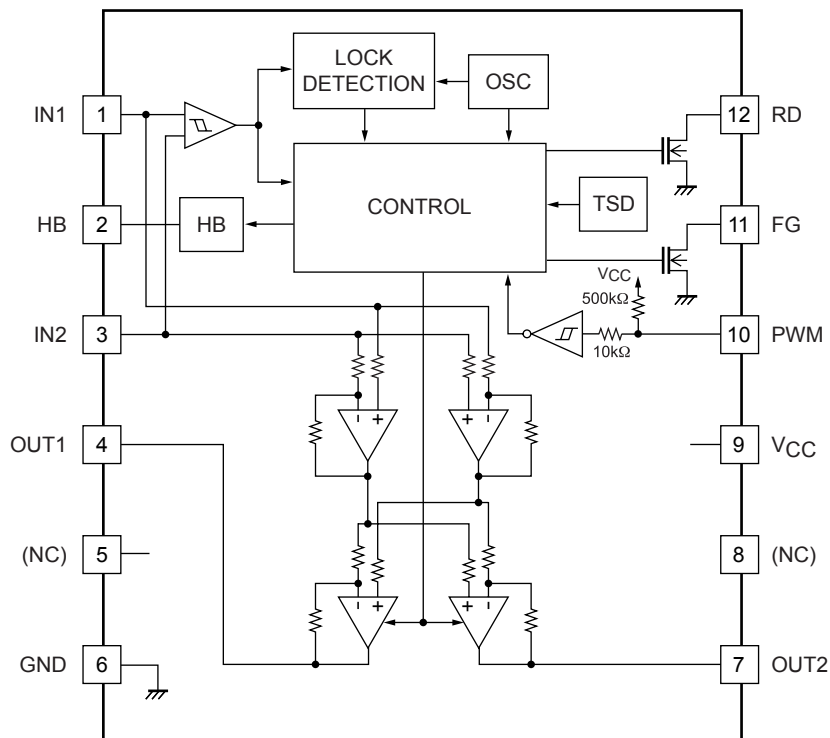
IN1	IN2	PWM	OUT1	OUT2	FG	RD	Mode
H	L	H	L	H	OFF	L	Drive (OUT2 → OUT1)
		L		L		Regeneration	
		*		OFF		Lock protection. See *1	
L	H	H	H	L	L	L	Drive (OUT1 → OUT2)
		L	L			Regeneration	
		*	OFF			Lock protection. See *1	
*		L	L	L	OFF	L	Standby mode. See *2

\*1: If no FG pulse switching occurs while the lock detection output is on, the IC enters lock protection mode.

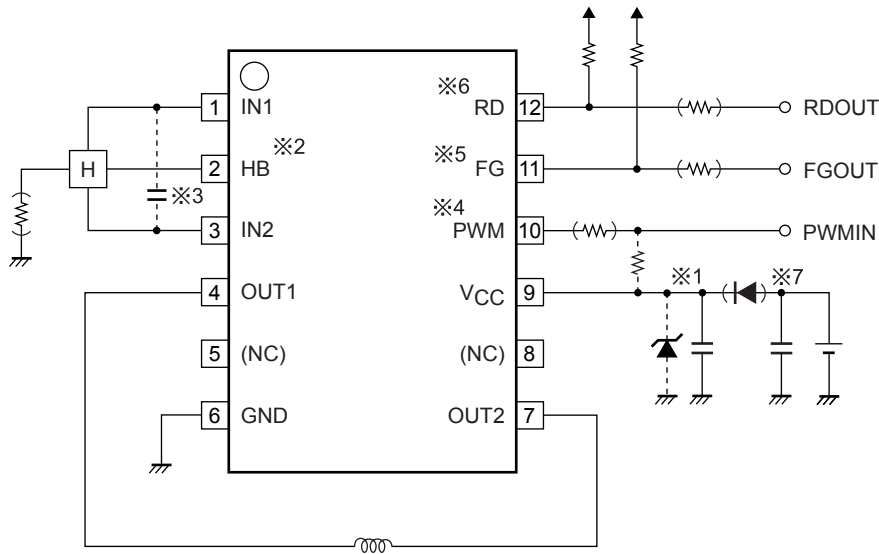
\*2: If "lock protection operation + PWM input low time" is 750μs or longer is satisfied, the IC enters standby mode.

The IC enters standby mode at a low time of 750μs only when the IC is started with low PWM input when the power is turned on.

## Block Diagram



Application Circuit Example



\*1 [Power stabilization capacitor]

Be sure to use the power stabilization capacitor with a capacitance of 1μF or higher. It cannot be removed. The VCC and GND are connected using a pattern that is think and short as possible. When a reverse-connection breakdown prevention diode is used and the supply voltage rises due to a coil kickback or other cause, increase the capacitance of the capacitor or use a zener diode between the power supply and GND to ensure that the absolute maximum rating is not exceeded.

This IC performs synchronous rectification for reducing heat generation and improving efficiency. The synchronous rectification can return the current to the power supply side under certain operating conditions.

- When the output duty drops suddenly
- When the PWM input frequency is low

The amount of increase in the supply voltage varies depending on whether a reverse-connection breakdown prevention diode is used, on the size of the power supply capacitor, and fan type, and so these factoes must be fully taken into consideration.

When the supply voltage rises, in the same way as above, increase the capacitance of the capacitor or use a zener diode between the power supply and GND to ensure that the absolute maximum rating is not exceeded.

\*2 [HB pin]

Constant-voltage output pin. This is used for Hall element bias purposes. If the HB pin is not needed because the bias current to the Hall element is supplied from the power supply, pull this pin down to GND with a resistor of about 1kΩ. The power supply bias and HB pin bias cannot be used at the same time. To adjust the amplitude of the Hall element, insert a resistor between the Hall element and GND.

\*3 [IN1 and IN2 pins]

Hall element signal input pin. The wiring must be made as short as possible to prevent carring of noise. If noise is carried, insert a capacitor between IN1 and IN2 pins. The Hall input level must satisfy the following condition:  
 Difference voltage between IN1 and IN2 > Operating voltage / Hall amplifier gain + Hall amplifier input offset.

### \*4 [PWM pin]

Speed control signal input pin.

The PWM pin is pulled up with a 500k $\Omega$  resistor inside the IC.

The 500k $\Omega$  is used for setting full speed when the PWM pin is open, and if speed control is to be performed by open collector (open drain) input, it is necessary to pull up the pin using a resistor of an appropriate value.

If speed control is performed using a push-pull input, a pull-up resistor is not required.

When the speed control is performed using the open collector input above, or when push-pull input is used and no pull-up resistor is used, the IC can be used without a sequence (power supply and PWM input can be turned on in any order).

It is recommended that a resistor of 1k $\Omega$  or more is connected in series to protect the pin against misconnection such as ground open and reverse connection.

### \*5 [FG pin]

Rotational speed detection pin.

This is open drain output that can detect the rotational speed by the FG output in response to the phase switching signal.

This pin is held off when in standby mode.

Keep this pin open when it is not to be used.

It is recommended that a resistor of 1k $\Omega$  or more is connected in series to protect the pin against misconnection such as ground open and reverse connection.

### \*6 [RD pin]

Lock detection pin.

This is open drain output that is low during rotation, off when lockup is detected, and low when in standby mode.

Keep this pin open when it is not to be used.

It is recommended that a resistor of 1k $\Omega$  or more is connected in series to protect the pin against misconnection such as ground open and reverse connection.

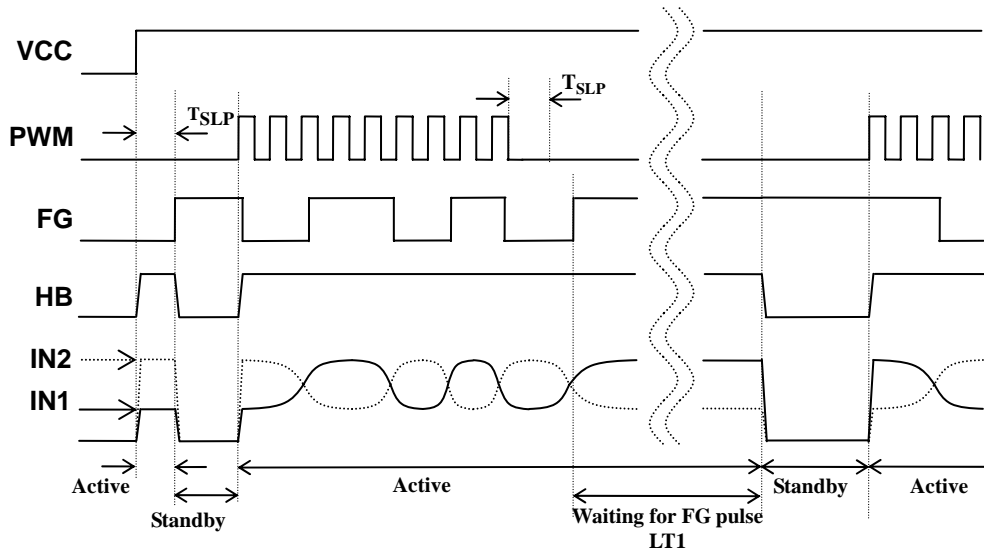
### \*7 [Low current consumption during standby]

The fan motor controlled using this IC can be set to a current consumption of 10 $\mu$ A (room temperature, typ.) when in standby mode. However, note that it will not become 10 $\mu$ A under any of the following conditions.

- When the Hall element bias current is fed from the power supply  
→ The current flowing to the Hall element is increased
- When connecting a pull-up resistor to the PWM pin.  
→ Because the PWM pin must be set to low when in standby mode, the current flowing to the pull-up resistor is increased.
- When using an RD pin.  
→ Because the RD pin is held low when in standby mode, the current flowing to the pull-up resistor is increased.

## Timing Chart

Standby/Operate switchover



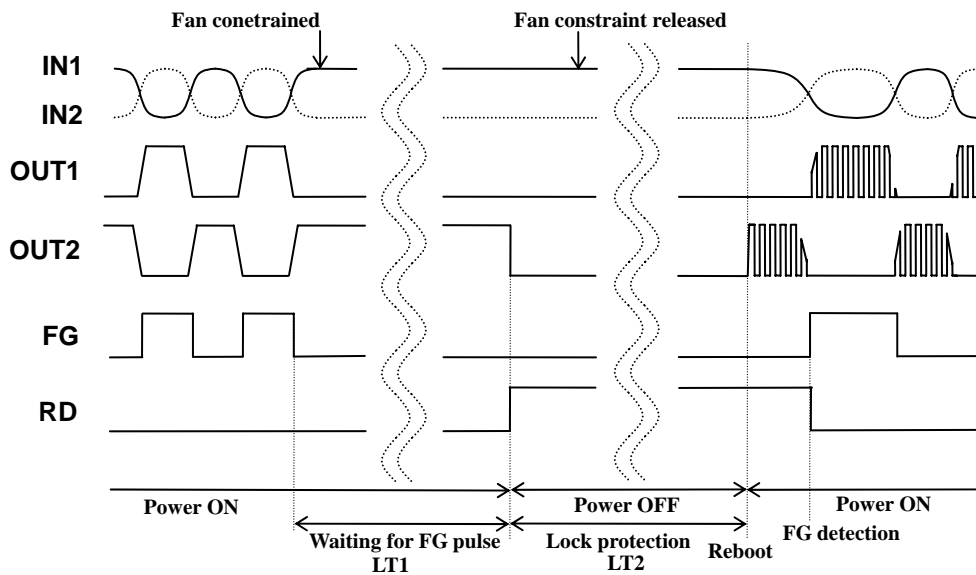
\*1  $T_{SLP}=750\mu s(Typ)$

\*2 If the PWM signal is held low during the TSLP period and no FG signal switching occurs during the LT1 period, the IC enters standby mode.

Only when the power is turned on, if the PWM signal is held low during the TSLP period, the IC enters standby mode.

\*3 The FG pin is off and the RD pin is low in standby mode.

## Lock protection



\*1 Both OUT1 and OUT2 are low when lock protection mode is established.

\*2 In the lock protection period, RD is set to off. After lock protection mode is released, RD is set to low when FG signal is switched (OFF → L or L → OFF)

\*3 If PWM is held low for a period longer than the TSLP when lock protection mode is established, the IC enters standby mode.

\*4 Driving starts at 50% duty cycle when the power is turned on, lock protection mode is released, or the IC is returned from standby mode. (period during which FG switches 5 or 6 times)

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