

Low $V_{CE(sat)}$ PNP Epitaxial Planar Transistor

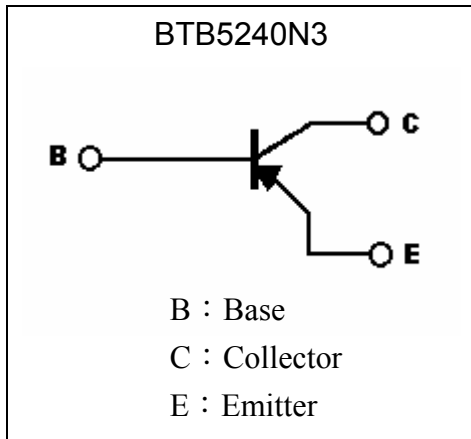
BTB5240N3

BV_{CEO}	-40V
I_C	-2A
$R_{CESAT}(typ.)$	0.106 Ω

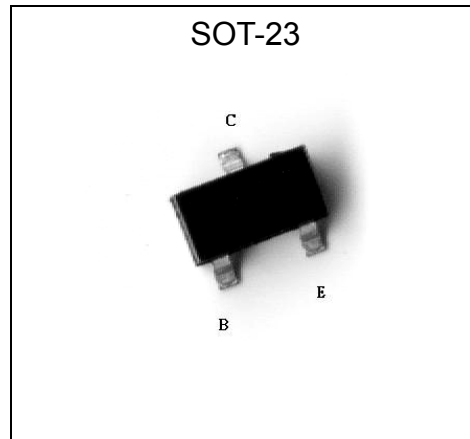
Features

- Excellent DC current gain characteristics
- Low Saturation Voltage
 $V_{CE(sat)} = -0.18V (typ.) (I_C = -2A, I_B = -200mA)$.
- Pb-free lead plating and halogen-free package

Symbol



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-40	V
Collector-Emitter Voltage	V_{CEO}	-40	V
Emitter-Base Voltage	V_{EBO}	-7	V
Collector Current(DC)	I_C	-2	A
Collector Current(Pulsed)(Note 1)	I_{CP}	-3	
Power Dissipation	P_D	300 (Note 2)	mW
		480 (Note 3)	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^{\circ}C/W$
		260	
Operating Junction Temperature Range	T_j	-65~+150	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65~+150	$^{\circ}C$

Note 1: Single pulse, $P_w \leq 10ms$, Duty Cycle $\leq 30\%$.

2. Device mounted on a FR-4 board of 2 oz, single sided copper, with area of minimum pad size.

3. Device mounted on a FR-4 board of 2 oz, single sided copper, with area of 1 cm².

**Characteristics (Ta=25°C)**

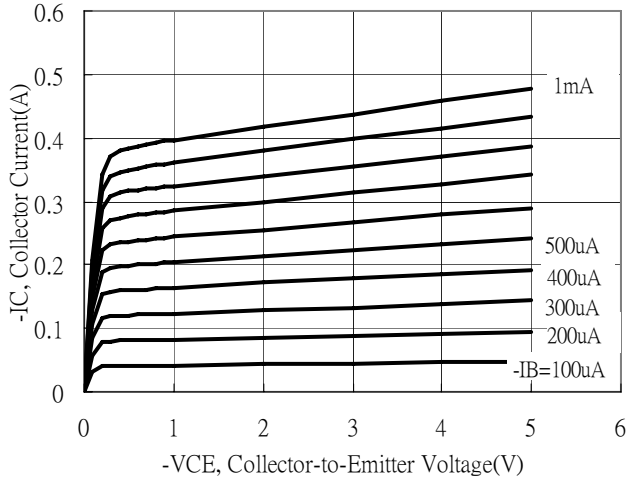
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-40	-	-	V	$I_C=-50\mu A$
BV_{CEO}	-40	-	-	V	$I_C=-1mA$
BV_{EBO}	-7	-	-	V	$I_E=-50\mu A$
I_{CBO}	-	-	-100	nA	$V_{CB}=-40V$
I_{EBO}	-	-	-100	nA	$V_{EB}=-5V$
* $V_{CE(sat) 1}$	-	-53	-80	mV	$I_C=-100mA, I_B=-1mA$
* $V_{CE(sat) 2}$	-	-53	-80	mV	$I_C=-500mA, I_B=-50mA$
* $V_{CE(sat) 3}$	-	-105	-160	mV	$I_C=-750mA, I_B=-15mA$
* $V_{CE(sat) 4}$	-	-106	-160	mV	$I_C=-1A, I_B=-50mA$
* $V_{CE(sat) 5}$	-	-180	-230	mV	$I_C=-2A, I_B=-200mA$
* R_{CESAT}	-	106	160	m Ω	$I_C=-500mA, I_B=-50mA$
* $V_{BE(sat)}$	-	-0.96	-1.1	V	$I_C=-2A, I_B=-200mA$
* $V_{BE(on)}$	-	-0.65	-0.75	V	$V_{CE}=-2V, I_C=-100mA$
* $h_{FE 1}$	300	-	600	-	$V_{CE}=-2V, I_C=-100mA$
* $h_{FE 2}$	260	-	-	-	$V_{CE}=-2V, I_C=-500mA$
* $h_{FE 3}$	210	-	-	-	$V_{CE}=-2V, I_C=-1A$
* $h_{FE 4}$	100	-	-	-	$V_{CE}=-2V, I_C=-2A$
f_T	100	190	-	MHz	$V_{CE}=-10V, I_C=-100mA, f=100MHz$
Cob	-	26	-	pF	$V_{CB}=-10V, I_E=0A, f=1MHz$

*Pulse Test: Pulse Width $\leq 380\mu s$, Duty Cycle $\leq 2\%$ **Ordering Information**

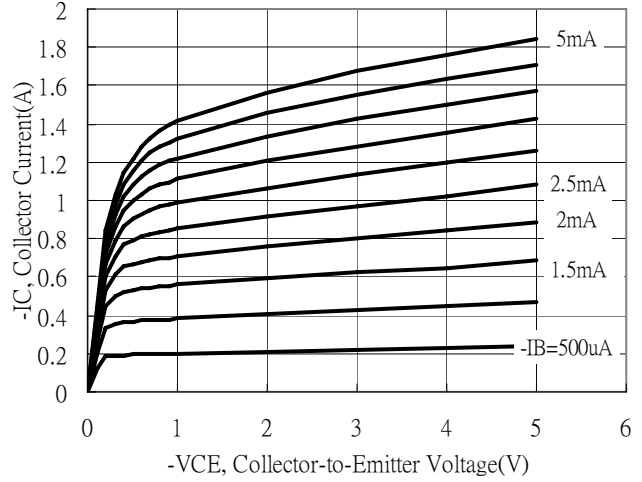
Device	Package	Shipping
BTB5240N3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel

Typical Characteristics

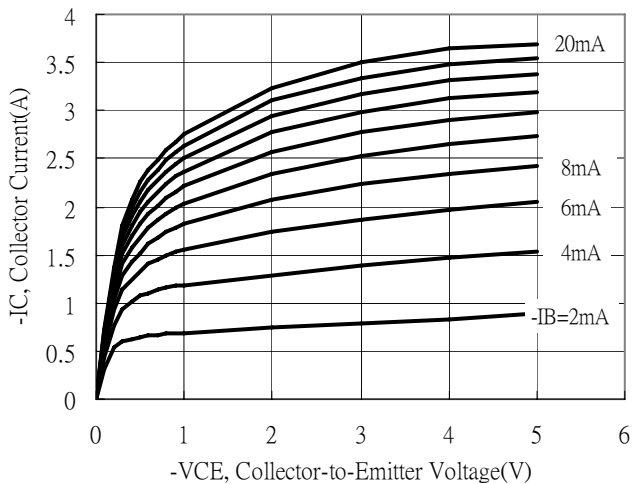
Emitter Grounded Output Characteristics



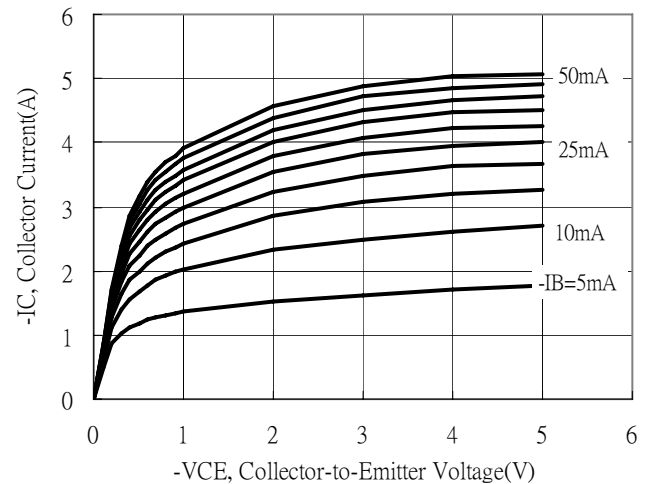
Emitter Grounded Output Characteristics



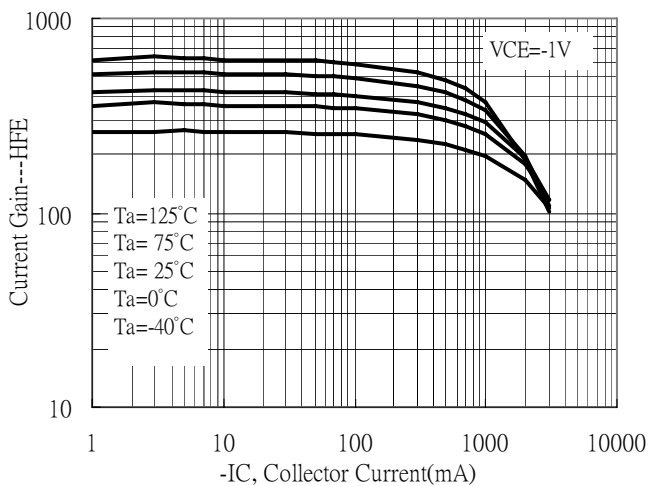
Emitter Grounded Output Characteristics



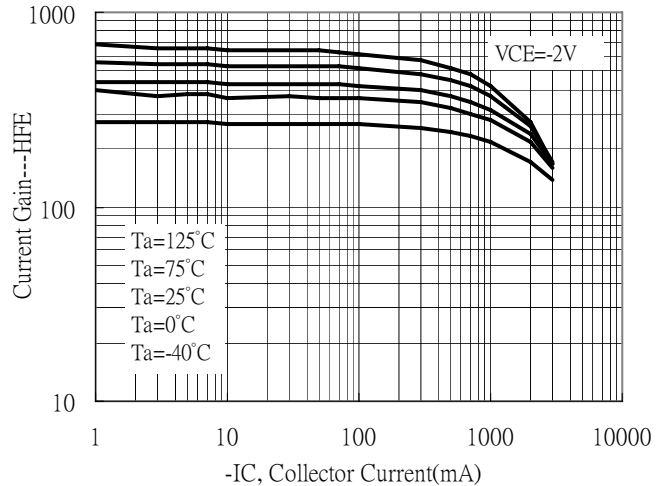
Emitter Grounded Output Characteristics



Current Gain vs Collector Current

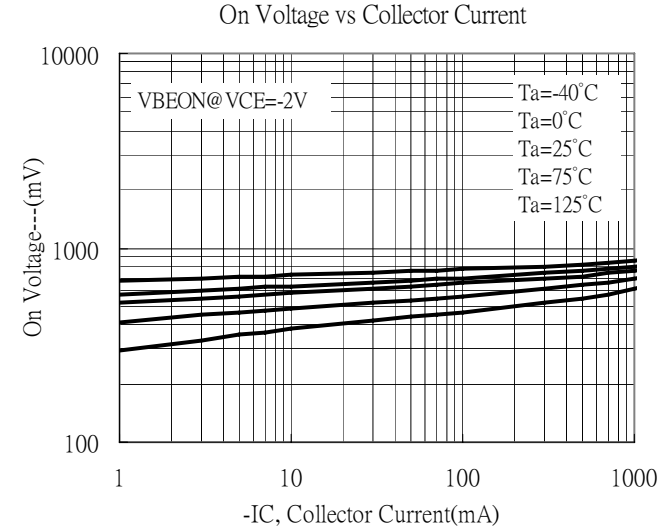
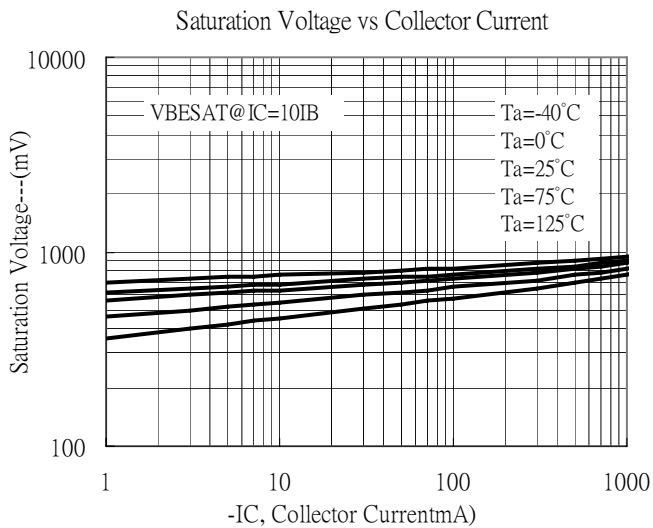
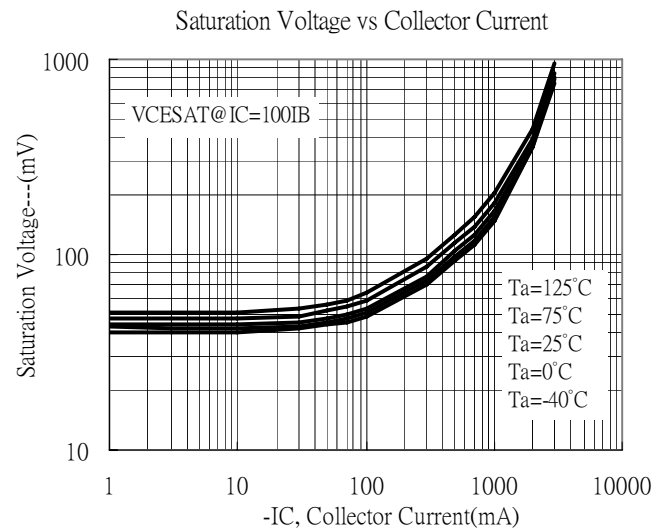
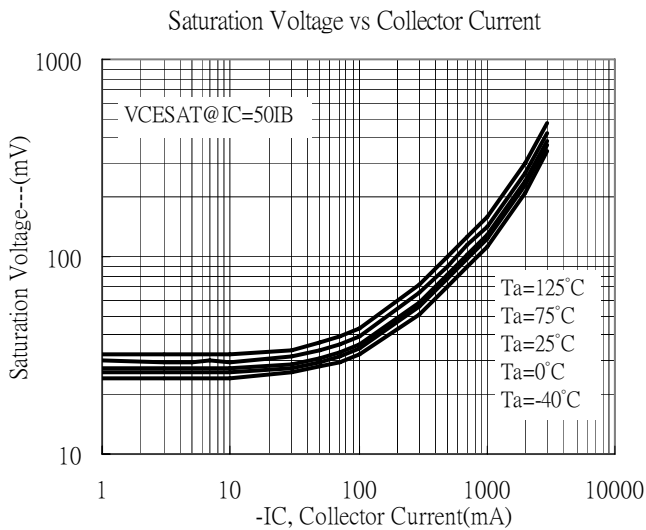
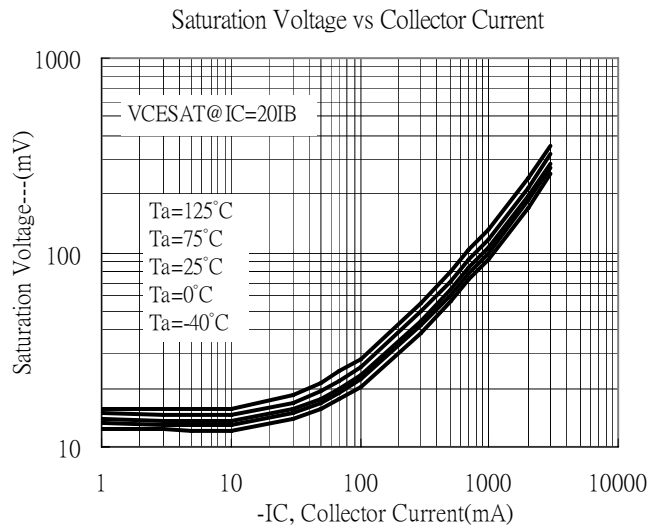
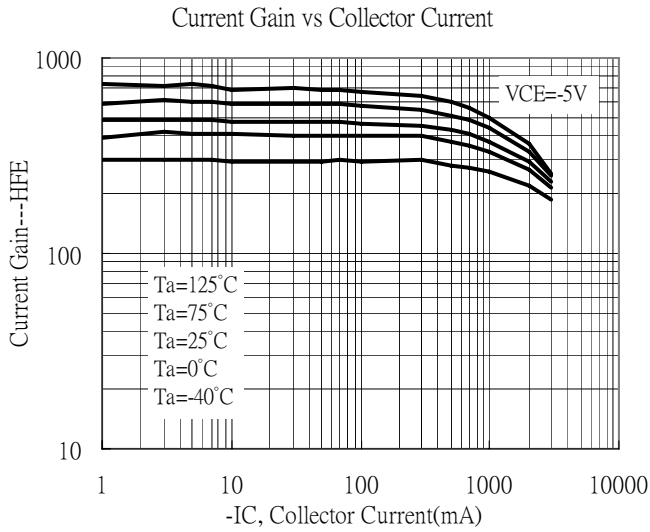


Current Gain vs Collector Current



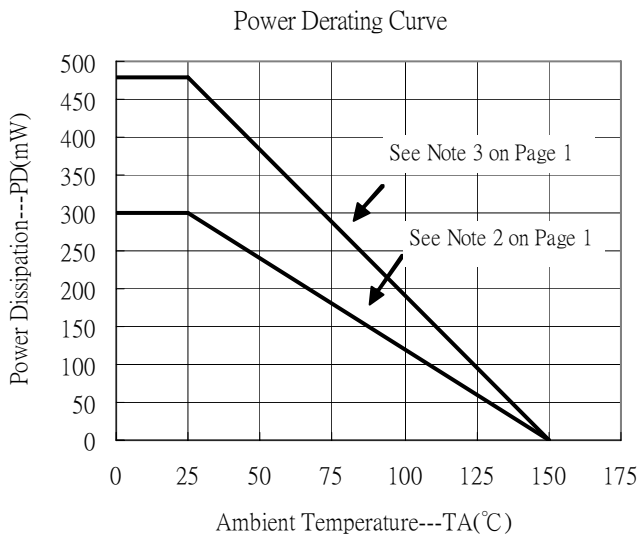
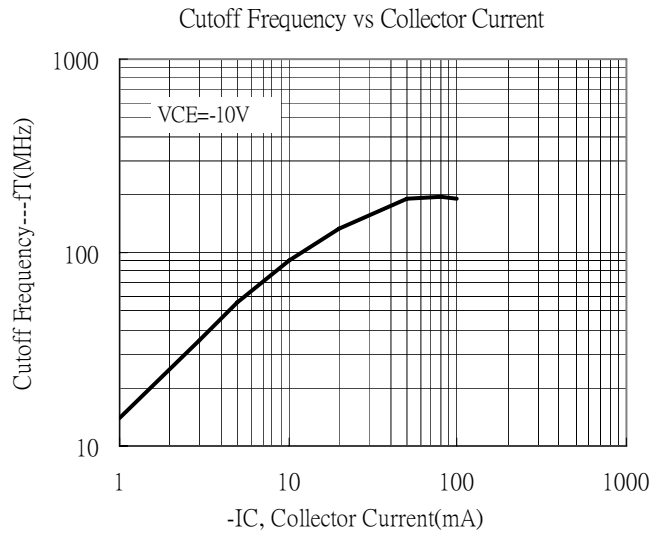
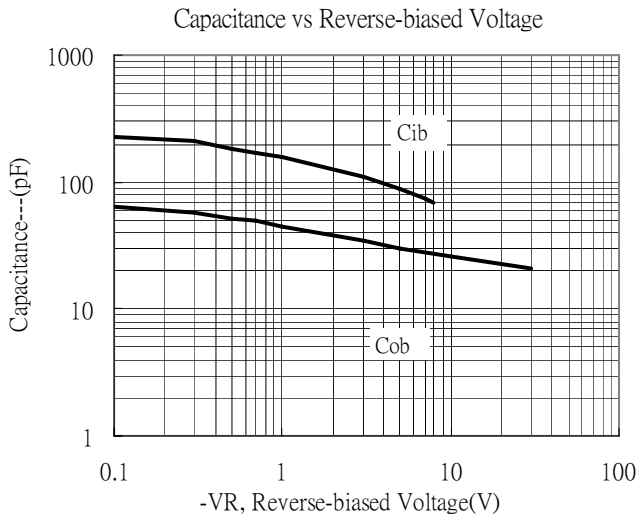


Typical Characteristics(Cont.)

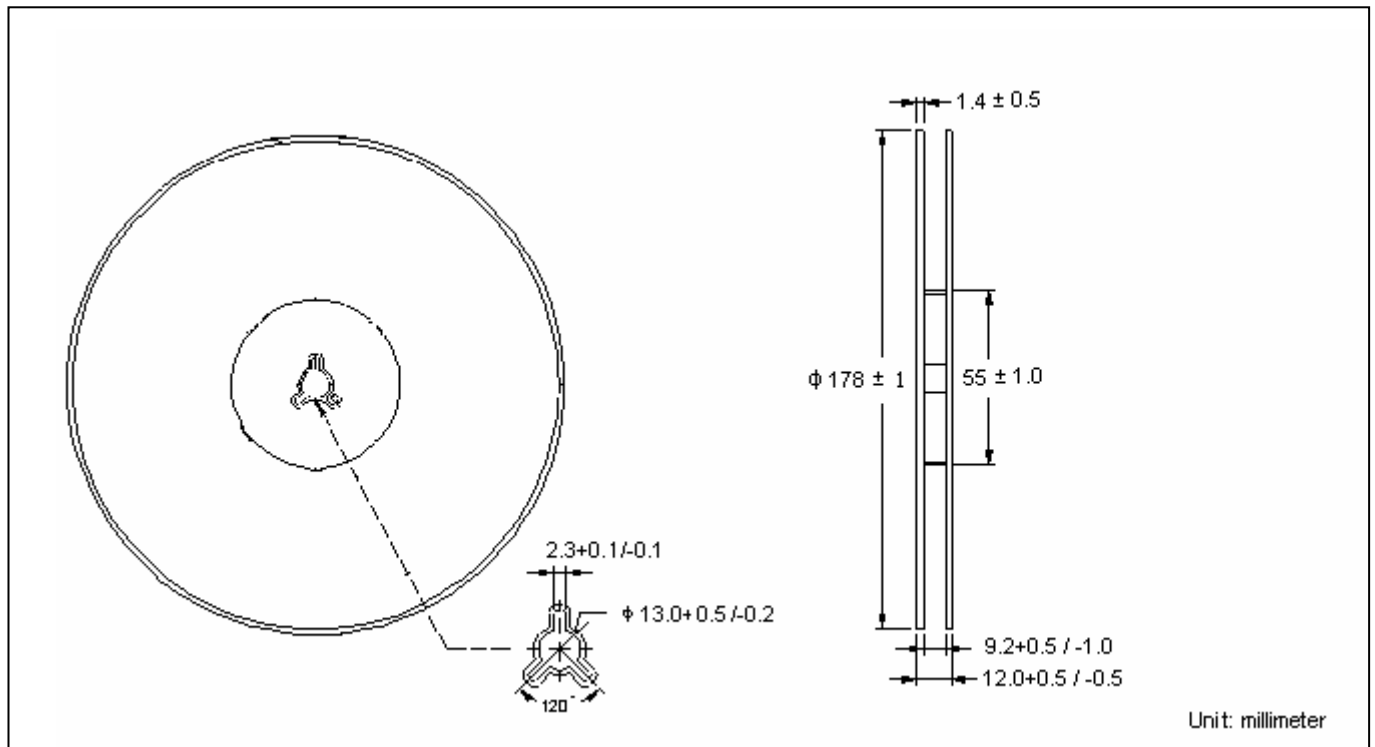




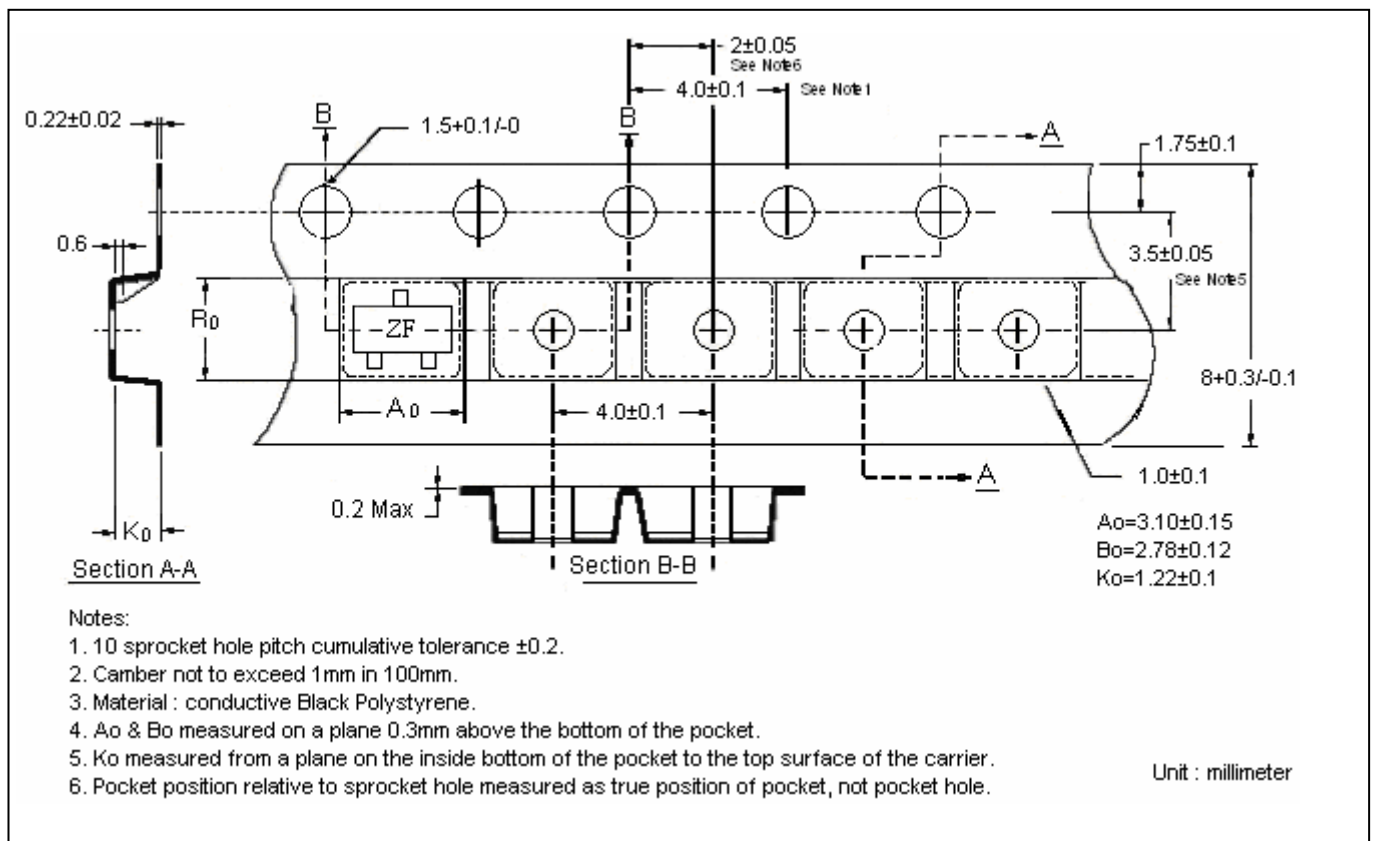
Typical Characteristics(Cont.)



Reel Dimension



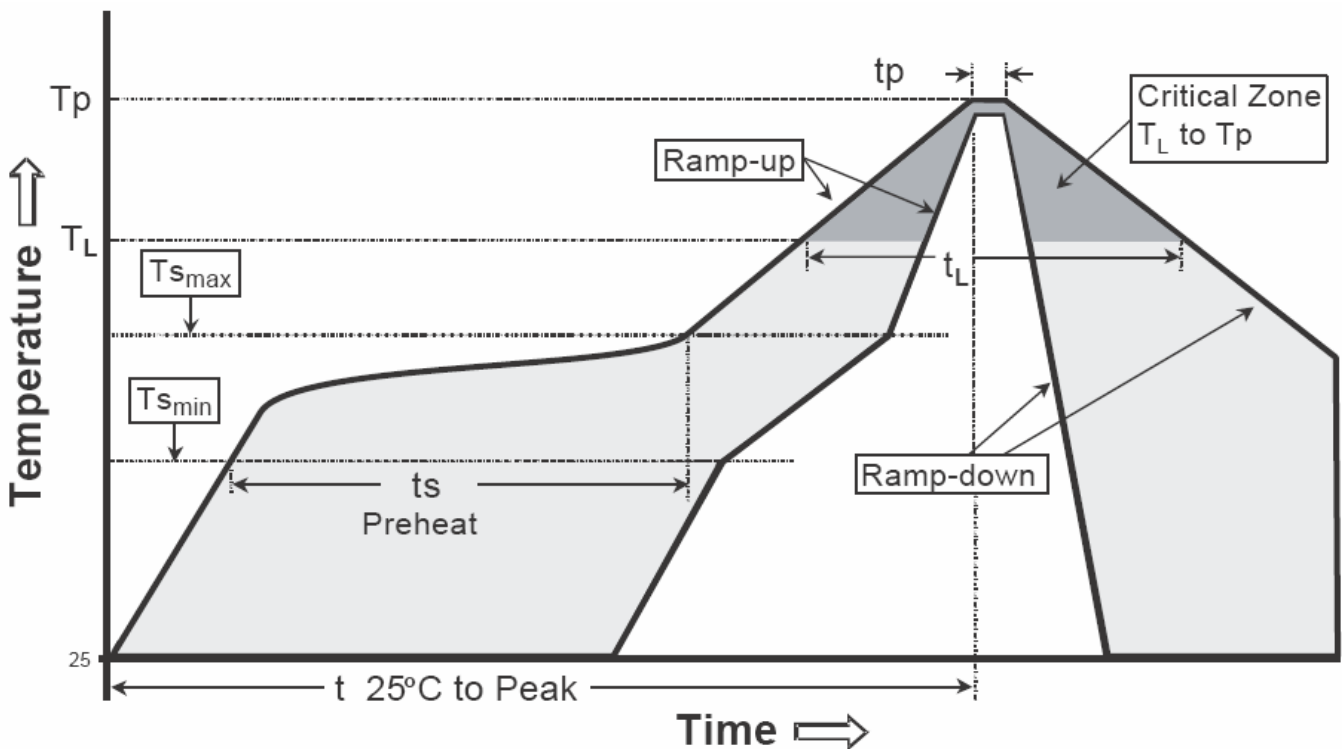
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

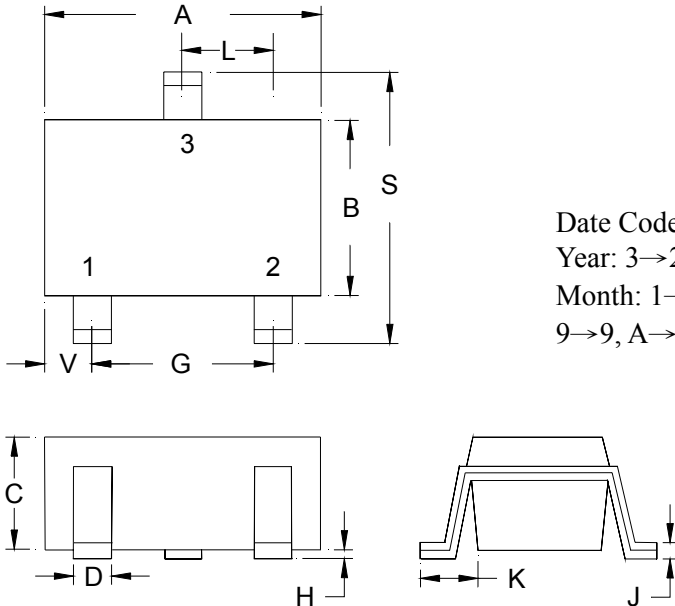
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

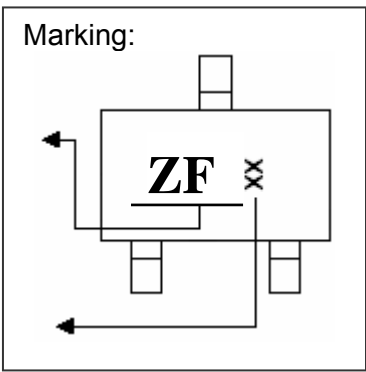
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-23 Dimension



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, and H; and a perspective view with dimensions K and J. The top view labels 1, 2, and 3 correspond to the base, emitter, and collector pins respectively.

Marking:



The marking diagram shows a top view of the package with 'ZF' and 'XX' markings. Arrows indicate the orientation of the package.

Product Code

Date Code: Year+Month
 Year: 3→2003, 4→2004
 Month: 1→1, 2→2, . . .
 9→9, A→10, B→11, C→12

3-Lead SOT-23 Plastic Surface Mounted Package
 CYStek Package Code: N3

Style : Pin 1.Base 2.Emitter 3.Collector

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0034	0.0070	0.085	0.177
B	0.0472	0.0630	1.20	1.60	K	0.0128	0.0266	0.32	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1161	2.10	2.95
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0005	0.0040	0.013	0.10					

- Notes:** 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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