AK5434D

Dual channel 14bit 30MHz A/D Converter with differential input

Features

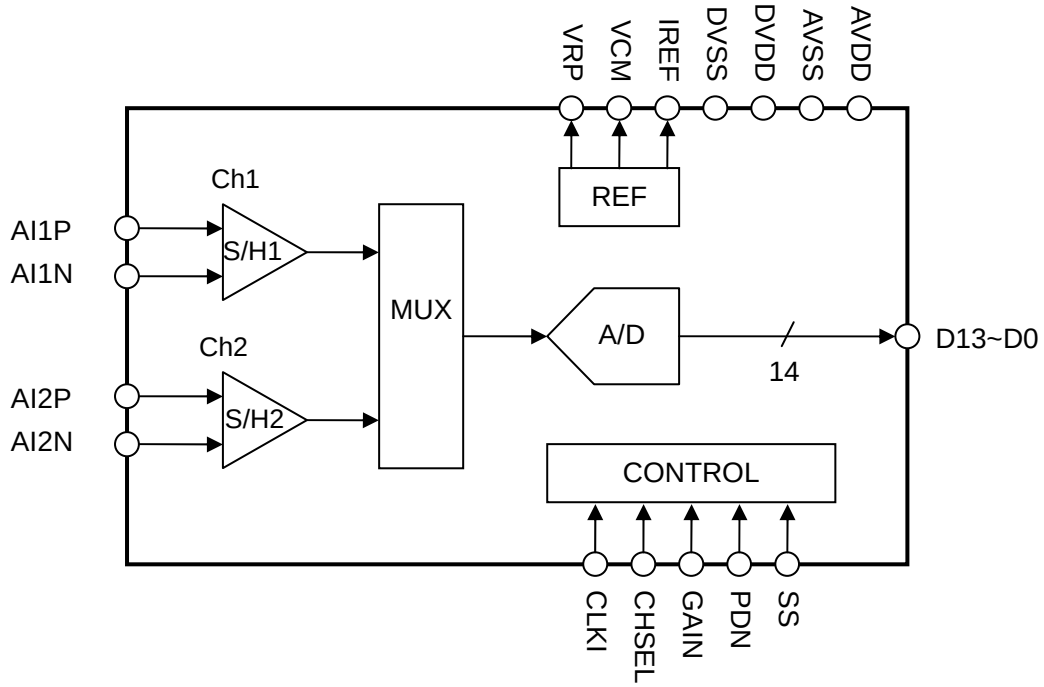
【Power Supply】 3.0V~3.45V Single-Supply

【Operation Temperature】 –40°C~+105°C

【Package】 30pinVSOP (Pin pitch 0.65mm)

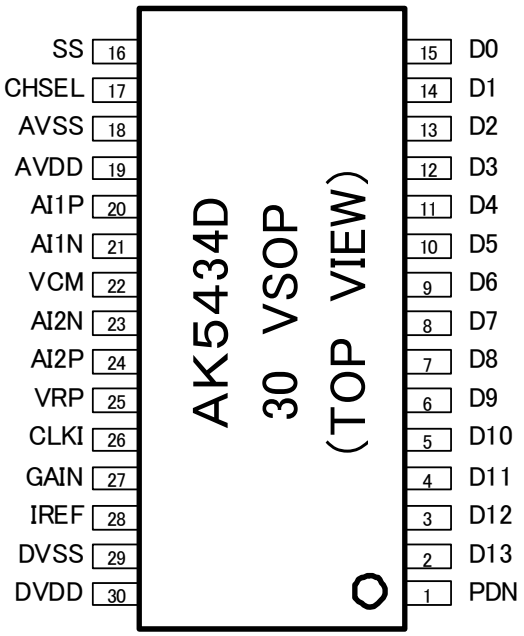
Input range：	4V (Differential input @ Gain 0dB)
Input signal bandwidth：	DC ~ 400MHz (typ.)
S/H Gain：	0dB/6dB/12dB
ADC：	14bit, 30MHz
S/(N+D)：	69dB (typ.)
	(30MHz operation, input signal frequency 14.9MHz@1ch)
Outputs：	14bit parallel data with straight binary
Power consumption：	172mW @typ. (power consumption @Power Down mode: under 1mW)

Circuit Block Diagram



Clock	Function
S/H1, S/H2	Sample/Hold AMP
MUX	Switch that selects input signal to A/D from S/H1 and S/H2
A/D	14bit 30MSPS A/D Converter
REF	Reference voltage generator
CONTROL	Operation control circuit

Pin Allocation



Pin Description

No.	Name	I/O	@Power down	Description
1	PDN	I	–	Power down（H: Normal Operation, L: Power down）
2	D13	O	High-Z	ADC output data MSB Straight binary code
3	D12	O	High-Z	ADC output data
4	D11	O	High-Z	ADC output data
5	D10	O	High-Z	ADC output data
6	D9	O	High-Z	ADC output data
7	D8	O	High-Z	ADC output data
8	D7	O	High-Z	ADC output data
9	D6	O	High-Z	ADC output data
10	D5	O	High-Z	ADC output data
11	D4	O	High-Z	ADC output data
12	D3	O	High-Z	ADC output data
13	D2	O	High-Z	ADC output data
14	D1	O	High-Z	ADC output data
15	D0	O	High-Z	ADC output data LSB
16	SS	I	–	Sampling timing setting L: Sampling timing is determined by applying Logic to CHSEL-pin. H: The sampling timing is the timing of CHSEL=L. Ch1 and Ch2 are sampled simultaneously.
17	CHSEL	I	–	Ch1/Ch2 select（L:Ch1, H:Ch2）
18	AVSS	PWR	–	Analog Ground
19	AVDD	PWR	–	Analog supply（3.0V～3.45V）
20	AI1P	I	–	Ch1 differential input P side
21	AI1N	I	–	Ch1 differential input N side
22	VCM	O	High-Z	Common-mode voltage output Connect 1μF between AVSS and this pin.
23	AI2N	I	–	Ch2 differential input N side
24	AI2P	I	–	Ch2 differential input P side
25	VRP	O	L	ADC Reference-voltage output. Connect 1μF between AVSS and this pin.
26	CLKI	I	–	ADC clock input
27	GAIN	I	–	S/H gain setting (L:0dB, M:12dB, H:6dB)
28	IREF	O	High-Z	bias current output Connect 8.2kΩ between AVSS and this pin.
29	DVSS	PWR	–	Digital Ground
30	DVDD	PWR	–	Digital Power Supply（3.0V~3.45V）

(NOTE)IO I: INPUT, O: OUTPUT, PWR: POWER/GROUND

Absolute Maximum Ratings

AVSS, DVSS=0V,All voltages are with respect to ground

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supplies Analog Digial	 AVDD DVDD	 −0.3 −0.3	 4.0 4.0	 V V	
Input Current	IIN	−10	10	mA	Except AVDD, AVSS, DVDD, DVSS pins
Analog Input Voltage Range (Note 1)	VINA	−0.3	AVDD+0.3	V	
Digital Input Voltage Range (Note 2)	VIND	−0.3	DVDD+0.3	V	
Operating Temperature	Ta	−40	105	°C	
Storage Temperature	Tstg	−65	150	°C	

(Note 1) AI1P, AI1N, AI2P, AI2N, GAIN, CLKI

(Note 2) CHSEL, SS, PDN

All power supply ground pins (AVSS, DVSS) should be at the same potential.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal Operating Specifications are not guaranteed at these extremes.

Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage Analog (Core) Digital (Core, IO)	 AVDD DVDD	 3.0 3.0	 3.3 3.3	 3.45 3.45	 V V	

Power supply voltages are values where each ground pin (AVSS=DVSS) is at 0V (Voltage reference)

All power supply ground pins (AVSS, DVSS) should be at the same potential.

Electrical Characteristics

■ Analog Specifications

(AVDD=DVDD=3.3V, S/H gain=0dB, Ta=25°C, CLKI=30MHz, fin=14.9MHz, Signal Level=3.4Vpp-diff)

Parameter	Symbol	Condition	min	Typ	Max	Units
DC Characteristics						
Resolution	RES				14	Bits
Integral Non-Linearity	INL			±2.8	±10.5	LSB
Differential Non-Linearity	DNL			±0.8	±4.0	LSB
Offset	EOC	AIxP=AIxN=VCM (x=1,2)			±100	LSB
Gain Error	GERR	Gain setting 0dB	-10	0	+10	%FS
Gain		Gain setting 6dB	5.5	6	6.5	dB
		Gain setting 12dB	11.5	12	12.5	dB
Input Range	AINFS	Gain setting 0dB	3.6	4.0	4.4	Vpp-diff
Common Voltage	VCM		1.26	1.4	1.54	V
ADC Reference Voltage	VRP		1.8	2.0	2.2	V
AC Characteristics						
S/N	SNR		68	73		dB
S/(N+D)	SND		64	69		dB
S/(N+D) (Note 1)	SND2	fin=1MHz	66	71		dB
SFDR	SFDR			70		dB
Total Harmonic Distortion	THD		64	70		dBc
Input Resistance (Note 1)	RIN	(Note 4)		60		kΩ
Input Capacitance (Note 1)	CIN			5	8	pF
Input Signal bandwidth (Note 1)	BW	-3dB Level		400		MHz
CMRR	CMR	fin=1MHz, common swing -26dB	50	56		dB
Crosstalk	CTK	fin=7.45MHz		–80	–70	dB
Current Consumption	IA ID IPD	Analog fin=1MHz Digital(Note 2) fin=1MHz		46 6	68 9 0.3	mA mA mA
Current Consumption in power down	IAS IDS	Analog Digital (Note 3)			0.1 0.1	mA mA

(Note 1) Design Value

(Note 2) CL=10pF are connected to D0~D13 pins.

(Note 3) Power down PDN=Low, CLKI=Low fix, Current consumption without no input signal.

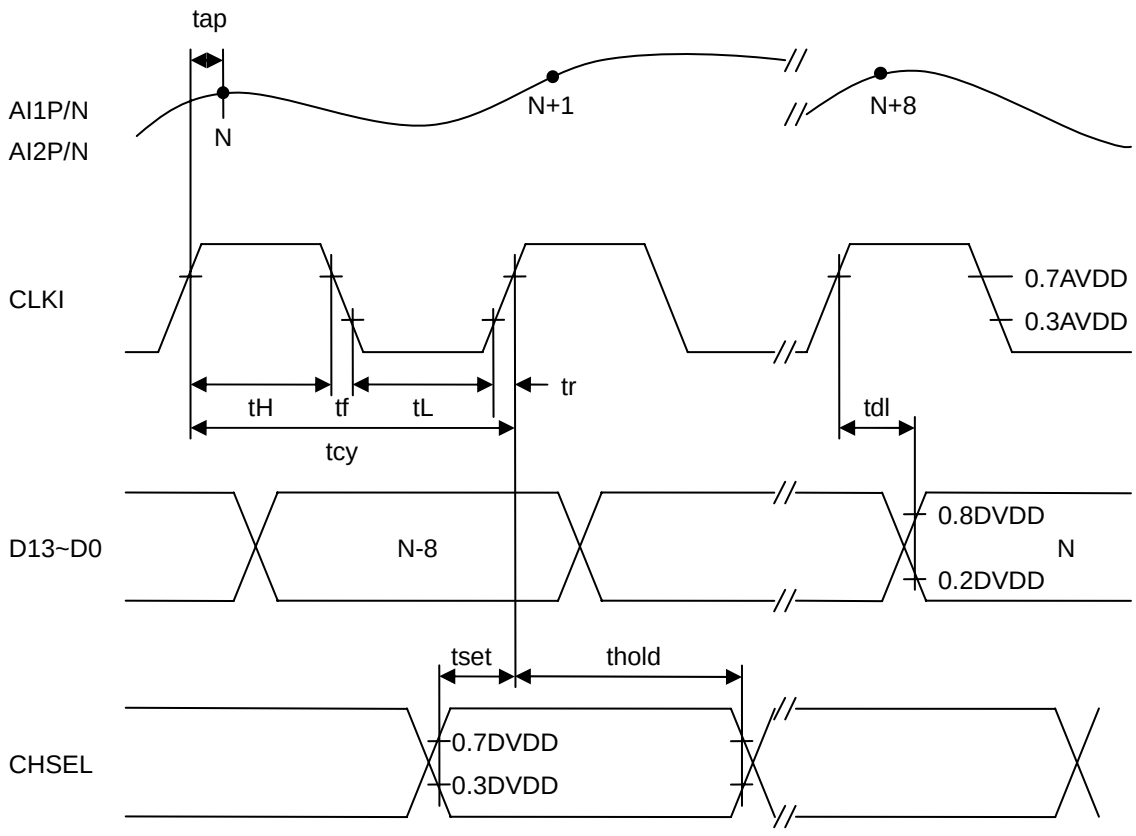
(Note 4) Equivalent resistance that from VCM operation middle point to differential input pins AI1P/N, AI2P/N. It is in inverse proportion to sampling frequency.

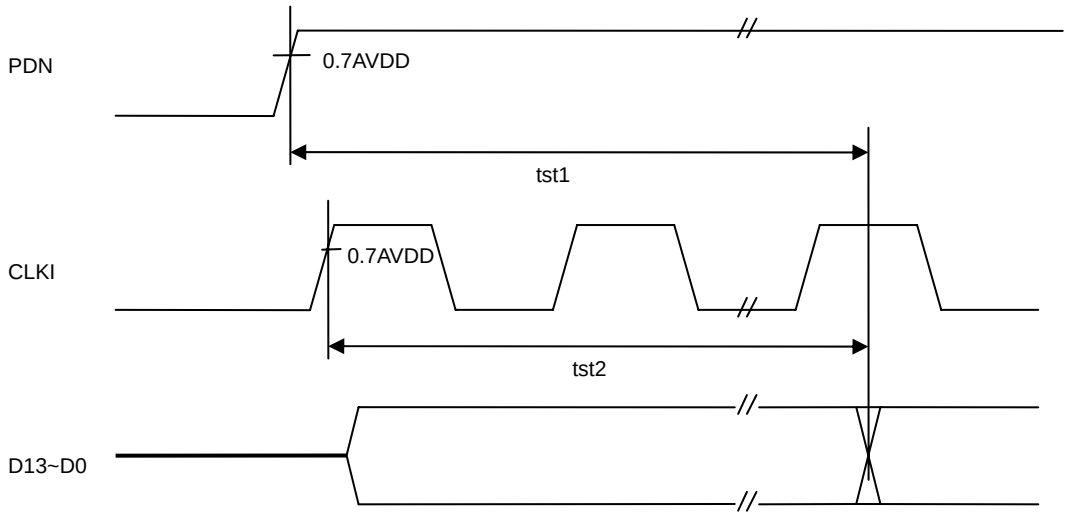
■ Switching Characteristics

(AVDD=DVDD=3.0~3.45V, Ta=–40~105°C, CL=10pF)

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Conversion rate	fs		15		30	MHz
Clock cycle	tcy		33.3		66.7	ns
Clock rise time Note 1	tr	0.3AVDD to 0.7AVDD		2	15	ns
Clock fall time Note 1	tf	0.7AVDD to 0.3AVDD		2	15	ns
Clock High width	tH		15			ns
Clock Low width	tL		15			ns
Clock duty	tduty		40	50	60	%
Pipeline delay Note 2	tpd			8		CLKI
Aperture delay Note 2	tap			2	4	ns
AD output delay	tdl		0	6	20	ns
CHSEL setup	tset		10			ns
CHSEL hold	thold		10			ns
Start up time 1	tst1			2	5	ms
Start up time 2	tst2			2	5	ms

Note 1) Clock high width and Low width must be fulfilled.
Note 2) Design Value





■ Digital DC Characteristics

(AVDD=DVDD=3.0~3.6V, Ta=－40~105°C)

Parameter	Symbol	Pin	Min.	Max.	Unit	Remark
High level input threshold 1	VIH1	Note 1	0.7×DVDD		V	
Low level input threshold 1	VIL1	Note 1		0.3×DVDD	V	
High level input threshold 2	VIH2	Note 2	0.7×AVDD		V	
Low level input threshold 2	VIL2	Note 2		0.3×AVDD	V	
High level input threshold 3	VIH3	GAIN	0.8×AVDD		V	
Middle level input threshold 3	VIM3	GAIN	0.3×AVDD	0.7×AVDD	V	
Low level input threshold 3	VIL3	GAIN		0.2×AVDD	V	
High level output voltage	VOH	Note 3, Note 4	0.8×DVDD		V	
Low level output voltage	VOL	Note 3, Note 5		0.2×DVDD	V	
Input leakage current	ILKG	Note 1, Note2, GAIN		±10	μA	
High-Z leakage current	IOZ	Note 3		±10	μA	

Note 1) CHSEL, SS, PDN,

Note 2) CLKI

Note 3) D13~D0

Note 4) IOH = –1mA

Note 5) IOL = 1mA

Functional Description

Power down function

Power Down mode can be activated by applying a logic Level “0” to the PDN-pin. All the data output pins [D13: D0] become Low state.at Power Down mode.

PDN	Condition
L	Power down
H	Normal opration

S/H AMP gain select

The gain of the S/H amplifier can be selected by the input level of GAIN-pin.

GAIN	Gain	Input full scale
AVSS	0dB	4Vpp-diff
AVDD	6dB	2Vpp-diff
VCM	12dB	1Vpp-diff

Sampling timing setting

The sampling timing of two channels can be set with SS-pin.

SS	Sampling timing
L	S/H1 or S/H2 samples the signal according to CHSEL.
H	At CHSEL=L, S/H1 and S/H2 sample the signal at the same time.

Sampling channel select

The samples timing can be selected with CHSEL-pin.

Separate sampling (@SS=Low)

CHSEL	Sampling channel
L	S/H1
H	S/H2

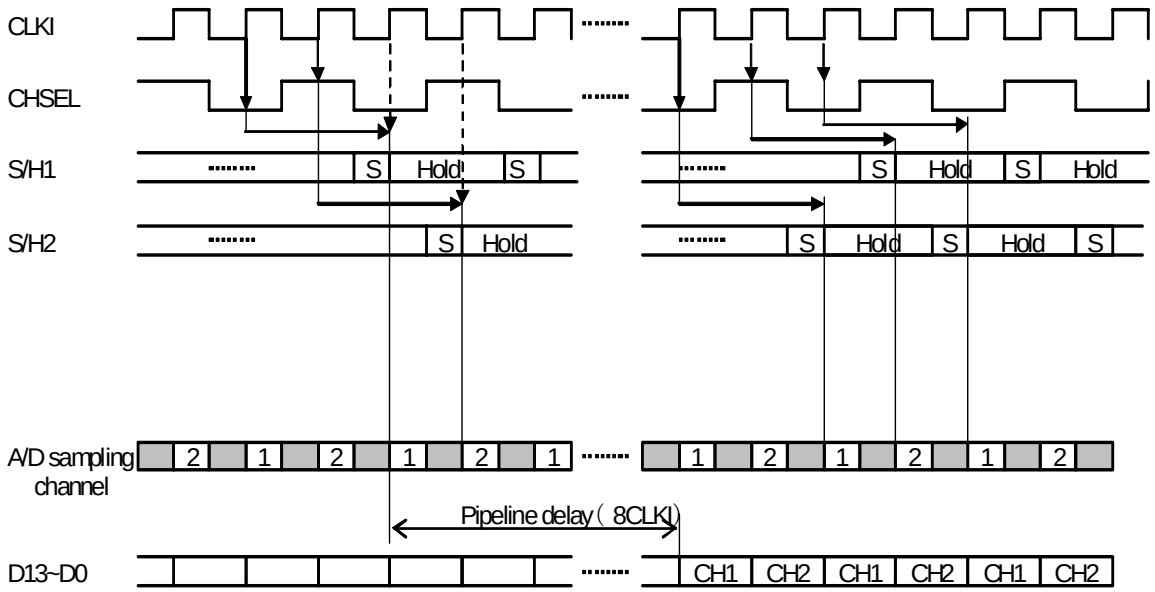
Simultaneous sampling (@SS=High)

CHSEL	Sampling channel
L	S/H1 & S/H2
H	Not sampled

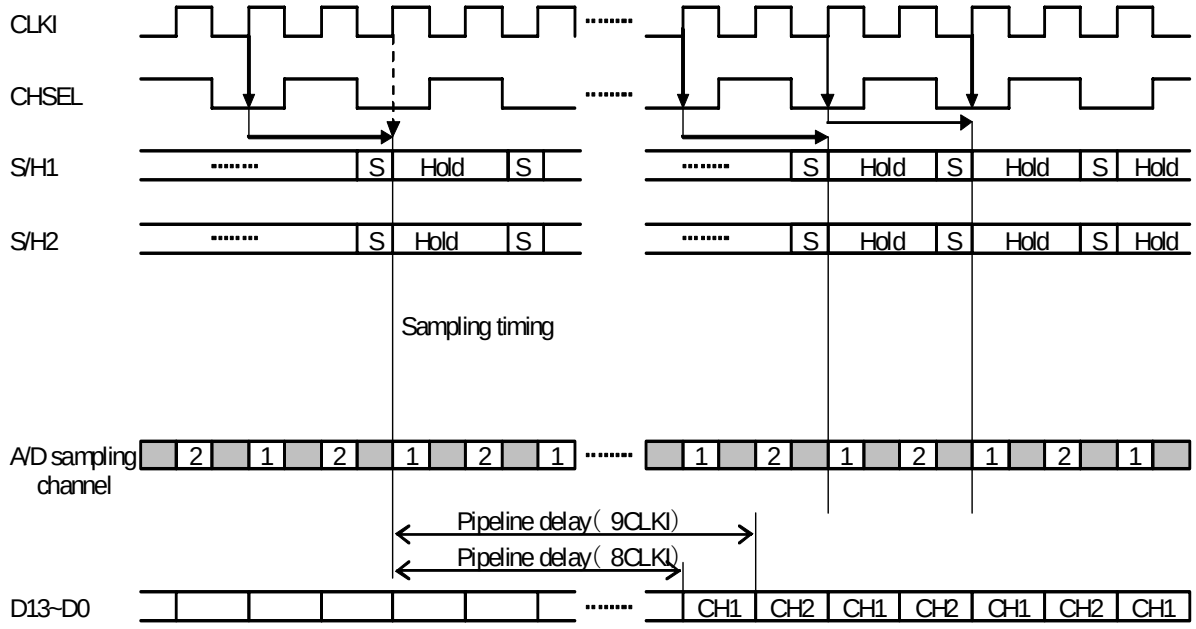
Only at CHSEL=Low, sampling is done at the same timing (SS=High).

■ Operation timing

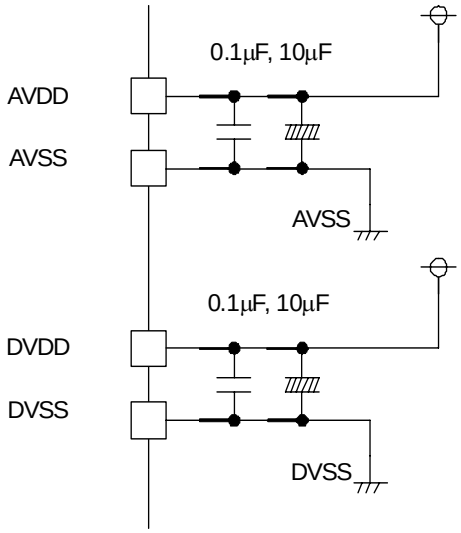
At SS="L"

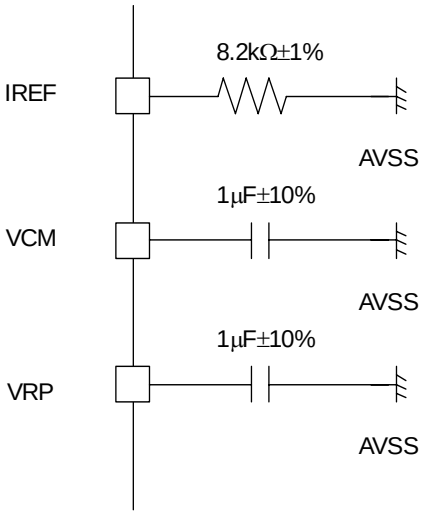


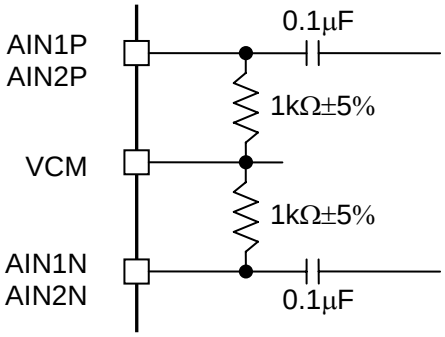
At SS="H"



External Circuit Examples

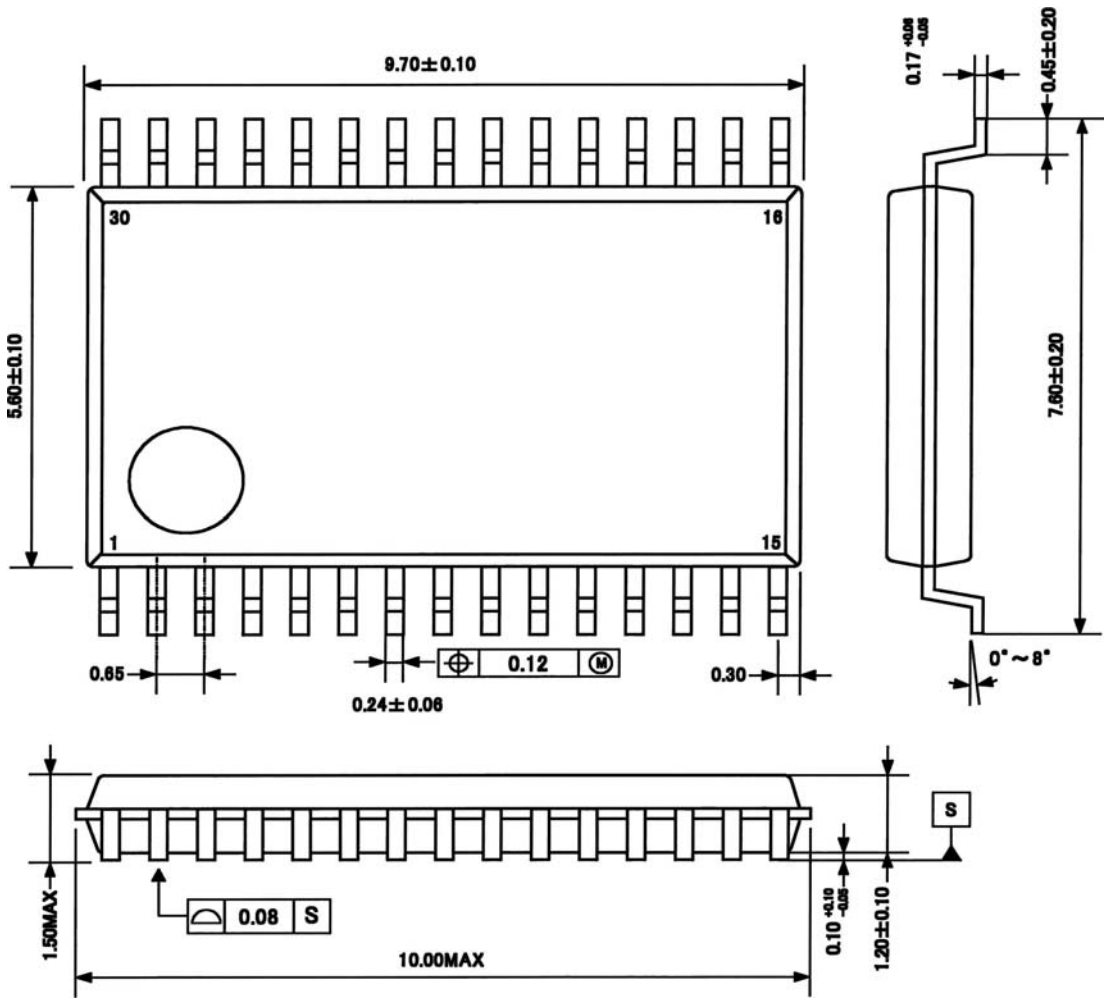






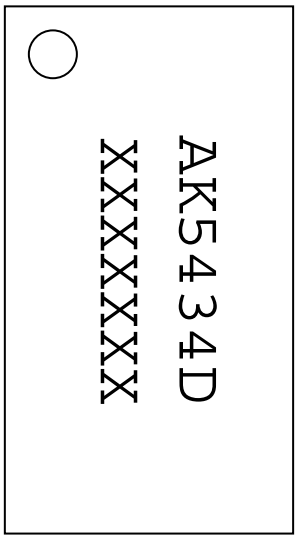
Note) Resisters must be metal-film type.

Packages



30-VSOP-0.65

Marking



Marketing Code: AK5434D
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