

μPA2815T1S

P-channel MOSFET

-30 V, -21 A, 11 mΩ

R07DS0777EJ0101 Rev.1.01 May 28, 2013

Description

The μ PA2815T1S is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- $V_{DSS} = -30 \text{ V } (T_A = 25^{\circ}\text{C})$
- Low on-state resistance
 - $R_{DS(on)} = 11 \text{ m}\Omega \text{ MAX.} (V_{GS} = -10 \text{ V}, I_D = -21 \text{ A})$
- 4.5 V Gate-drive available
- Small & thin type surface mount package with heat spreader
- Pb-free and Halogen free



HWSON-8

Ordering Information

Part No.	Lead Plating	Packing	Package
μPA2815T1S-E2-AT *1	Pure Sn	Tape 5000 p/reel	HWSON-8
			typ. 0.022 g

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V_{DSS}	-30	V
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	∓21	Α
Drain Current (pulse) *1	I _{D(pulse)}	∓84	Α
Total Power Dissipation *2	P _{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P _{T2}	3.8	W
Total Power Dissipation (T _C = 25°C)	P _{T3}	14.5	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	−55 to +150	°C
Single Avalanche Current *3	I _{AS}	19	Α
Single Avalanche Energy *3	E _{AS}	36.1	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2 $R_{th(ch-A)}$ 83.3 °C/W Channel to Case (Drain) Thermal Resistance $R_{th(ch-C)}$ 8.6 °C/W

Notes: *1. PW \leq 10 μ s, Duty Cycle \leq 1%

*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

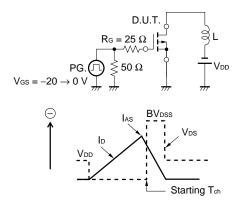
*3. Starting T_{ch} = 25°C, V_{DD} = -15 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C)

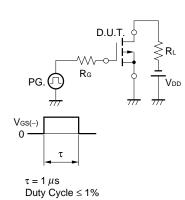
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			-1	μΑ	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			∓100	nA	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate Cut-off Voltage	$V_{GS(off)}$	-1.0		-2.5	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Forward Transfer Admittance *1	y _{fs}	15			S	$V_{DS} = -5 \text{ V}, I_{D} = -10.5 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		9	11	mΩ	$V_{GS} = -10 \text{ V}, I_D = -21 \text{ A}$
Resistance *1	R _{DS(on)2}		16	23	mΩ	$V_{GS} = -4.5 \text{ V}, I_D = -10.5 \text{ A}$
Input Capacitance	C _{iss}		1760		pF	$V_{DS} = -10 \text{ V},$
Output Capacitance	Coss		850		pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		750		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		13		ns	$V_{DD} = -15 \text{ V}, I_D = -10.5 \text{ A},$
Rise Time	t _r		40		ns	$V_{GS} = -10 \text{ V},$
Turn-off Delay Time	t _{d(off)}		88		ns	$R_G = 10 \Omega$
Fall Time	t _f		171		ns	
Total Gate Charge	Q_{G}		47		nC	$V_{DD} = -24 \text{ V},$
Gate to Source Charge	Q_{GS}		4.2		nC	$V_{GS} = -10 \text{ V},$
Gate to Drain Charge	Q_{GD}		24		nC	I _D = -21 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9		V	I _F = 21 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		166		ns	$I_F = 21 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		222		nC	di/dt = 100 A/μs

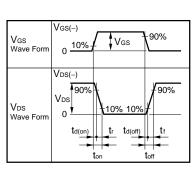
Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME





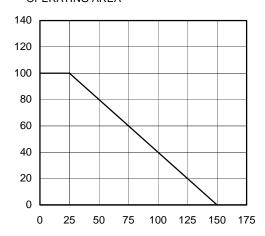
TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. \\ \hline \\ IG = -2 \text{ mA} \\ \hline \\ PG. \\ \hline \\ \end{array}$$

dT - Percentage of Rated Power - %

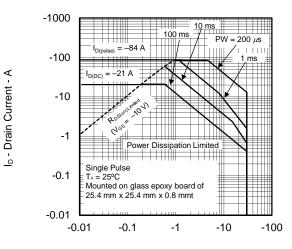
Typical Characteristics ($T_A = 25$ °C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



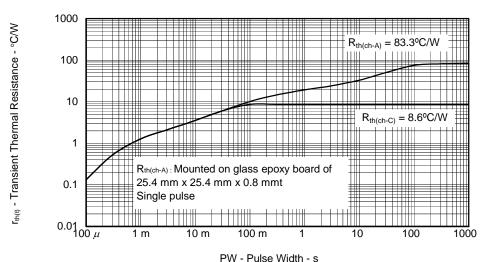
T_A - Ambient Temperature - °C

FORWARD BIAS SAFE OPERATING AREA

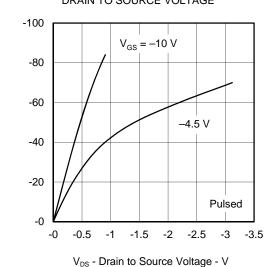


V_{DS} - Drain to Source Voltage - V

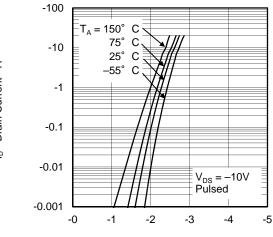
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



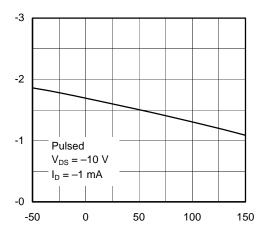
 V_{GS} - Gate to Source Voltage - V



I_D - Drain Current - A

 $V_{\text{GS}(\text{off})}$ – Gate to Source Cut-off Voltage - V

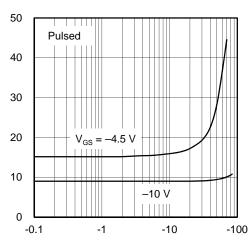
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



 T_{ch} - Channel Temperature - $^{\circ}C$

$R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

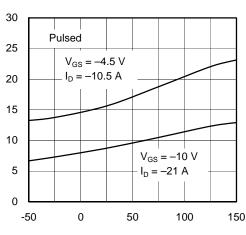
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



ID - Drain Current - A

$R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

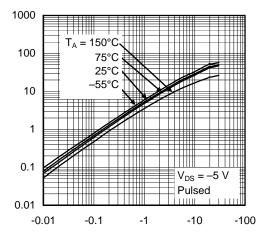


T_{ch} - Channel Temperature - °C

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

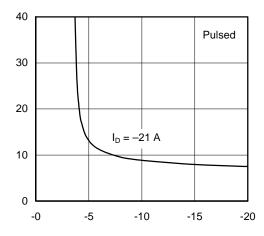


 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - m Ω



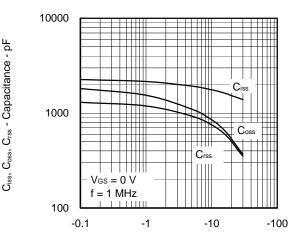
ID - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



V_{GS} - Gate to Source Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS

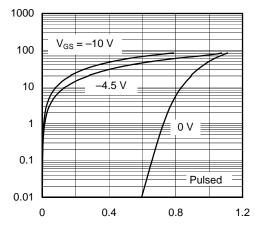
-12 -30 $V_{\text{GS}} \\$ $V_{\text{DS}} \\$ V_{DS} - Drain to Source Voltage - V $y_{DD} = -24 \text{ V}$ -10 -20 -8 -6 -10 -2 $I_D = -21 A$ -0 -0 50 0 10 20 30 40

 $\ensuremath{\mathsf{Q}}_{\ensuremath{\mathsf{G}}}$ - Gate Charge - nC

V_{GS} - Gate to Source Voltage - V

I_F - Diode Forward Current - A

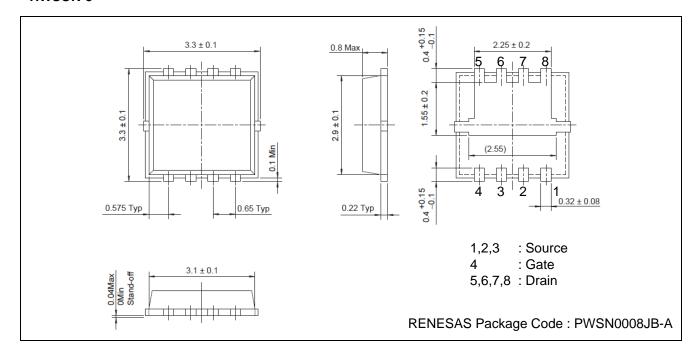
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



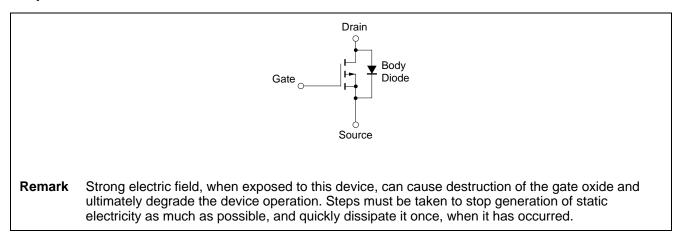
 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

Package Drawings (Unit: mm)

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Equivalent Circuit



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