

MN4052B/MN4052BS

Dual 4-Channel Analog Multiplexer

Outline

The MN4052B/S is a multiplexer which can select and multiplex dual 4-channel analog signals and digital signals. The corresponding switch of each channel is turned "ON" by the control signal of the enable input ($\bar{E}$). It can switch a signal of large amplitude ($V_{DD}-V_{EE} \leq 15V$) even if the logical amplitude ($V_{DD}-V_{SS}$) of the control signal is small.

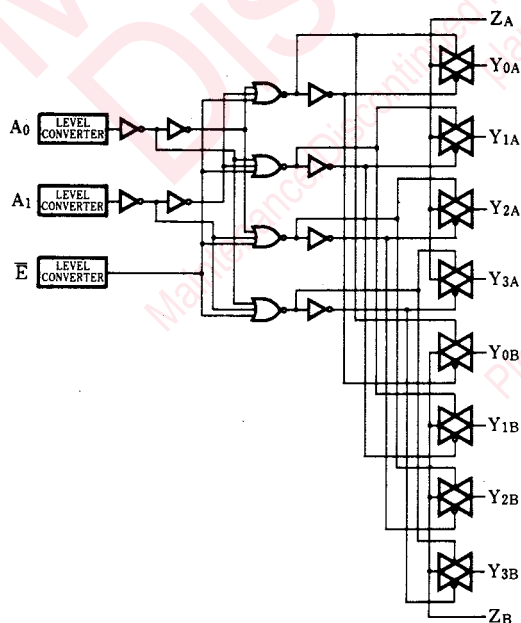
It is also connectable with a low impedance circuit since the ON resistance of each switch is low. This dual 4-channel analog multiplexer is equivalent to Motorola's MC14052B and RCA's CD4052B.

Truth Table

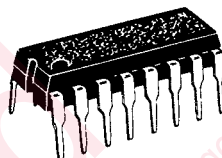
Input			Channel ON
$\bar{E}$	A_1	A_0	
L	L	L	$Y_{0A}-Z_A; Y_{0B}-Z_B$
L	L	H	$Y_{1A}-Z_A; Y_{1B}-Z_B$
L	H	L	$Y_{2A}-Z_A; Y_{2B}-Z_B$
L	H	H	$Y_{3A}-Z_A; Y_{3B}-Z_B$
H	x	x	None

Note) x: don't care

Logic Diagram

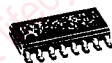


P-3



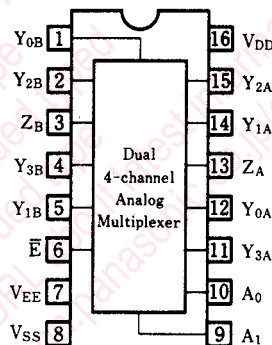
16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

Pin Configuration



Pin description

$Y_{0A} \sim Y_{3A}$: Analog input output
 $Y_{0B} \sim Y_{3B}$: Analog input output
 A_0, A_1 : Address input
 $\bar{E}$: Enable input
 Z_A, Z_B : Common input output

■ Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

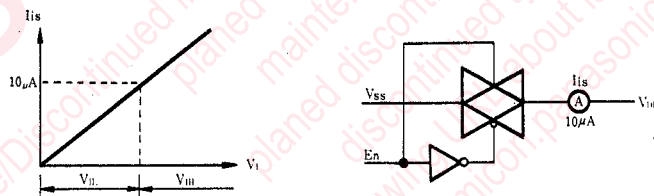
Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	$-0.5 \sim +18$	V
Input voltage	V_I	$-0.5 \sim V_{DD} + 0.5^*$	V
Output pin voltage	V_O	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak input · output pin current	$\pm I_I$	max. 10	mA
Power dissipation (per package)	P_D	max. 400	mW
		Decrease to 200mW at the rate of $8\text{mW}/^\circ\text{C}$	
Power dissipation (per output pin)	P_D	max. 100	mW
Operating ambient temperature	T_{opr}	$-40 \sim +85$	$^\circ\text{C}$
Storage temperature	T_{slg}	$-65 \sim +150$	$^\circ\text{C}$

* $V_{DD} + 0.5\text{V}$ should be lower than 18V.

■ DC Characteristics ($V_{SS}=0\text{V}$)

Item	V_{DD} (V)	Symbol	Condition	$T_a = -40^\circ\text{C}$		$T_a = 25^\circ\text{C}$		$T_a = 85^\circ\text{C}$		Unit
				min.	max.	min.	max.	min.	max.	
Static supply current	5	I_{DD}	$V_I = V_{SS}$ or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Input voltage low level (Fig. 1)	5	V_{IL}	$I_{is} = 10\mu\text{A}$	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input voltage high level (Fig. 1)	5	V_{IH}	$I_{is} = 10\mu\text{A}$	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Input leakage current	15	$\pm I_I$	$V_I = 0\text{V}$ or 15V	—	0.3	—	0.3	—	1	μA
I/O ON leakage current	15	$\pm I_{ON}$	$V_I = 0\text{V}$ or 15V , $V_O = \text{Open}$	—	—	—	300	—	2000	nA
I/O OFF leakage current	15	$\pm I_{OFF}$	$V_I = 0\text{V}$ or 15V , $V_O = 0\text{V}$ or 15V	—	—	—	1000	—	3000	nA

Note) In case that current flows into Y pin, when voltage drop between Y-Z becomes more than 0.4V, current flows into Z pin from V_{DD} . When current flows to Z pin, there is no limit of voltage drop.

Fig. 1 Standard of V_{IL} , V_{IH} ■ DC Characteristics ($T_a=25^\circ\text{C}$, $V_{SS}=0\text{V}$)

Item	$V_{DD}-V_{EE}$ (V)	Symbol	Condition	min.	typ.	max.	Unit
ON resistance	5	R_{ON}	$V_I = 5\text{V}$	—	200	800	Ω
			$V_I = 2.5\text{V}$	—	550	1300	
			$V_I = 0.25\text{V}$	—	200	800	
ON resistance	10	R_{ON}	$V_I = 10\text{V}$	—	80	300	Ω
			$V_I = 5\text{V}$	—	100	350	
			$V_I = 0.25\text{V}$	—	80	300	
ON resistance	15	R_{ON}	$V_I = 15\text{V}$	—	60	200	Ω
			$V_I = 7.5\text{V}$	—	80	250	
			$V_I = 0.25\text{V}$	—	60	200	

■ Switching Characteristics (Ta=25°C, V_{SS}=0V)

Item	V _{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Propagation time (Fig. 1) Vis→Vos (H→L)	5	t _{PHL}	R _L =10kΩ C _L =50pF E=V _{SS}	—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation time (Fig. 1) Vis→Vos (L→H)	5	t _{PLH}	R _L =10kΩ C _L =50pF E=V _{SS}	—	10	30	ns
	10			—	5	15	
	15			—	5	15	
Propagation time (Fig. 1) An→Vos (H→L)	5	t _{PHL}	R _L =10kΩ C _L =50pF E=V _{SS}	—	150	450	ns
	10			—	65	195	
	15			—	50	150	
Propagation time (Fig. 1) An→Vos (L→H)	5	t _{PLH}	R _L =10kΩ C _L =50pF E=V _{SS}	—	75	225	ns
	10			—	35	105	
	15			—	30	90	
Output disable time (Fig. 1) E→Vos (H)	5	t _{PHZ}	R _L =10kΩ C _L =50pF E=V _{DD}	—	100	300	ns
	10			—	90	270	
	15			—	90	270	
Output disable time (Fig. 1) E→Vos (L)	5	t _{PLZ}	R _L =10kΩ C _L =50pF E=V _{DD}	—	95	285	ns
	10			—	90	270	
	15			—	90	270	
Output enable time (Fig. 1) E→Vos (H)	5	t _{PZH}	R _L =10kΩ C _L =50pF E=V _{DD}	—	130	390	ns
	10			—	55	165	
	15			—	45	135	
Output enable time (Fig. 1) E→Vos (L)	5	t _{PZL}	R _L =10kΩ C _L =50pF E=V _{DD}	—	120	360	ns
	10			—	50	150	
	15			—	35	105	
Sine wave transfer distortion rate (Fig. 2)	5		R _L =10kΩ, C _L =15pF fis=1kHz, Vis=½ V _{DD(P-P)}	—	0.25	—	%
	10			—	0.04	—	
	15			—	0.04	—	
Crosstalk (Fig. 3) (between 2 channel)	5		R _L =1kΩ Vis=½ V _{DD(P-P)}	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Crosstalk (Fig. 1) (Address Input→Output)	5		R _L =10kΩ, C _L =15pF E or An=V _{DD}	—	—	—	mV
	10			—	50	—	
	15			—	—	—	
Feedthrough (Fig. 2) (Note 1) (OFF state)	5		R _L =1kΩ, C _L =5pF Vis=½ V _{DD(P-P)}	—	—	—	MHz
	10			—	1	—	
	15			—	—	—	
Transfer frequency (Fig. 2) (Note 2)	5		R _L =1kΩ, C _L =5pF Vis=½ V _{DD(P-P)}	—	13	—	MHz
	10			—	40	—	
	15			—	70	—	
Input capacitance		C _I		—	—	7.5	pF

Fig. 1 Propagation delay time, output disable/enable time, crosstalk test circuit

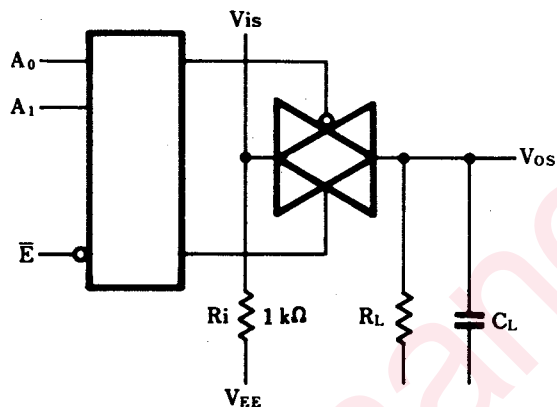
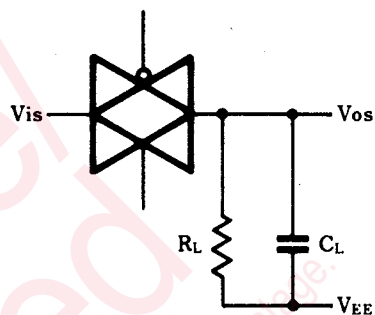


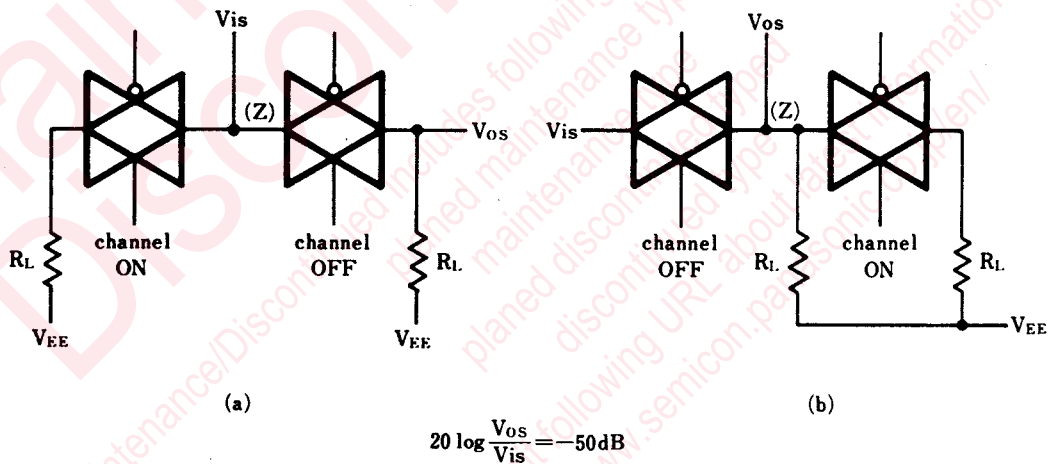
Fig. 2 Sine wave distortion, feedthrough, frequency response, test circuit



Note 1) $20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB}$

Note 2) $20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB}$

Fig. 3 Crosstalk test circuit



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