AmPAL*16XX Family

20-Pin IMOX™ Programmable Array Logic (PAL) Elements

DISTINCTIVE CHARACTERISTICS

- AMD's superior IMOX technology
  - Guarantees t_{PD} = 15 ns Max. "B" Versions
- High-Speed, Half-Power ("AL") and Quarter-Power ("Q") versions
- Platinum-silicide fuses and added test words ensure programming yields > 98%
- Post Programming Functional Yields (PPFY) of 99.9%
- PRELOAD feature permits full logical verification
- Reliability assured through more than 70 billion fuse hours of life testing with no failures
- Full AC and DC parametric testing at the factory through on-board testing circuitry
- AMD's industry-leading quality guarantees

GENERAL DESCRIPTION

AMD PAL devices are high-speed, electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to fit most applications precisely. Typically they are a replacement for low-power Schottky SSI/MSI logic circuits, reducing chip count by more than 5 to 1 and greatly simplifying prototyping and board layout.

Seven different devices are available, including both registered and combinatorial devices, in six different speed and power versions. The very High-Speed "B" versions (t_{PD} = 15 ns) run approximately 40% faster than the High-Speed "A" versions (t_{PD} = 25 ns). High-Speed, Half-Power "AL" versions (t_{PD} = 25 ns, I_{CC} = 90 mA) are available, as well as Standard-Speed, Half-Power "L" versions (t_{PD} = 35 ns, I_{CC}* = 80 mA). Quarter-Power "Q" versions (t_{PD} = 35 ns, I_{CC} = 45 mA) are also available.

Please see the following pages for Block Diagrams.

*Combinatorial functions

PRODUCT SELECTOR GUIDE

AMD PAL Speed/Power Families

Family	t_{PD} ns (Max.)		t_S (1) ns (Min.)		t_{CO} (1) ns (Max.)		I_{CC} (2) mA (Max.)	I_{OL} mA (Min.)	
	C Devices	M Devices	C Devices	M Devices	C Devices	M Devices	C/M Devices	C Devices	M Devices
Very High-Speed ("B") Versions	15	20	13	18	12	15	180	24	12
High-Speed ("A") Versions	25	30	20	25	15	20	155 (2)	24	12
High-Speed, Half-Power ("AL") Versions	25	30	20	25	15	20	90	24	12
Standard Versions	35	40	30	35	25	25	155 (2)	24	12
Half-Power ("L") Versions	35	40	30	35	25	25	80 (2)	24	12
Quarter-Power ("Q") Versions	35	40	30	35	25	25	45	12	8

(1) Sequential functions
(2) Combinatorial functions

AMD PAL FUNCTIONS

Part Number	Array Inputs	Logic	Output Enable	Outputs	Package Pins
16R8	Eight Dedicated, Eight Feedback	Eight 8-Wide AND-OR	Dedicated	Registered Inverting	20
16R6	Eight Dedicated, Six Feedback, Two Bidirectional	Six 8-Wide AND-OR	Dedicated	Registered Inverting	20
		Two 7-Wide AND-OR-INVERT	Programmable	Bidirectional	
16R4	Eight Dedicated, Four Feedback, Four Bidirectional	Four 8-wide AND-OR	Dedicated	Registered Inverting	20
		Four 7-Wide AND-OR-INVERT	Programmable	Bidirectional	
16L8	Ten Dedicated, Six Bidirectional	Eight 7-Wide AND-OR-INVERT	Programmable	Six Bidirectional Two Dedicated	20
16H8	Ten Dedicated, Six Bidirectional	Eight 7-Wide AND-OR	Programmable	Six Bidirectional Two Dedicated	20
16LD8	Ten Dedicated, Six Bidirectional	Eight 8-Wide AND-OR-INVERT	–	Dedicated	20
16HD8	Ten Dedicated, Six Bidirectional	Eight 8-Wide AND-OR	–	Dedicated	20

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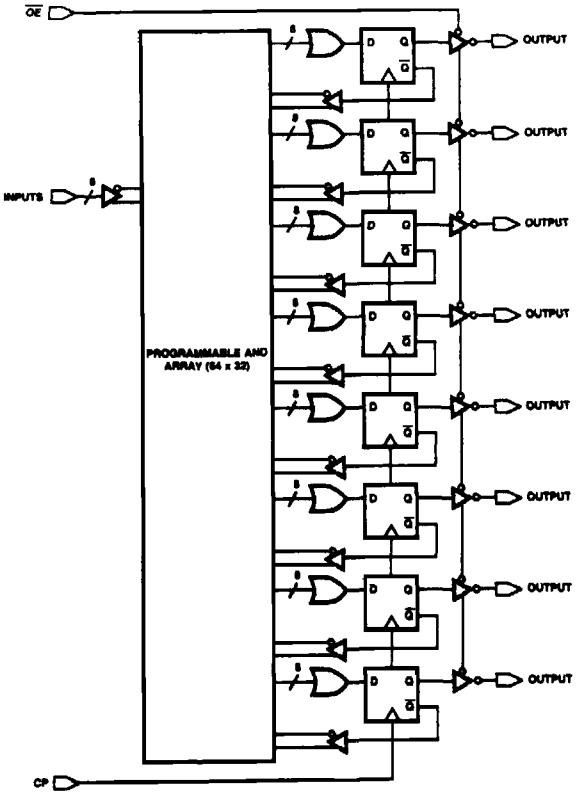
BLOCK DIAGRAMS

AmPAL16R8



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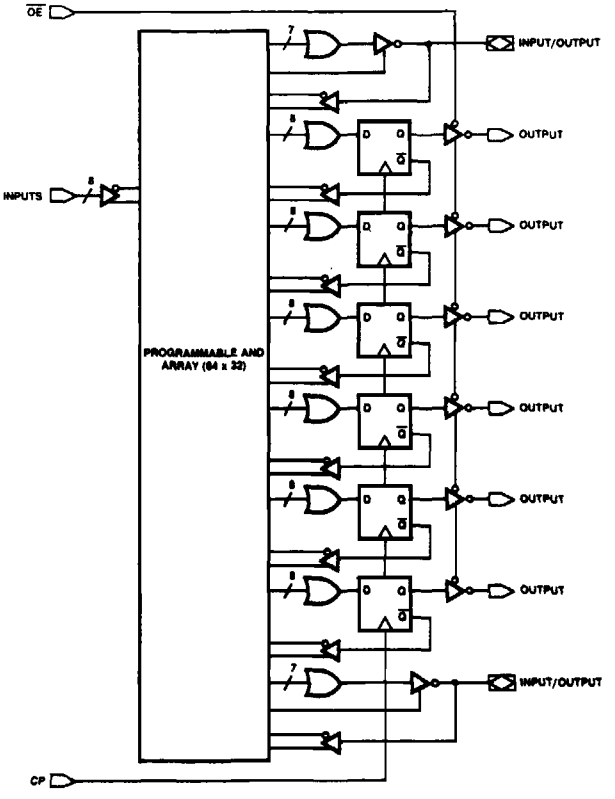
AmPAL16R6



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BLOCK DIAGRAMS (Cont'd.)

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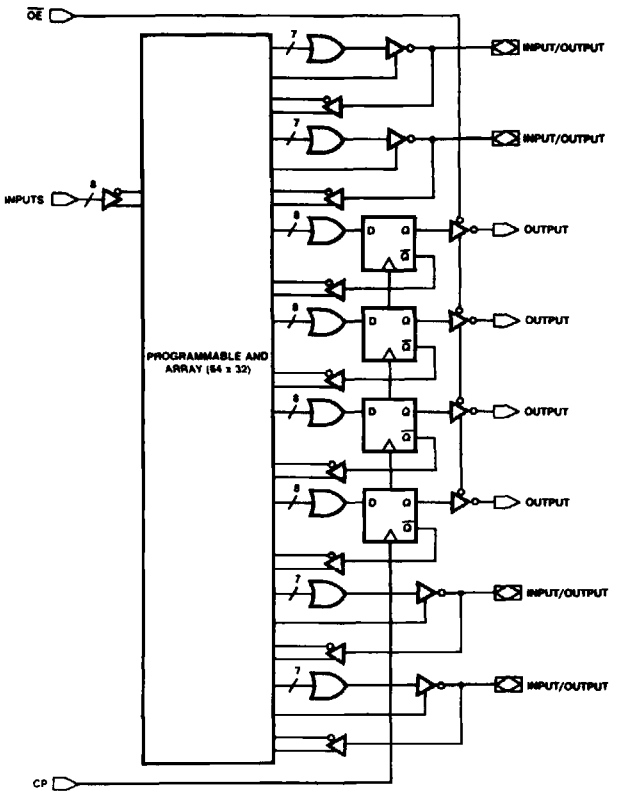

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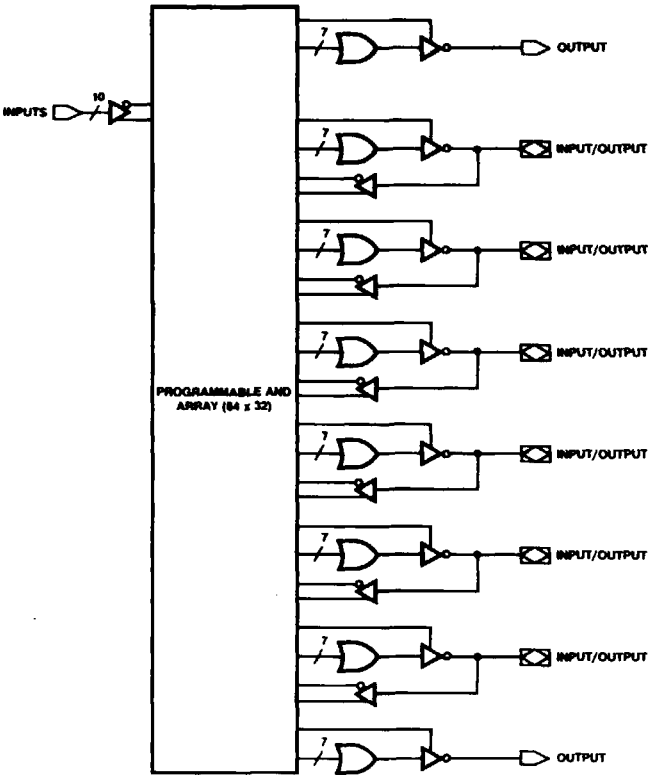
AmPAL16L8



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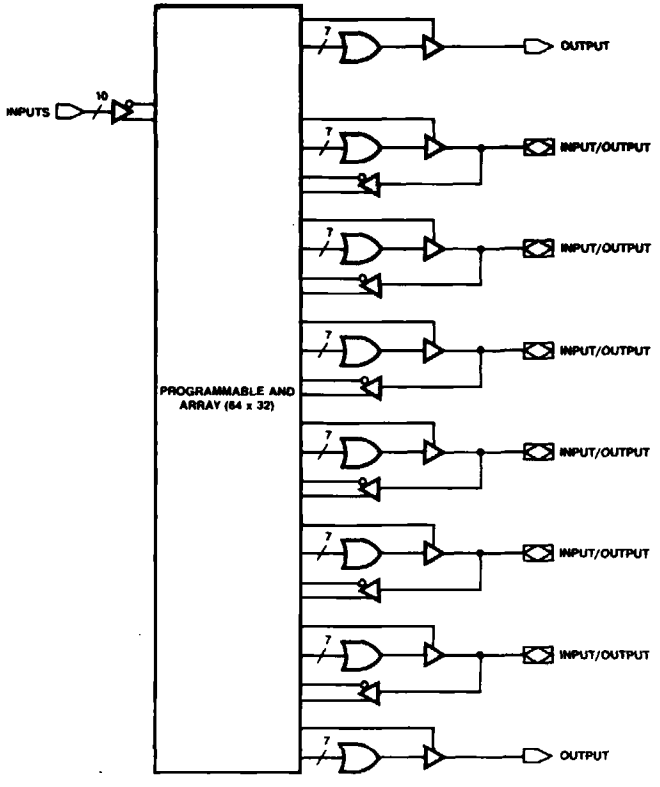
BLOCK DIAGRAMS (Cont'd.)

AmPAL16H8



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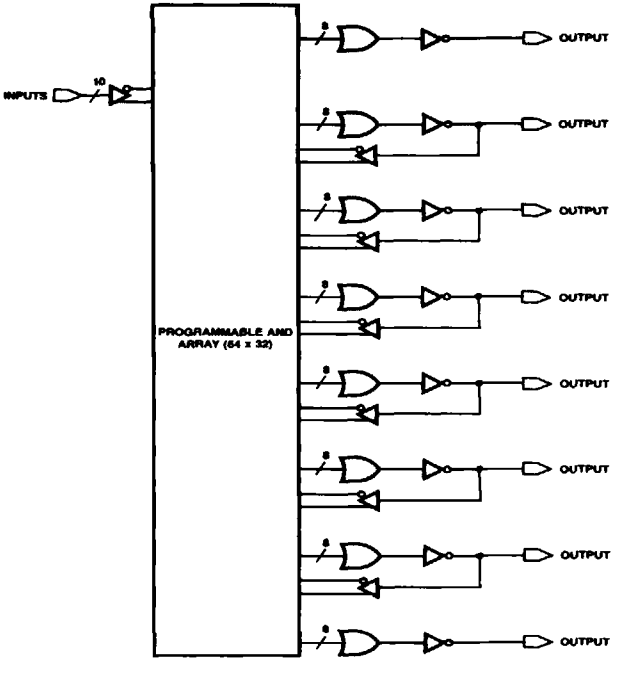
AmPAL16LD8



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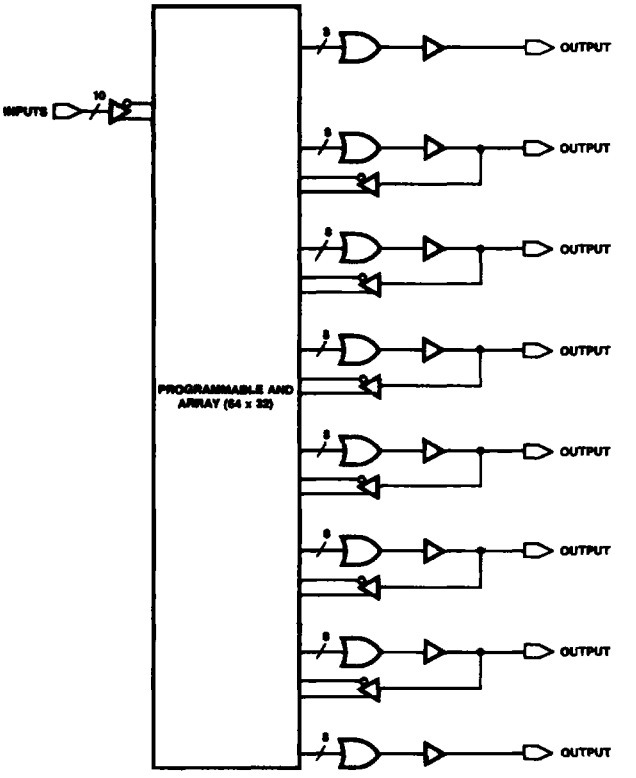
BLOCK DIAGRAMS (Cont'd.)

AmPAL16HD8



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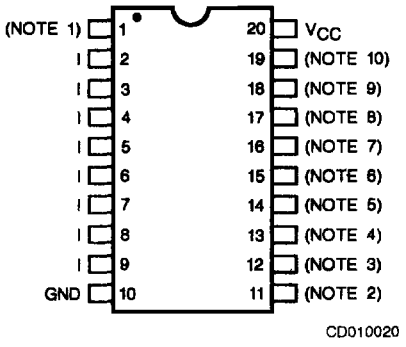
CONNECTION DIAGRAMS
Top View

DIPs*



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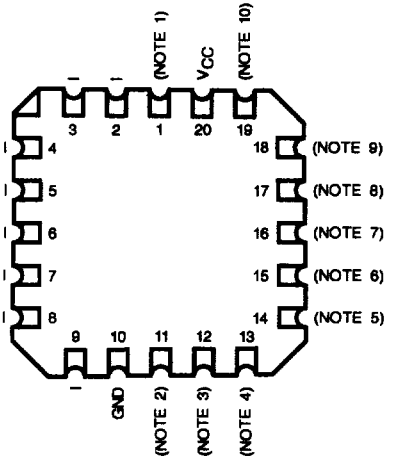
LCC**



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Note: Pin 1 is marked for orientation.

Notes:

	16L8	16R8	16R6	16R4	16H8	16HD8	16LD8
1	I	CLK	CLK	CLK	I	I	I
2	I	OE	OE	OE	I	I	I
3	O	O	I/O	I/O	O	O	O
4	I/O	O	O	I/O	I/O	O	O
5	I/O	O	O	O	I/O	O	O
6	I/O	O	O	O	I/O	O	O
7	I/O	O	O	O	I/O	O	O
8	I/O	O	O	O	I/O	O	O
9	I/O	O	O	I/O	I/O	O	O
10	O	O	I/O	I/O	O	O	O

*Also available in 20-Pin Ceramic Flatpack. Pinouts identical to DIPs.
**Also available in 20-Pin Plastic Leaded Chip Carrier. Pinouts identical to LCC.

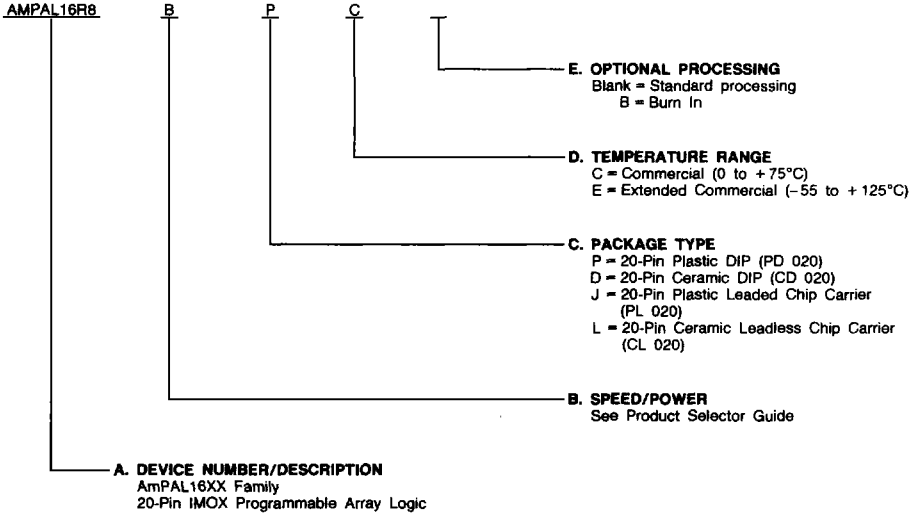
PIN DESIGNATIONS

I = Input
I/O = Input/Output
O = Output
V_{CC} = Supply Voltage
GND = Ground
CLK = Clock
OE = Output Enable

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AMPAL16R8/B/A/AL/L/Q	PC, DC, DCB, DE, JC, LC, LE
AMPAL16R6/B/A/AL/L/Q	
AMPAL16R4/B/A/AL/L/Q	
AMPAL16L8/B/A/AL/L/Q	
AMPAL16H8/A/L	
AMPAL16LD8/A/L	
AMPAL16HD8/A/L	

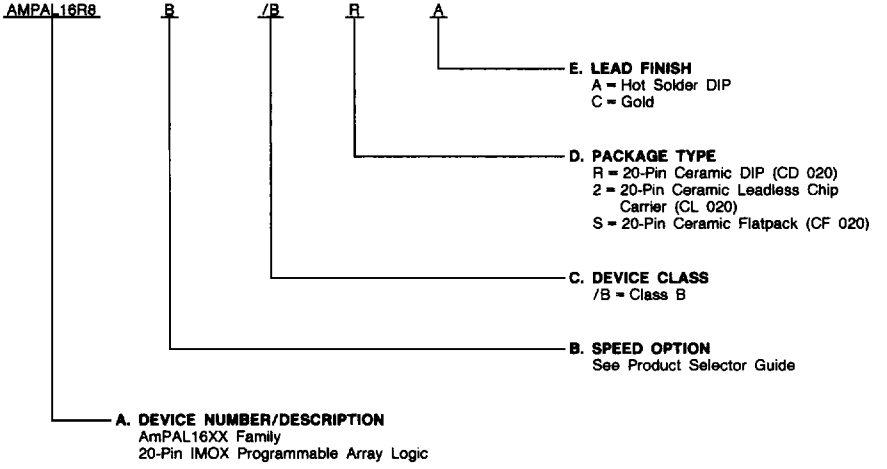
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AMPAL16R8/B/A/AL/L/Q	/BRA, /B2C, /BSA
AMPAL16R6/B/A/AL/L/Q	
AMPAL16R4/B/A/AL/L/Q	
AMPAL16L8/B/A/AL/L/Q	
AMPAL16H8/A/L	
AMPAL16LD8/A/L	
AMPAL16HD8/A/L	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 4, 9, 10, 11.

DESC Certified PAL Devices

Generic	AMD Part Number	DESC Numbers
16L8	AmPAL16L8A/BRA	8103607RX
	AmPAL16L8A/B2C	81036072X
	AmPAL16L8A/BSA	8103607SX
	AmPAL16L8L/BRA	8103611RX
	AmPAL16L8L/B2C	81036112X
	AmPAL16L8L/BSA	8103611SX
	AmPAL16L8/BRA	8103601RX
	AmPAL16L8/B2C	81036012X
16R8	AmPAL16R8A/BRA	8103608RX
	AmPAL16R8A/B2C	81036082X
	AmPAL16R8A/BSA	8103608SX
	AmPAL16R8L/BRA	8103612RX
	AmPAL16R8L/B2C	81036122X
	AmPAL16R8L/BSA	8103612SX
	AmPAL16R8/BRA	8103602RX
	AmPAL16R8/B2C	81036022X
16R6	AmPAL16R6A/BRA	8103609RX
	AmPAL16R6A/B2C	81036092X
	AmPAL16R6A/BSA	8103609SX
	AmPAL16R6L/BRA	8103613RX
	AmPAL16R6L/B2C	81036132X
	AmPAL16R6L/BSA	8103613SX
	AmPAL16R6/BRA	8103603RX
	AmPAL16R6/B2C	81036032X
16R4	AmPAL16R4A/BRA	8103610RX
	AmPAL16R4A/B2C	81036102X
	AmPAL16R4A/BSA	8103610SX
	AmPAL16R4L/BRA	8103614RX
	AmPAL16R4L/B2C	81036142X
	AmPAL16R4L/BSA	8103614SX
	AmPAL16R4/BRA	8103604RX
	AmPAL16R4/B2C	81036042X

FUNCTIONAL DESCRIPTION

AMD PAL Family Characteristics

All members of the AMD PAL Family have common electrical characteristics and programming procedures. All parts are produced with a fusible link at each input to the AND-gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Initially the AND gates are connected, via fuses, to both the TRUE and complement of each input. By selective programming of fuses the AND gates may be "connected" to only the TRUE input (by blowing the complement fuse), to only the complement input (by blowing the TRUE fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the TRUE and complement fuses are left intact a logical FALSE results on the output of the AND gate, while all fuses blown results in a logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates. The only limitations imposed are the number of inputs to the AND gates (up to 16) and the number of AND gates per OR (up to 8).

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Power-Up RESET

The registered devices in the AMD PAL family have been designed to reset during system power-up. Following power-up, all registers will be initialized to zero, setting all the outputs to a logic 1. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization.

PRELOAD

AMD PAL devices are designed with unique PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the registered output of an AMD PAL device.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Without PRELOAD, it is difficult and in some cases impossible to load an arbitrary present state value. This can lead to logic verification sequences that are either incomplete or excessively long. Long test sequences result when the feedback from the state register "interferes" with the inputs, forcing the machine to go through many transitions before it can reach an arbitrary state value. Therefore the test sequence will be mostly state initialization and not actual testing. The test sequence becomes excessively long when a state must be reentered many times to test a wide variety of input combinations.

In addition, complete logic verification may become impossible when states that need to be tested cannot be entered with normal state transitions. For example, even though necessary, the state entered when a machine powers up cannot be tested, because it cannot be entered from the main sequence. Similarly, "forbidden" or "don't care" states that are not normally entered need to be tested to ensure that they return to the main sequence.

PRELOAD eliminates these problems by providing the capability to go directly to any desired arbitrary state. Thus test sequences may be greatly shortened, and all possible states can be tested, greatly reducing test time and development costs, and guaranteeing proper in-system operation.

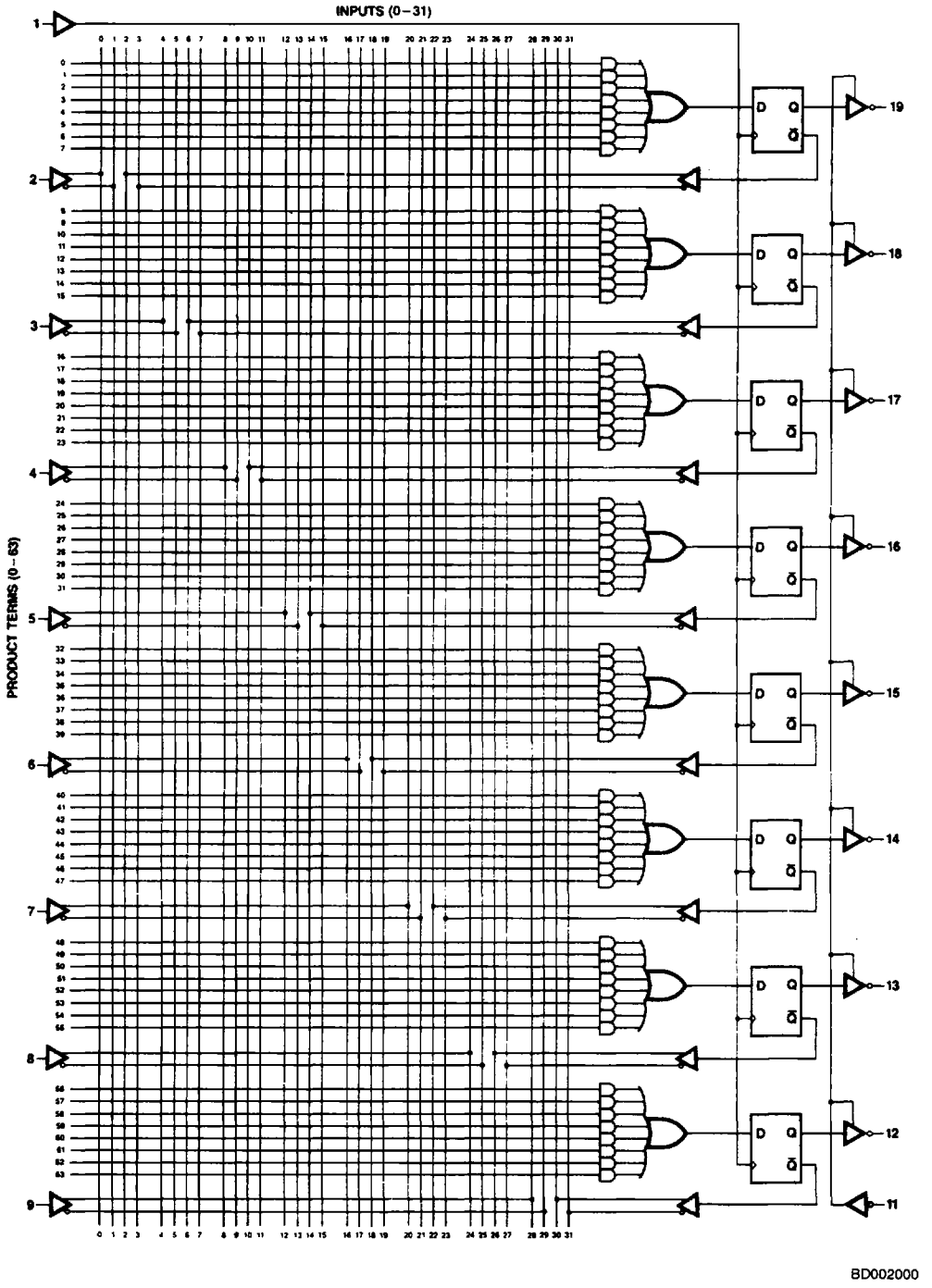


Figure 1. AmPAL16R8 Logic Diagram

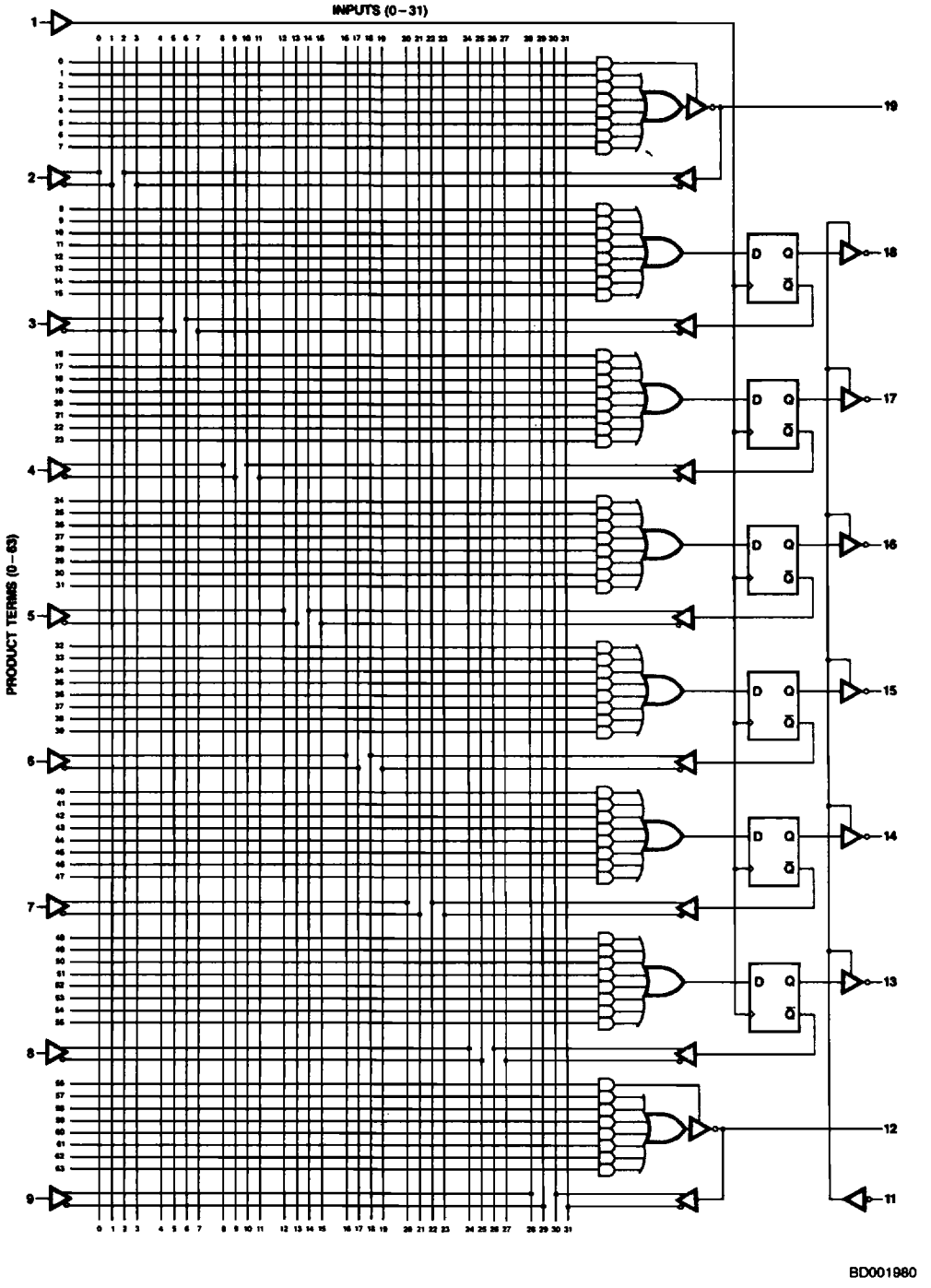


Figure 2. AmPAL16R6 Logic Diagram

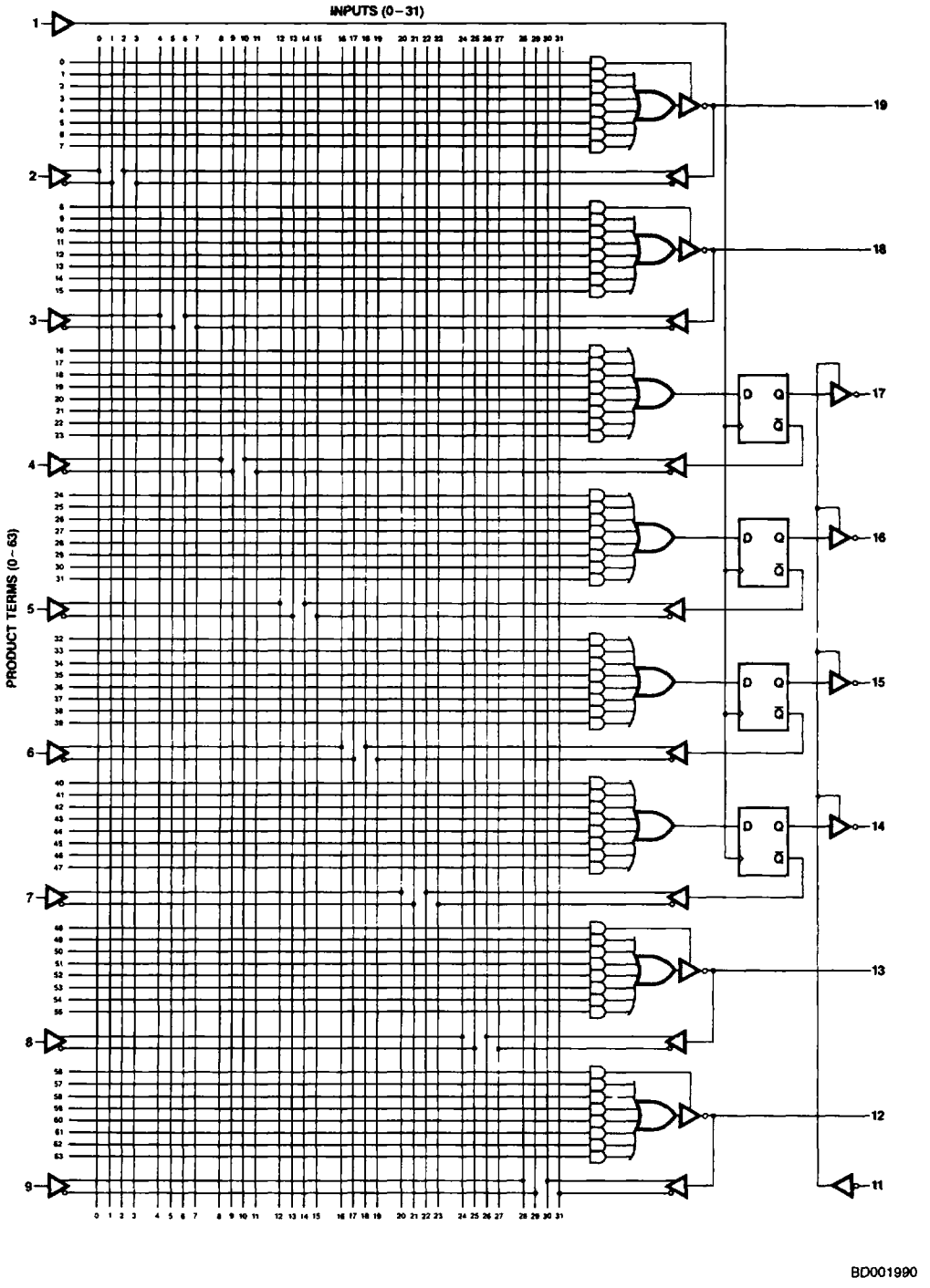


Figure 3. AmPAL16R4 Logic Diagram

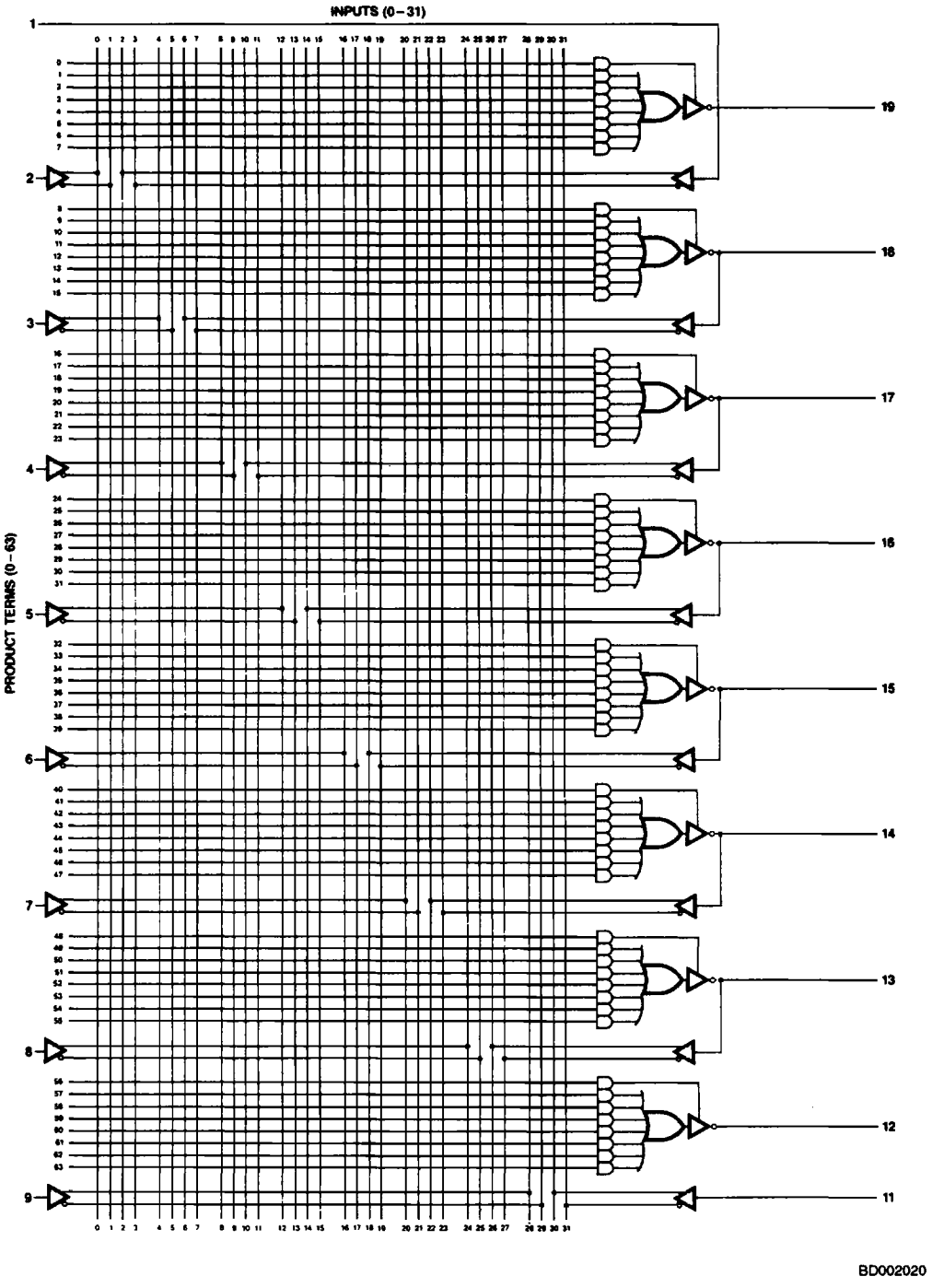


Figure 4. AmPAL16L8 Logic Diagram

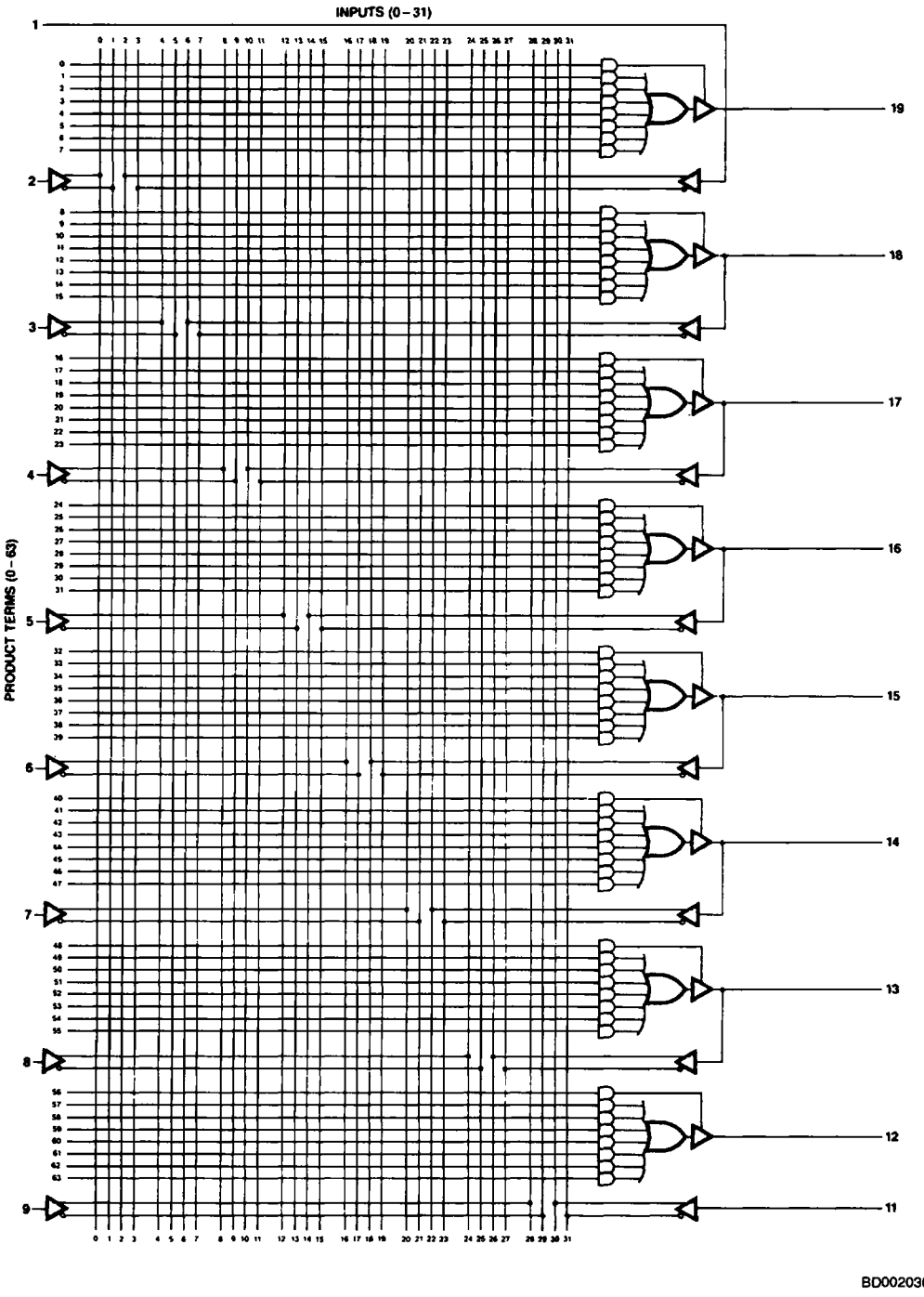


Figure 5. AmPAL16H8 Logic Diagram

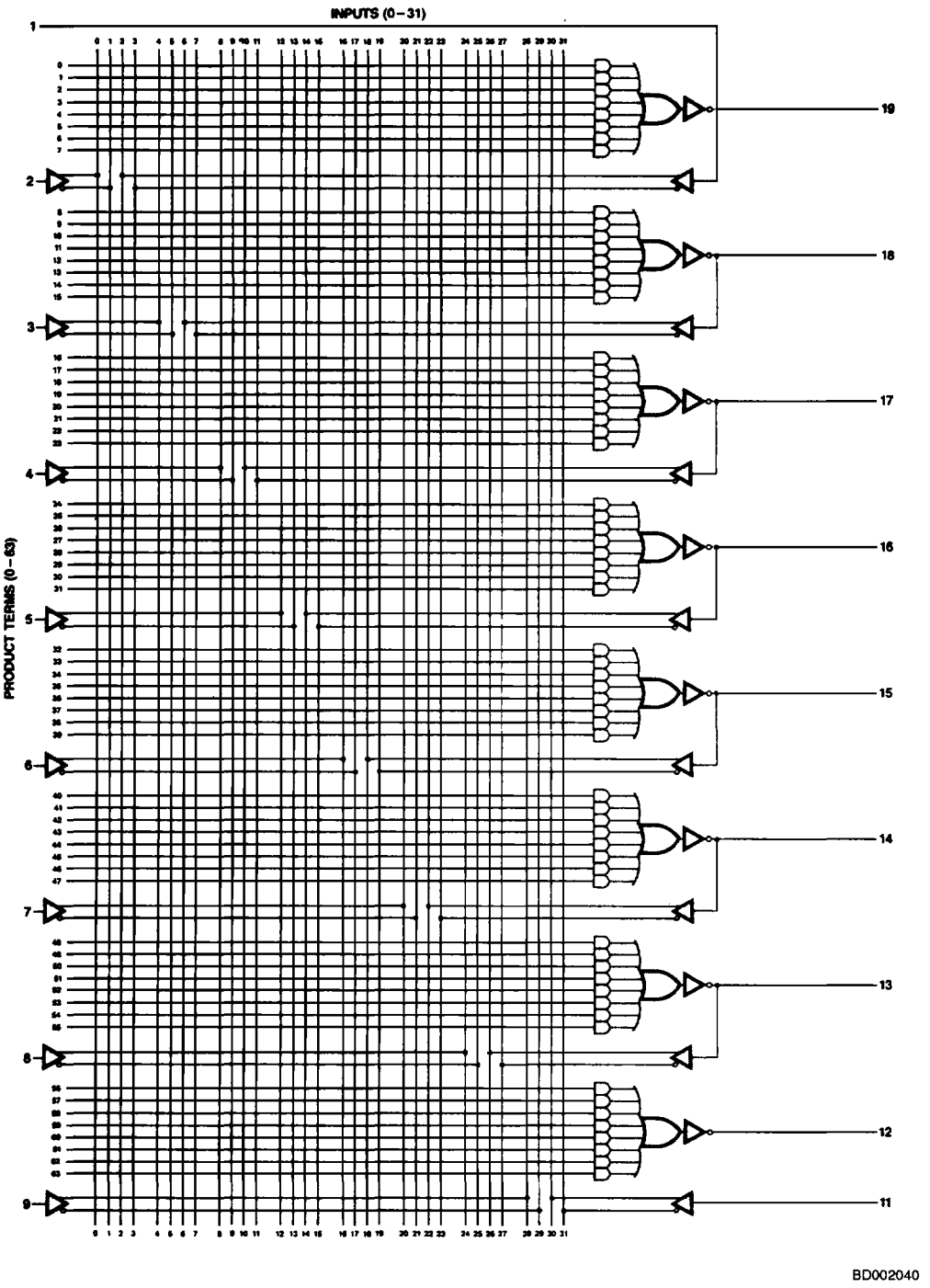


Figure 6. AmPAL16LD8 Logic Diagram

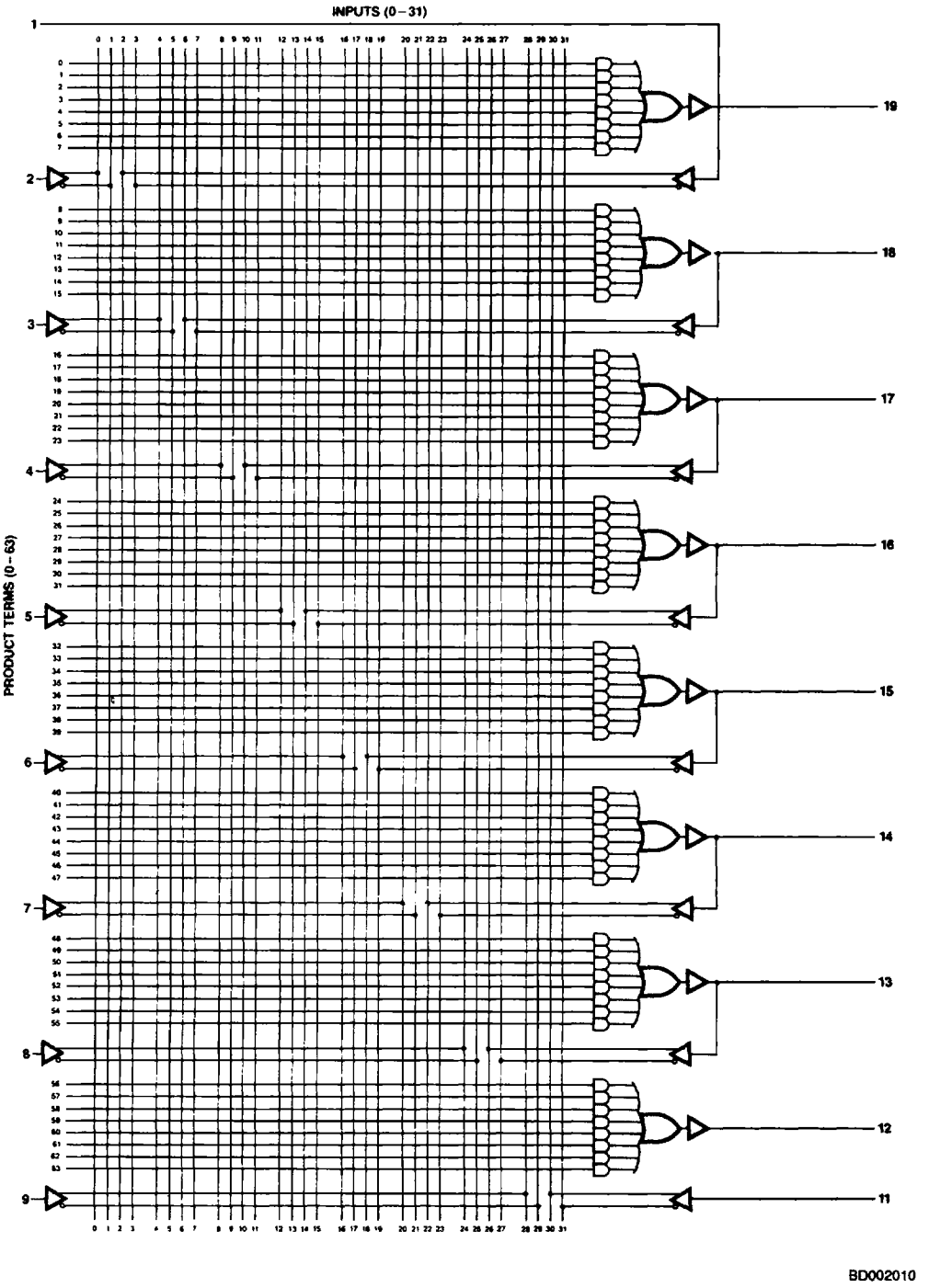


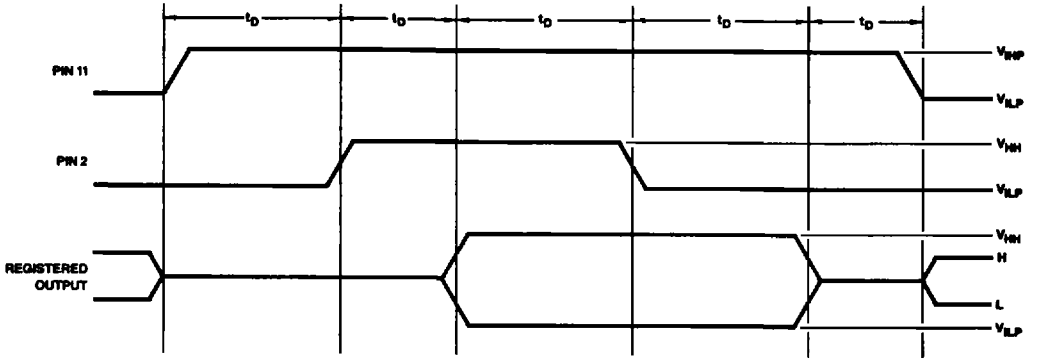
Figure 7. AmPAL16HD8 Logic Diagram

APPLICATIONS

PRELOAD of Registered Outputs

AMD PAL registered outputs are designed with extra circuitry to allow loading each register asynchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



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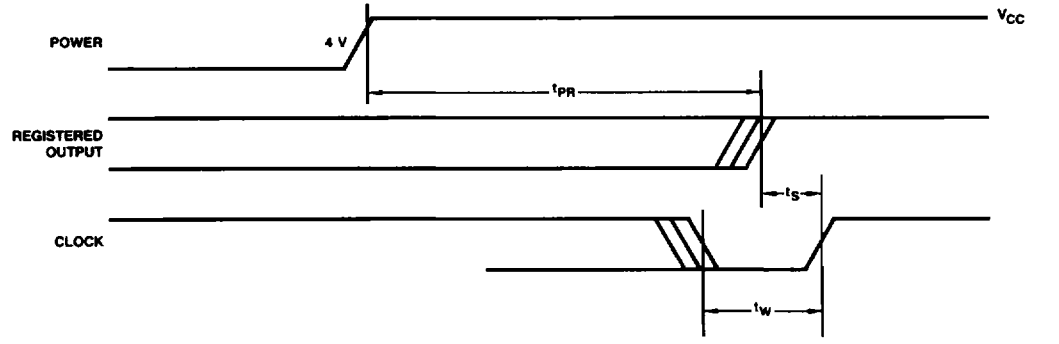
Level forced on registered output pin during PRELOAD cycle	State of the output pin after cycle
V_{HH}	HIGH
0 V to V_{CCH} or OPEN	LOW

Power-Up Reset

The registered devices in the AMD PAL Family have been designed to reset during system power-up. Due to the asynchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from low to high until all applicable input and feedback setup times are met.



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Parameters	Description	Min.	Typ.	Max.	Units
t_{PR}	Power-Up Reset Time	-	600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	Clock Width				

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
(Pin 20 to Pin 10) Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming).....−0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 21 V
Output Current Into Outputs During
Programming (Max Duration of 1 sec) ..... 200 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Extended Commercial (E) Devices
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Military (M) Devices*
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3, 4 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	"Q"	I_{OH} = −2 mA	COM'L	2.4	3.5		V
			All others	I_{OH} = −3.2 mA	COM'L				
				I_{OH} = −2 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	"B," "A," "Std." "AL," & "L"	I_{OL} = 24 mA	COM'L			0.5	V
				I_{OL} = 12 mA	MIL				
			"Q"	I_{OL} = 12 mA	COM'L				
				I_{OL} = 8 mA	MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs				2.0		5.5	V
V_{IL} (Note 2)	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs						0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., I_{IN} = 0.40 V		"B," "AL," & "Q"			−20	−100	μA
				"A," "L," & "Std."			−20	−250	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V						25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V						1.0	mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 3)				−30	−60	−90	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.		16L8A, 16H8A, 16HD8A, 16LD8A, 16L8, 16H8, 16HD8, 16LD8			110	155	mA
				16L8L, 16H8L, 16HD8L, 16LD8L			55	80	
				16R8B, 16R6B, 16R4B, 16L8B, 16R8A, 16R6A, 16R4A, 16R8, 16R6, 16R4				180	
				16R8L, 16R6L, 16R4L, 16L8AL, 16R8AL, 16R6AL, 16R4AL			60	90	
				16L8Q, 16R8Q, 16R6Q, 16R4Q				45	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−0.9	−1.2	V
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = Max., V_{IL} = 0.8 V V_{IH} = 2.0 V		V_O = 2.7 V				100	μA
I_{OZL}				V_O = 0.4 V				−100	
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 5)					6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz (Note 5)					9		

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

COMMERCIAL RANGE

No.	Parameter Symbol	Parameter Description	"B" Version			"A" & "AL" Version			"Std," "L" & "Q" Versions			Units
			Typ. (Note 1)	Min.	Max.	Typ. (Note 1)	Min.	Max.	Typ. (Note 1)	Min.	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4, 16LD8, 16H8, 16HD8	12		15	17		25	23		35	ns
2	t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8	12		15	17		25	23		35	ns
3	t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8	12		15	17		25	23		35	ns
4	t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4	8		15	12		20	17		25	ns
5	t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4	8		15	12		20	17		25	ns
6	t_{CO}	Clock to Output 16R8, 16R6, 16R4	8		12	12		15	17		25	ns
7	t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	10	13		15	20		20	30		ns
8	t_H	Hold Time 16R8, 16R6, 16R4	−8	0		−10	0		−10	0		ns
9	t_P	Clock Period ($t_S + t_{CO}$)		25			35			55		ns
10	t_W	Clock Width		10			15			25		ns
11	$f_{MAX.}$	Maximum Frequency			40			28.5			18	MHz

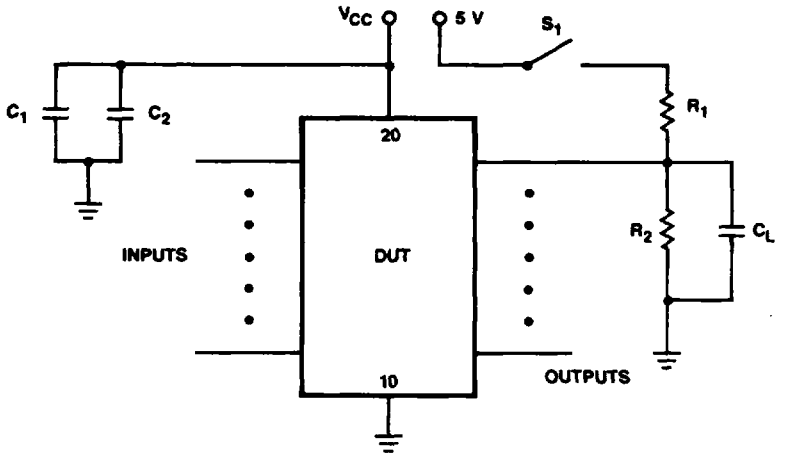
Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

MILITARY RANGE

No.	Parameter Symbol	Parameter Description	"B" Version			"A" & "AL" Version			"Std," "L" & "Q" Versions			Units
			Typ. (Note 1)	Min.	Max.	Typ. (Note 1)	Min.	Max.	Typ. (Note 1)	Min.	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4, 16LD8, 16H8, 16HD8	12		20	17		30	23		40	ns
2	t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8	12		20	17		30	23		40	ns
3	t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8	12		20	17		30	23		40	ns
4	t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4	8		20	12		25	17		25	ns
5	t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4	8		20	12		25	17		25	ns
6	t_{CO}	Clock to Output 16R8, 16R6, 16R4	8		15	12		20	17		25	ns
7	t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	10	18		15	25		20	35		ns
8	t_H	Hold Time 16R8, 16R6, 16R4	−8	0		−10	0		−10	0		ns
9	t_P	Clock Period ($t_S + t_{CO}$)		33			45			60		ns
10	t_W	Clock Width		12			20			25		ns
11	$f_{MAX.}$	Maximum Frequency			30			22			16.5	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

SWITCHING TEST CIRCUIT

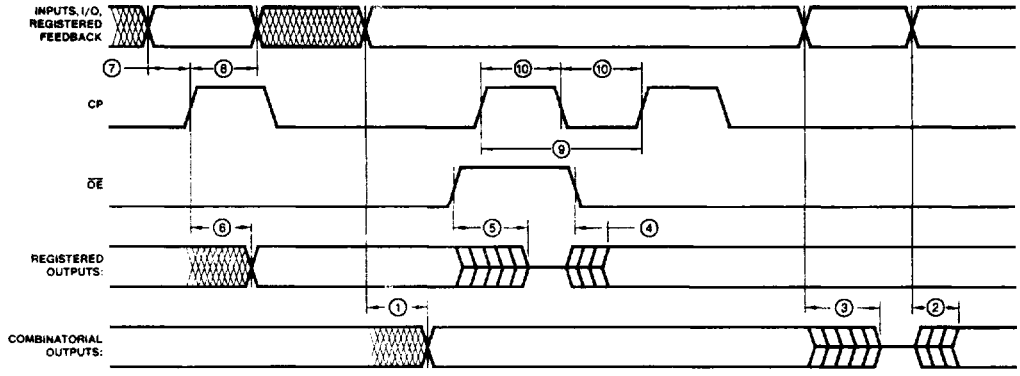


Note: C_1 and C_2 are to bypass V_{CC} to ground.

TEST OUTPUT LOADS

	"Std," "B," "A," "AL" & "L"		"Q"	
Pin Name	**Commercial**	**Military**	**Commercial**	**Military**
R_1	200 Ω	390 Ω	390 Ω	600 Ω
R_2	390 Ω	750 Ω	750 Ω	1200 Ω
C_1	1 μF	1 μF	1 μF	1 μF
C_2	0.1 μF	0.1 μF	0.1 μF	0.1 μF
C_L	50 pF	50 pF	50 pF	50 pF

SWITCHING WAVEFORMS



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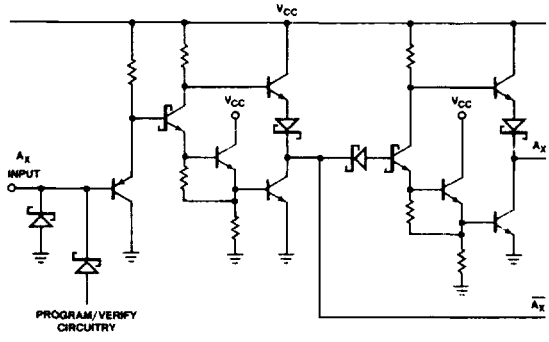
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

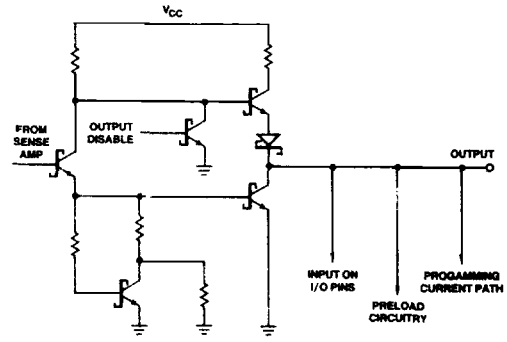
KS000010

INPUT CIRCUITRY



IC000720

OUTPUT CIRCUITRY



IC000730

PROGRAMMING

Each AMD PAL fuse is programmed with a simple sequence of voltages applied to two control pins (1 and 11) and programming voltage pulse applied to the output under programming. Addressing of the 2048 element fuse array is accomplished with normal TTL levels on eight input pins (five select the input line number and three select the product term number). V_{CC} is maintained at a normal level throughout the programming and verify cycle – no extra high levels are required.

The necessary sequence levels for programming any fuse is shown in the Programming Waveforms. The address of each fuse in terms of Input Line Number and Product Term Line Number is defined by the Fuse Address Tables 1 and 2. Current, voltage and timing requirements for each pin are specified in the Programming Parameter Table below.

The 16L8, 16R8, 16R6, 16R4, 16H8, 16LD8 and 16HD8 use identical programming conditions and sequences.

After all programming has been completed, the entire array should be reverified at V_{CCL} and again at V_{CCH}. Reverification can be accomplished by reading all eight outputs in parallel rather than one at a time. The array fuse verification cycle checks that the correct array fuses have been blown and can be sensed by the outputs.

AMD PAL devices have been designed with many internal test features that are used to assure high programming yield and correct logical operation for a correctly programmed part.

An additional fuse is provided on each AMD PAL circuit to prevent unauthorized copying of AMD PAL fuse patterns when design security is desired. Blowing the security fuse blocks entry to the fuse pattern verify mode.

To blow the security fuse:

1. Power up part to V_{CCP}
2. Raise Pin 5 to V_{HH}.
3. Pulse Pin 11 from ground to V_{OP} for a 50μsec duration.
4. Perform a normal end-of-programming verify cycle at V_{CCL} and V_{CCH}. All fuse locations should be sensed as blown if the security fuse has been successfully blown.

Note that parts with the security fuse blown may not be returned as programming rejects.

AMD PAL devices normally have high programming yields (> 98%). Programming yield losses are frequently due to poor socket contact, equipment out of calibration or improperly used.

PROGRAMMING PARAMETERS $T_A = 25°C$

Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Units
V_{HH}	Control Pin Extra High Level	Pin 1 @ 10-40 mA	10	11	12	V
		Pin 11 @ 10-40 mA	10	11	12	
V_{OP}	Program Voltage Pins 12-19 @ 15-200 mA		18	20	22	V
V_{IHP}	Input HIGH Level During Programming and Verify		2.4	5	5.5	V
V_{ILP}	Input LOW Level During Programming and Verify		0.0	0.3	0.5	V
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50-200 mA		5	5.2	5.5	V
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50-200 mA		4.1	4.3	4.5	V
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50-200 mA		5.4	5.7	6.0	V
V_{Blown}	Successful Blown Fuse Sense Level @ Output	16L8, 16R8, 16R6, 16R4, 16LD8		0.3	0.5	V
		16H8, 16HD8	2.4	3		
V_{OP}/dt	Rate of Output Voltage Change		20		250	V/μs
dV_{11}/dt	Rate of Fusing Enable Voltage Change (Pin 11 Rising Edge)		100		1000	V/μs
t_P	Fusing Time First Attempt		40	50	100	μs
	Subsequent Attempts		4	5	10	ms
t_D	Delays Between Various Level Changes		100	200	1000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level				500	ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed		$V_{CCP} - 0.3$	V_{CCP}	$V_{CCP} + 0.3$	V
R	Pull-Up Resistor On Outputs Not Being Programmed		1.9	2	2.1	kΩ

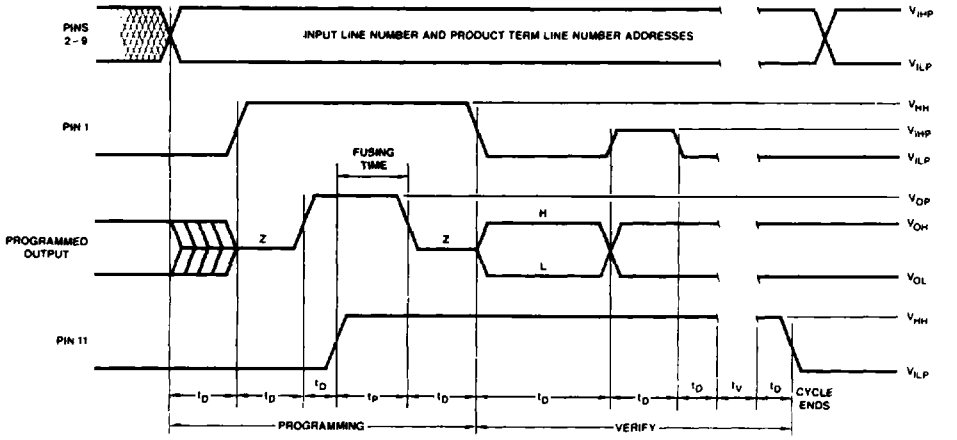
Design Aid Software for AmPAL16XX Family

Name	Vendor	Versions	Notes
ABEL	Data I/O (206) 881-6444	IBM PC VAX/VMS VAX/UNIX	Rev 1.1
CUPL	P-CAD Systems (408) 971-1300	IBM PC VAX/VMS VAX/UNIX CPM 80/86	Rev 2.1
AmCUPL	Advanced Micro Devices (408) 732-2400	IBM PC	Supported by P-CAD Systems

AMD Qualified Programmers

Name	Programmer Model(s)	AMD PAL Personality Module	Socket Adapter
Data I/O 10525 Willow Road N.E. Redmond, WA 93052	Systems 19, 29	950-1942-0044	303A-004, Rev 3 or newer
	60	N/A	360A-001, Rev 4 or newer
Stag Microsystems 528-5 Weddell Drive Sunnyvale, CA 94086	Model PPZ	2200	On Board
	ZL30	On Board Module (Rev 38 or newer)	
Structured Design 1700 Wyatt Drive Suite 3 Santa Clara, CA 95084	SD-1000J	N/A	On Board
Valley Data Sciences 2426 Charleston Road Mountain View, CA 94043	160 Series	N/A	On Board
Digelec 586 Weddell Drive Suite 1 Sunnyvale, CA 94089	803 Series	FAM-52	DA-53
JMC 2999 Monterey Rd. Monterey, CA 93940	PROMAC P3	On-board Module rev 2.0	On Board

PROGRAMMING TIMING DIAGRAM



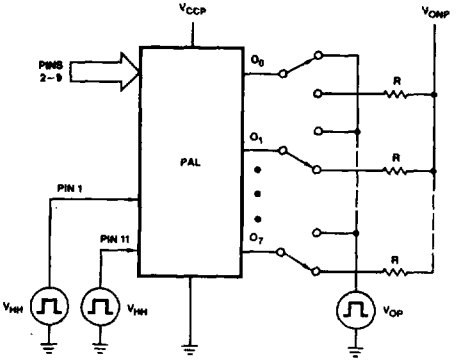
PF001100

TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States				
	9	8	7	6	5
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

L = V_{ILP}
H = V_{IHP}

SIMPLIFIED PROGRAMMING DIAGRAM



PF000380

TABLE 2. PRODUCT TERM ADDRESSING

Product Term Line Number								Product Term Select Address Pin		
								4	3	2
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	L	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	L	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	H	L
7	15	23	31	39	47	55	63	H	H	H
Pin 19	Pin 18	Pin 17	Pin 16	Pin 15	Pin 14	Pin 13	Pin 12			
Programming Access and Verify Pin										

L = V_{ILP}
H = V_{IHP}