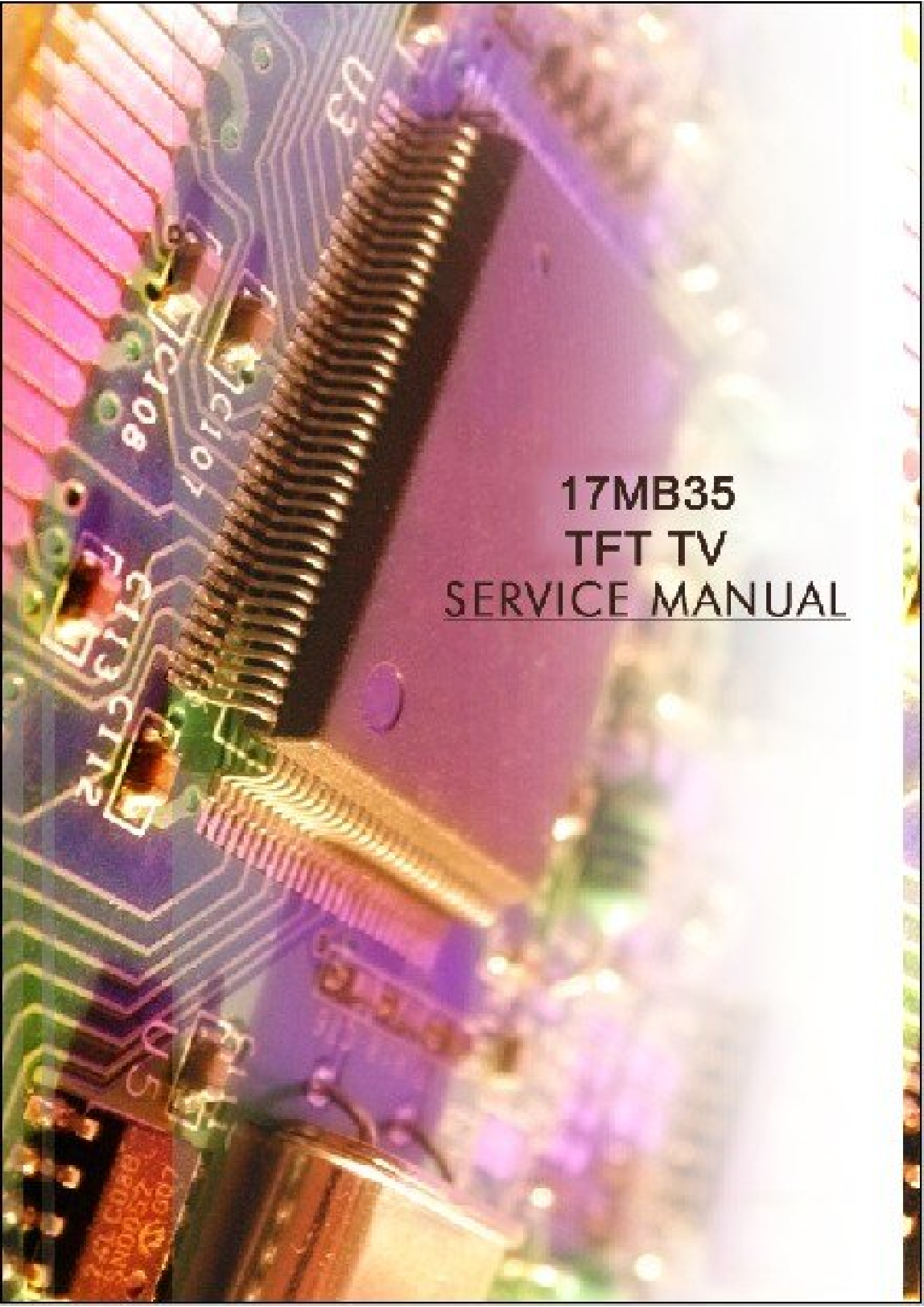


17MB35
TFT TV
SERVICE MANUAL

TABLE OF CONTENTS

1. INTRODUCTION

17MB35 Main Board consists of MSTAR concept. This IC is capable of handling Audio processing, video processing, Scaling-Display processing, 3D comb filter, OSD and text processing, 8 bit dual LVDS transmitter.
TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo.

Sound system output is supplying 2x10W (10%THD) for stereo 8Ω speakers.
Supported peripherals are:

1 RF input VHF1, VHF3, UHF @ 75Ohm(Common)
1 Side AV (SVHS, CVBS, HP, R/L_Audio) (Common)
2 SCART sockets(Common)
1 YPbPr (Common)
1 PC input(Optional)
4 HDMI 1.3 input(2 HDMI inputs are common, 4 inputs are optional)
1 Stereo audio input for PC(Common)
1 Line out(Common)
1 Subwoofer out(Common)
1 S/PDIF output(Common)
1 Side S-Video(Optional)
1 Headphone(Common)
1 Common interface(Optional)
1 Digital USB(Opional)
1 Analog USB(Opional)
1 RS232(Optional)
1 Smart card connector(Optional)

2. TUNER

A horizontal mounted and Digital Half-Nim tuner is used in the product, which covers 3 Bands(From 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on the Tuner in use.

2.1. General description of TDTC-G101D:

The Tuner covers 3 Bands(from 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). Band selection and Tuning are performed digitally via the I2C bus.

2.2. Features of TDTC-G101D:

- Digital Half-NIM tuner for COFDM
- Covers 3 Bands(From 48MHz to 862MHz for COFDM,

- From 45.25MHz to 863.25MHz for CCIR CH)
- Including IF AGC with SAW Filter
- Bandwidth Switching (7/8 MHz) possible
- DC/DC Converter built in for Tuning Voltage
- Internal(or External) RF AGC, Antenna Power Optional

2.3. Pinning:

PIN NAME	PIN No.	PIN Description
Ant PWR	1	+5V (for Active Antenna), Optional
B1	2	+ 5V (for Loop through & DC-DC)
RF AGC	3	N.C
SCL	4	I²C Bus for TUNER PLL
SDA	5	I²C Bus for TUNER PLL
B2	6	+ 5V (for TU & IF AGC AMP)
Vtu T.P	7	N.C
AS	8	PLL IC Address selection
IF AGC Control	9	IF AGC Control
DIF2	10	Total IF Output2
DIF1	11	Total IF Output1
AIF	12	Tuner IF Output

3. AUDIO AMPLIFIER STAGE WITH MP7722

3.1. General Description

17MB35 uses a 20W Class D Stereo Single Ended Audio Amplifer for audio. The MP7722 is a stereo 20W Class D Audio Amplifier. It is one of MPS' second generation of fully integrated audio amplifiers which dramatically reduces solution size by integrating the following:

- 180mΩ power MOSFETs
- Startup / Shutdown pop elimination
- Short circuit protection
- Mute / Standby

The MP7722 utilizes a single ended output structure capable of delivering 2 x 20W into 4Ω speakers. MPS Class D Audio Amplifiers exhibit the high fidelity of a Class A/B amplifier at efficiencies greater than 90%. The circuit is based on the MPS' proprietary variable frequency topology that delivers low distortion, fast response time and operates on a single power supply.

3.2. Features

- 2 x 20W Output at VDD = 24V into a 4Ω load
- THD+N = 0.06% at 1W, 8Ω
- 93% Efficiency at 20W

- Low Noise (190μV Typical)
- Switching Frequency Up to 1MHz
- 9.5V to 24V Operation from a Single Supply
- Integrated Startup and Shutdown Pop Elimination Circuit
- Thermal and Short Circuit Protection
- Integrated 180mΩ Switches
- Mute/Standby Modes (Sleep)
- Thermally Enhanced 20-Pin TSSOP Package with Exposed Pad

3.3. Applications

- Surround Sound DVD Systems
- Televisions
- Flat Panel Monitors
- Multimedia Computers
- Home Stereo Systems

3.4. Absolute Ratings

3.4.1. Electrical Characteristics

V_{DD} = 24V, V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Standby Current		V_{EN} = 0V		2	10	μA
Quiescent Current				3	6	mA
Output Drivers						
SW On Resistance		Sourcing and Sinking		0.18		Ω
Short Circuit Current		Sourcing and Sinking		5.0		A
Inputs						
REF1/2, IN1/2 Input Common Mode Voltage Range			0	$\frac{V_{DD}}{2}$	V_{DD} – 1.5	V
REF1/2, IN1/2 Input Current		V_{PIN} = V_{NIN} = 12V		1	5	μA
EN Enable Threshold Voltage		V_{EN} Rising		1.4	2.0	V
		V_{EN} Falling	0.4	1.2		V
EN Enable Input Current		V_{EN} = 5V		1		μA
Thermal Shutdown						
Thermal Shutdown Trip Point		T_J Rising		150		°C
Thermal Shutdown Hysteresis				30		°C

3.4.2. Operating Specifications

Parameters	Symbol	Condition	Min	Typ	Max	Units
Standby Current		V_{EN} = 0V		260		μA
Quiescent Current				23		mA
Power Output		f = 1KHz, THD+N = 10%, 4Ω Load		20		W
		f = 1KHz, THD+N = 10%, 8Ω Load		10		W
THD+ Noise		P_{OUT} = 1W, f = 1KHz, 4Ω Load		0.16		%
		P_{OUT} = 1W, f = 1KHz, 8Ω Load		0.06		%
Efficiency		f = 1KHz, P_{OUT} = 1W, 4Ω Load		90		%
		f = 1KHz, P_{OUT} = 1W, 8Ω Load		95		%
Maximum Power Bandwidth				20		KHz
Dynamic Range				93		dB
Noise Floor		A-Weighted		190		μV
Power Supply Rejection		f = 1KHz		60		dB

3.5. Pinning

Pin #	Name	Description
1, 5, 11, 16	NC	No Connect. Not internally connected
2	REF1	Amplifier 1 Reference. REF1 is the reference point for amplifier 1. Use a resistive voltage divider to set the voltage at REF1 to V_{DD}/2.
3	IN1	Amplifier 1 Input. IN1 is the input for amplifier 1. This is an inverting input.
4	AGND1	Analog Ground 1. Connect AGND1 to AGND2.
6	EN1	Enable Input 1. EN1 must be connected to EN2. Drive high to enable MP7722, drive low to disable.
7	IN2	Amplifier 2 Input. IN2 is the input for amplifier 2. This is an inverting input.
8	REF2	Amplifier 2 Reference. REF2 is the reference point for amplifier 2. Use a resistive voltage divider to set the voltage at REF1 to V_{DD}/2.
9	AGND2	Analog Ground 2. Connect AGND2 to AGND1.
10	EN2	Enable Input 2. EN2 must be connected to EN1. Drive high to enable MP7722, drive low to disable.
12	BS2	High-Side MOSFET Bootstrap Input for Amplifier 2. A capacitor from BS2 to SW2 supplies the gate drive current to the internal high-side MOSFET. Connect a 1μF capacitor from SW2 to BS2.
13	VDD2	Power Supply Input. Bypass VDD2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN13 and PIN15.
14	SW2	Switched Power Output. SW2 is the output of Amplifier 2. Connect the LC filter to this pin.
15	PGND2	Power Ground for Amplifier 2. Connect PGND2 to PGND1.
17	BS1	High-Side MOSFET Bootstrap Input for Amplifier 1. A capacitor from BS1 to SW1 supplies the gate drive current to the internal high-side MOSFET. Connect a 1μF capacitor from SW1 to BS1. See Figure 1.
18	VDD1	Power Supply Input. Bypass VDD1 to PGND1 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the IC PIN18 and PIN20.
19	SW1	Switched Power Output. SW1 is the output of Amplifier 1. Connect the LC filter to this pin. See Figure 1.
20	PGND1	Power Ground for Amplifier 1. Connect PGND1 to PGND2. See Figure 1.

4. POWER STAGE

The DC voltages required at various parts of the chassis and inverters are provided by a main power supply unit. The power supply generates 33V, 24V, 12V, 5V, 3,3V and 5V, 3,3V stand by mode DC voltages. Power stage which is on-chasis generates 1,26V stand by voltage and 8V, 2,6V, 1,8V and 1V supplies for other different parts of the chassis.

5. MICROCONTROLLER (MSTAR)

5.1. General Descripction

The MST6WB7GQ-3 is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard TV video and audio decoder, two video de-interlacers, two scaling engines, the MStarACE-3 color engine, an on-screen display controller, an 8-bit MCU and a built-in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3-D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST6WB7GQ-3 also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

5.2. General Features

LCD TV controller with PIP/POP display functions

- Input supports up to UXGA & 1080P
- Panel supports up to full HD (1920x1080)
- TV decoder with 3-D comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 3-D video de-interlacers
- 3-D video noise reduction
- Full function PIP/PBP/POP
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controler engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8/10-bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 296-pin LQFP

NTSC/PAL/SECAM Video Decoder

- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- Motion adaptive 3-D comb filter for NTSC/PAL

- 8 configurable CVBS & Y/C S-video inputs
- Supports Teletext level-1.5, WSS, VPS, Closed-caption, and V-chip
- Macrovision detection
- CVBS video output

Video IF for Multi-Standard Analog TV

- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

Multi-Standard TV Sound Decoder

- Supports BTSC/NICAM/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- L/Rx4, mono, and SIF audio inputs
- L/Rx3 loudspeaker and line outputs
- Supports sub-woofer output
- Built-in audio output DAC's
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, and virtual stereo/surround
- Optional advanced surround available (Dolby1, SRS2, BBE3… etc)

Digital Audio Interface

- I2S digital audio input & output
- S/PDIF digital audio input & output
- HDMI audio channel processing capability
- Programmable delay for audio/video synchronization

Analog RGB Compliant Input Ports

- Three analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

DVI/HDCP/HDMI Compliant Input Port

- Two HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection(HDCP) 1.1 compliant receiver

6. SIL9185 3:1 HDMI 1.3 Switch

6.1. General Desription

The SiI9185A is the first generation of TMDS switch device supporting Revision 1.3 of the HDMI Specification (HDMI Consortium; June 2006). With three HDMI inputs and a single output, the SiI9185A provides a low-cost method of adding additional HDMI ports to the latest Digital TVs. New DTVs can easily connect to the many HDMI sources coming on the market, including DVDs, STB, game consoles, PCs, camcorders, and digital still cameras. The SiI9185A is a fully HDMI compliant device providing a simple, lowcost method of retransmitting protected digital audio and video, giving end-users a truly all-digital experience. Built-in backward compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 source. The SiI9185A provides additional integrated features to help lower system cost and provide enhanced features to the end consumer. To lower system cost, the SiI9185A provides a complete solution for switching sink-side HDMI signals. This includes DDC switching, individual HPD control, and 5V sense. The addition of these features eliminates additional external components, helping to lower cost. For source-side applications, the SiI9185A DDC switching can be bypassed with an external 4-channel I2C-bus switch(e.g., Texas Instruments PCA95445) to allow clock stretching.

6.2. Features

- Three-input, single-output HDMI switcher
- Integrated TMDS® receiver and transmitt cores capable of receiving and transmitting 2.25 Gbps:
- Support 60 Hz, 12-bit or 720p/1080i, 120 Hz, 12-bit
- Builcable support even at deep-color resolutions
- Pre-emphasi
- DVI 1.0, HDCP 1.1 and HDM compliant receiver and transmitter
- Uses HDMI-compliant TMDS core recovery and retransmission, unlike TMDS switches, which use high-spee analog switches and degrade TMDS signals
- Built-in Cons support:
- HDM lowers cost for adding CEC support to DTV
- Integra requirements on system microcontrolle speeds design

6.3. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Note
DVCC18	Digital Core Supply Voltage	−0.5	-	2.5	V	1, 2, 3
AVCC18	TMDS Analog Supply Voltage	−0.3	-	2.5	V	1, 2, 3
AVCC33	TMDS Analog Supply Voltage	−0.3	-	4.0	V	1, 2, 3
V_I	Input Voltage	−0.3	-	AVCC33+ 0.3	V	1, 2, 4
V_O	Output Voltage	−0.3	-	AVCC33+ 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5V Tolerant Pins	−0.3	-	5.5	V	4
T_J	Junction Temperature	-	-	125	°C	-
T_{STG}	Storage Temperature	−65	-	150	°C	-

6.4. Pinning

System Switching Pins

Pin Name	Pin #	Type	Dir	Description
DSDA0, DSDA1, DSDA2	30, 50, 70	LVTTL, Schmitt Trigger, 5V Tolerant	Input/ Output	DDC I^2C Data for respective port. See Note 1.
DSCL0, DSCL1, DSCL2	31, 51, 71	LVTTL, Schmitt Trigger, 5V Tolerant	Input	DDC I^2C Clock for respective port. See Note 1.
RPWR0, RPWR1, RPWR2	32, 52, 72	LVTTL, 5V Tolerant	Input	5V Port detection input for respective port. Connect to 5V signal from HDMI input connector.
HPD0, HDP1, HPD2	16, 36, 56	LVTTL, 2mA, 5V Tolerant	Output	Hot Plug Detect Output for respective port. Connect to HOTPLUG of HDMI input connector.
HPDIN	76	LVTTL, 5V Tolerant	Input	Hot Plug Detect Input.
TSCL	78	LVTTL, Schmitt Trigger. Open Drain 5V Tolerant	Output	Master DDC I^2C Clock (Open Drain Output) to HDMI receiver. I^2C transactions required for HDCP operation are performed over this I^2C bus. See Note 1.
TSDA	77	LVTTL, Schmitt Trigger, 5V Tolerant	Input/ Output	Master DDC Data (Open drain output.) to HDMI receiver. I^2C transactions required for HDCP operation are performed over this I^2C bus. See Note 1.

Configuration Pins

Pin Name	Pin #	Type	Dir	Description
I2CADDR/ TPWR	79	LVTTL, 4mA, 5V Tolerant	Input/ Output	I^2C Slave Address input / Transmit Power Sense output pin. When RESET# is low, this pin is used as an input to latch the I^2C sub-address. The level on this pin is latched when the RESET# pin transitions from low to high. When RESET# is high, this pin is used as the TPWR output, indicating that the selected Rx-port has 5V present. When none of the Rx ports are selected, this signal is low. See page 9 for more information.
I2CSEL/ INT#	35	Schmitt Trigger, Open Drain, 4mA, 5V Tolerant	Input/ Output	I^2C Selection input / Interrupt output pin. When RESET# is low, this pin is used as an input to latch the External Port Detection signal. The level on this pin is latched when the RESET# pin transitions from low to high. When this pin is low during reset, the external pins EPSEL1/LSCL and EPSEL0/LSDA are used to select the Rx-port as EPSEL[1:0]. When this pin is high during reset, the internal local I^2C register is used to select the Rx-port. After reset, this pin becomes the Interrupt output. This is an open-drain output and requires an external pull-up. See page 8 for more information.
RSVDL	75		Input	Reserved for use by Silicon Image and must be tied low.

Control Pins

Pin Name	Pin #	Type	Dir	Description
RESET#	13	LVTTL, Schmitt Trigger. 5V Tolerant	Input	Reset Pin (Active LOW). Certain configuration inputs are latched when RESET# transitions from low to high. See page 8 for more information.
LSCL/ EPSEL1	15	Schmitt 5V Tolerant	Input	Local I^2C Clock / External Port Select 1. When I2CSEL is high, this becomes the Local I^2C bus clock pin, LSCL. When I2CSEL is low, this becomes the external port select pin, EPSEL1. True open drain, so does not pull to ground if power not applied. An external pull-up is required. See page 8 for more information.
LSDA/ EPSEL0	14	LVTTL, Schmitt Trigger. Open Drain 5V Tolerant	Input/ Output	Local I^2C Data / External Port Select 0. When I2CSEL is high, this becomes the Local I^2C bus data pin, LSDA. When I2CSEL is low, this becomes the external port select pin, EPSEL0. True open drain, so does not pull to ground if power not applied. An external pull-up is required. See page 8 for more information.

CEC Pins

Pin Name	Pin #	Type	Direction	Description
CEC_A	54	CEC Compliant, 5V Tolerant	Input/ Output	HDMI compliant CEC I/O used to interface to CEC devices. CEC electrically compliant signal. This pin connects to the CEC signal of all HDMI connectors in the system. As an input, the pad acts as a LVTTL Schmitt triggered input and is 5V tolerant. As an output, the pad acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor.
CEC_D	53	LVTTL, Schmitt Trigger 5V Tolerant	Input/ Output	CEC interface to local system. True open-drain. An external pull-up is required. This pin typically connects to the local CPU.

Power and Ground Pins

Pin Name	Pin #	Type	Description
AVCC33	23, 43, 55, 63	Power	Analog VCC. Connect to 3.3V supply.
AVCC18	6, 17, 29, 37, 49, 57, 69	Power	Analog VCC. Connect to 1.8V supply.
AGND	3, 9, 20, 26, 40, 46, 60, 66, 80	Ground	Analog GND.
DVCC18	33, 73	Power	Digital VCC. Connect to 1.8V supply.
DGND	34, 74	Ground	Digital GND.

7. QAM DEMODULATOR – STV0297E

7.1. General Desription

The STV0297E is a complete single-chip QAM (quadrature amplitude modulation) demodulation and FEC (forward error correction) solution that performs sampled IF to transport stream (MPEG-2 or MPEG-4) block processing of QAM signals. It is intended for the digital transmission of compressed television, sound, and data services over cable. It is fully compliant with ITU-T J83 Annexes A/C or DVB-C specification bitstreams (ETS 300 429, “Digital broadcasting systems for television, sound and data services – Framing structure, channel coding and modulation - Cable Systems”). It can handle square (16, 64, 256-QAM) and non-square (32, 128-QAM) constellations.

Japanese DBS systems require a transport stream multiplex frame (TSMF) layer to carry digital signals over cable systems. When the recovered transport stream is a multiplex frame, the STV0297E post-processes it to extract a single transport stream. Automatic detection of the TSMF layer is provided. The chip integrates an analog-to-digital converter that delivers the required performance to handle up to 256-QAM signals in a direct IF sampling architecture, thus eliminating the need for external downconversion.

7.2. Features

- Decodes ITU-T J.83-Annexes A/C and DVB-C bit streams
- Processes Japanese transport stream multiplex frame (TSMF)
- High-performance integrated A/D converter suitable for direct IF architecture in all QAM (quadrature amplitude modulation) modes
- Supports 16, 32, 64, 128 and 256 point constellations
- Small footprint package: (10 x 10 mm²)
- Very low power consumption
- Full digital demodulation
- Variable symbol rates
- Front derotator for better low symbol rate performance and relaxed tuner constraints
- Integrated matched filtering
- Robust integrated adaptive pre and post equalizer
- On-chip FEC A/C with ability to bypass individual blocks
- 10 programmable GPIO
- Two AGC outputs suitable for delayed AGC applications (sigma-delta outputs)
- Integrated signal quality monitors, plus lock indicator and interrupt function mapped to GPIO pin
- Improved signal acquisition
- System clock generated on-chip from quartz crystal
- Low frequency crystal operations 4, 16, 25 - 30 MHz
- 4 I2C addresses
- Easy control and monitoring via 2-wire fast I2C bus

7.3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD_1V0}	DC supply voltage	-0.1, +1.1	V
V_{DD_2V5}	DC supply voltage	-0.25, +2.75	V
V_{DD_3V35}	DC supply voltage	-0.5, +3.63	
V_{IN_D}	Voltage on digital input pins	-0.3, $V_{DD_}$3V3 + 0.3	V
V_{IN_A}	Voltage on analog input pins	0.3, $V_{DD_}$2V5 + 0.3	V
T_{OPER}	Operating ambient temperature	0, +70	°C
T_{STG}	Storage temperature	-40, +150	°C
Tj	Junction temperature	+125	°C

7.4. Pinning

Pad num	Name	Type	Drive
1	GPIO9	digital	2mA
2	GPIO8	digital	2mA
3	TDI	digital	2mA
4	TDO	digital	2mA
5	TRST	digital	2mA
6	TCK	digital	2mA
7	TMS	digital	2mA
8	GPIO7/AUX_CLK	digital	2mA
9	N_RESET	digital	2mA
10	VDD	dig. supply	
11	GND	dig. supply	
12	VDD_IO_3V3	dig. supply 3.3v	
13	GPIO6/CS0	digital	2mA
14	GPIO5/CS1	digital	2mA
15	SDA	digital	2mA
16	SCL	digital	2mA
17	M_CKOUT	digital	4mA
18	M_SYNC	digital	2mA
19	M_VALID	digital	4mA
20	M_ERR	digital	2mA
21	TS_DATA[0]	digital	4mA
22	TS_DATA[1]	digital	2mA
23	TS_DATA[2]	digital	2mA
24	TS_DATA[3]	digital	2mA
25	VDD	dig. supply	
26	GND	dig. supply	
27	VDD_IO_3V3	dig. supply 3.3v	
28	TS_DATA[4]	digital	2mA
29	TS_DATA[5]	digital	2mA
30	TS_DATA[6]	digital	2mA
31	TS_DATA[7]	digital	4mA
32	GPIO4/SDAT	digital	2mA

Pad num	Name	Type	Drive
33	GPIO3/SCLT	digital	2mA
34	GPIO2	digital	2mA
35	GPIO1/AGC1	digital	2mA
36	GPIO0/AGC2	digital	2mA
37	VDD	dig. supply	
38	GND	dig. supply	
39	VDD_IO_3V3	dig. supply 3.3v	
40	GNDAS_AD	analog gnd	
41	INM	analog	
42	INP	analog	
43	VCCAISO_D	anal. 2.5v supply	
44	INCM	analog	
45	REFM	analog	
46	REFP	analog	
47	GNDA_AD12	analog ground	
48	VCCA_AD12	analog supply	
49	GNDD_AD12	analog ground	
50	VCCD_AD12	anal. 1.0v supply	
51	GNDA_PLL	analog ground	
52	VCCA_PLL	anal. 2.5v supply	
53	GNDD_PLL	analog ground	
54	VCCD_PLL	anal.1.0v supply	
55	ZO		
56	VCCA_OSC	anal. 2.5v supply	
57	A		
58	GNDA_OSC	analog ground	
59	VBASE		
60	VDD10REG		
61	VDD	dig. supply	
62	GND	dig. supply	
63	VDD_IO_3V3	dig. supply 3.3v	
64	CLK_TST	digital	4mA

8. HY5DV281622DT-5 DDR SDRAM 128M

8.1. General Description

The Hynix HY5DV281622 is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the point-to-point applications which requires high bandwidth. The Hynix 8Mx16 DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data,Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

8.2. Features

- 3.3V for VDD and 2.5V for VDDQ power supply
- All inputs and outputs are compatible with SSTL_2 interface
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has 2 bytewide data strobes (LDQS, UDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- Data(DQ) and Write masks(DM) latched on the both rising and falling edges of the data strobe
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Write mask byte controls by LDM and UDM
- Programmable /CAS latency 3 / 4 supported
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal 4 bank operations with single pulsed /RAS
- tRAS Lock-Out function supported
- Auto refresh and self refresh supported
- 4096 refresh cycles / 32ms
- Full, Half and Matched Impedance(Weak) strength driver option controlled by EMRS

8.3. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	^{o}C
Storage Temperature	TSTG	-55 ~ 125	^{o}C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	^{o}C · sec

8.4. Pinning

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied.
/CS	Input	Chip Select : Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
LDM, UDM	Input	Input Data Mask: DM(LDM,UDM) is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
LDQS, UDQS	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ0 ~ DQ15	I/O	Data input / output pin : Data Bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

9. IS42S16100C1 SDRAM

9.1. General Description

*I*SSI's 16Mb Synchronous DRAM IS42S16100C1 is organized as a 524,288-word x 16-bit x 2-bank for improved performance. The synchronous DRAMs achieve high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input.

9.2. Features

- Clock frequency: 200, 166, 143 MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Two banks can be operated simultaneously and independently

- Dual internal bank controlled by A11 (bank select)
- Single 3.3V power supply
- LVTTL interface
- Programmable burst length (1, 2, 4, 8, full page)
- Programmable burst sequence:Sequential/Interleave
- 4096 refresh cycles every 64 ms
- Random column address every clock cycle
- Programmable CAS latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Byte controlled by LDQM and UDQM
- Industrial temperature up to 143 MHz
- Packages 400-mil 50-pin TSOP-II, 60-ball fBGA
- Lead-free package option

9.3. Pinning

A0-A11	Address Input
A0-A10	Row Address Input
A11	Bank Select Address
A0-A7	Column Address Input
DQ0 to DQ15	Data DQ
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command

$\overline{CAS}$	Column Address Strobe Command
$\overline{WE}$	Write Enable
LDQM	Lower Bye, Input/Output Mask
UDQM	Upper Bye, Input/Output Mask
VDD	Power
GND	Ground
VDDQ	Power Supply for DQ Pin
GNDQ	Ground for DQ Pin
NC	No Connection

10. SAW FILTER

10.1. IF Filter for Audio Applications – Epcos K9656M

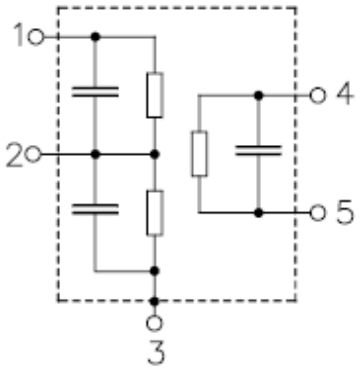
10.1.1. Standart:

- B/G
- D/K
- I
- L/L’

10.1.2. Features:

- TV IF audio filter with two channels
- Channel 1 (L’) with one pass band for sound carriers at 40,40 MHz (L’) and 39,75 MHz (L’- NICAM)
- Channel 2 (B/G,D/K,L,I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

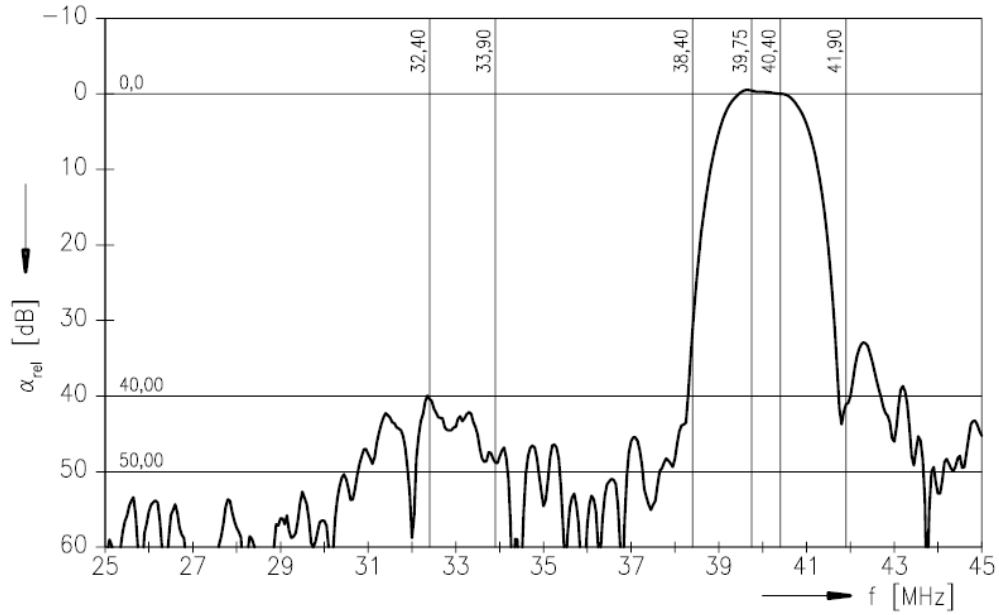
10.1.3. Pin configuration:



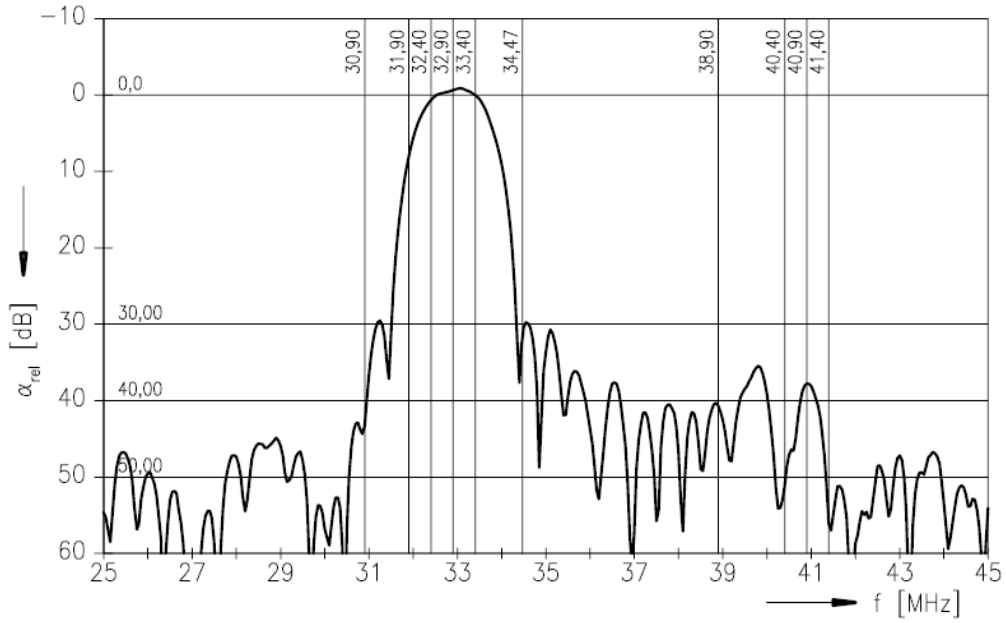
1 Input
2 Switching input
3 Chip carrier - ground
4 Output
5 Output

10.1.4. Frequency response:

Frequency response of channel 1



Frequency response of channel 2



10.2. IF Filter for Video Applications – Epcos K3958M

10.2.1. Standart:

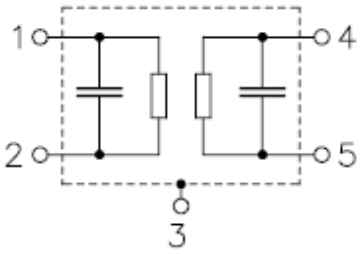
- B/G
- D/K
- I
- L/L’

10.2.2. Features:

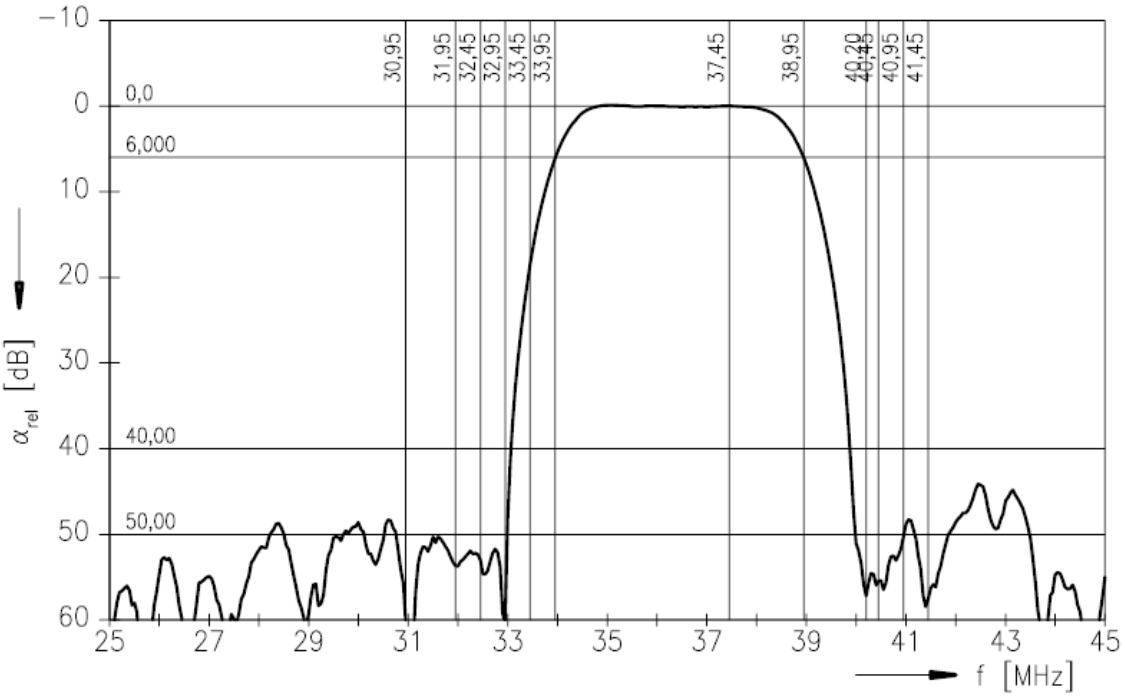
- TV IF filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

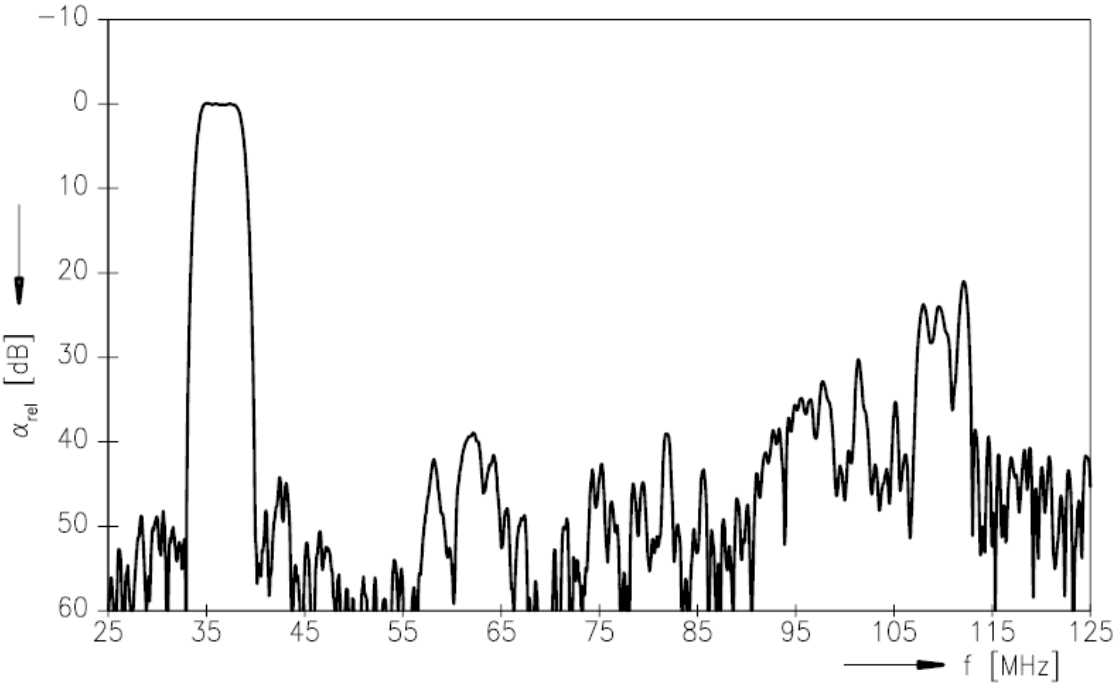
Pin configuration:

1 Input
2 Input - ground
3 Chip - carrier ground
4 Output
5 Output



10.2.3. Frequency response:





11. 2048-Bits Serial EEPROM – 24LC02

11.1. General Description

The 24LC01/02 is a 1K/2K-bit serial read/write non-volatile memory device using the CMOS floating gate process. Its 1024/2048 bits of memory are organized into 128/256 words and each word is 8 bits. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. Up to eight HT24LC01/02 devices may be connected to the same two-wire bus. The HT24LC01/02 is guaranteed for 1M erase/write cycles and 40-year data retention.

11.2. Features

- Operating voltage: 2.4V~5.5V
- Low power consumption
- Operation: 5mA max.
- Standby: 5mA max.
- Internal organization
- 1K (HT24LC01):128´8
- 2K (HT24LC02): 256´8
- 2-wire serial interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Partial page write allowed
- 8-byte Page write modes
- Write operation with built-in timer
- Hardware controlled write protection

- 40-year data retention
- 106 erase/write cycles per word
- 8-pin DIP/SOP package
- 8-pin TSSOP (HT24LC02 only)
- Commerical temperature range (0°C to +70°C)

11.3. Electrical Specifications

DC Electrical Characteristics (Vcc =2.7~5.5V, Ta = 25ºC)

Symbol	Parameter	Conditions	24LC02		Units
			Min	Max	
I_{CC1}	Operating Current (Program)	SCL = 100KHz CMOS Input Levels	—	3	mA
I_{CC2}	Operating Current (Read)	SCL = 100KHz CMOS Input Levels	—	200	µA
I_{SB1}	Standby Current	SCL=SDA=0V, Vcc=5V	—	10	µA
I_{SB2}	Standby Current	SCL=SDA=0V, Vcc=3V	—	1	
I_{IL}	Input Leakage	VIN = 0 V to VCC	-1	+1	µA
I_{OL}	Output Leakage	VOUT = 0 V to Vcc	-1	+1	µA
V_{IL}	Input Low Voltage**		-0.1	Vcc x 0.3	V
V_{IH}	Input High Voltage**		Vcc x 0.7	V_{CC}+ 0.2	V
V_{OL1}	Output Low Voltage	IOL = 2.1mA TTL	—	0.4	V
V_{OL2}	Output Low Voltage	IOL = 10uA CMOS	—	0.2	V
V_{LK}	VCC Lockout Voltage	Programming Command Can Be Executed	Default	—	V

AC Electrical Characteristics (Vcc =2.7~5.5V)

Parameter	Symbol	24LC02		Units
		Min	Max	
Clock frequency	Fscl	0	100	kHz
Clock high time	Thigh	4000	—	ns
Clock low time	Tlow	4700	—	ns
SDA and SCL rise time**	Tr	—	1000	ns
SDA and SCL fall time**	Tf	—	300	ns
START condition hold time	Thd:Sta	4000	—	ns
START condition setup time	Tsu:Sta	4700	—	ns
Data input hold time	Thd:Dat	0	—	ns
Data input setup time	Tsu:Dat	250	—	ns
STOP condition setup time	Tsu:Sto	4000	—	ns
Output valid from clock	Taa	300	3500	ns
Bus free time **	Tbuf	4700	—	ns
Data out hold time	Tdh	300	—	ns
Write cycle time	Twr	—	10	ms
5V, 25ºC, Byte Mode	Endurance**	1M	—	write cycles

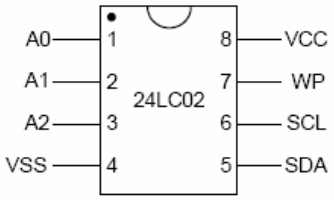
Capacitance TA= 25°C , f=250KHz

Symbol	Parameter	Max	Units
C_{OUT}	Output capacitance	5	pF
C_{IN}	Input capacitance	5	pF

A.C. Conditions of Test

Input Pulse Levels	Vcc x 0.1 to Vcc x 0.9
Input Rise and Fall times	10 ns
Input and Output Timming level	Vcc x 0.5
Output Load	1 TTL Gate and CL = 100pf

11.4. Pinning



PDIP/SOP/TSSOP

A0, A1, A2	Address Inputs
VSS	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
VCC	Power Input

12. 32K Smart Serial EEPROM – 24C32

12.1. General Description

The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24C32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

12.2. Features

- Voltage operating range: 4.5V to 5.5V
- Peak write current 3 mA at 5.5V
- Maximum read current 150 µA at 5.5V
- Standby current 1 µA typical
- Industry standard two-wire bus protocol, I2C compatible
- Including 100 kHz and 400 kHz modes

- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance: 10,000,000 Erase/Write cycles guaranteed for High Endurance Block, 1,000,000 E/W cycles guaranteed for Standard Endurance Block
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges: Commercial (C): 0°C to +70°C, Industrial (I): -40°C to +85°C

11.3 Absolute Maximum Ratings and Electrical Characteristics

VCC 7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins .....≥ 4 kV

DC CHARACTERISTICS

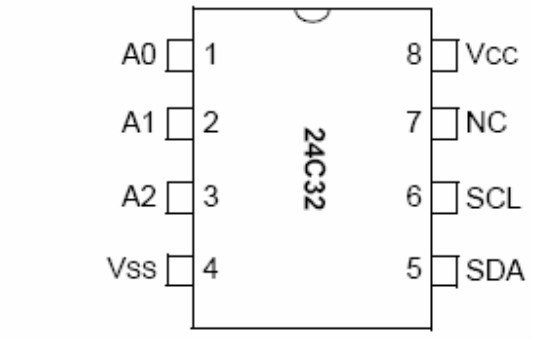
					VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V TO VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE ICC Read	— —	3 150	mA µA	VCC = 5.5V, SCL = 400 kHz VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.5V, SCL = SDA = VCC A0, A1, A2 = VSS

AC CHARACTERISTICS

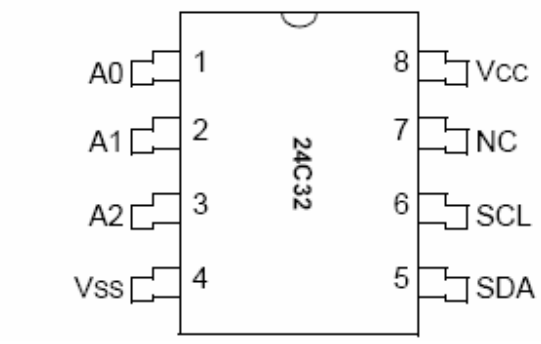
Parameter	Symbol	STD. MODE		FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms/page	(Note 4)
Endurance High Endurance Block Rest of Array	 — —	 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 5)

11.4 Pinning

PDIP



SOIC



Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

13. 512K CMOS Serial Flash – MX25L512

13.1. General Description

The MX25L512 is a CMOS 524,288 bit serial Flash memory, which is configured as 65,536 x 8 internally. The MX25L512 feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input. The MX25L512 provide sequential read operation on whole chip. After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on page (256 bytes) basis, and erase command is executes on chip or sector (4K-bytes). To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit. When the device is not in operation and CS# is high, it is put in standby mode and draws less than 10uA DC current. The MX25L512 utilize MXIC's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

13.2. Features

GENERAL

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 524,288 x 1 bit structure
- 16 Equal Sectors with 4K byte each
- Any Sector can be erased individually
- Single Power Supply Operation
- 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

PERFORMANCE

- High Performance
- Fast access time: 85MHz serial clock (15pF + 1TTL Load) and 66MHz serial clock (30pF + 1TTL Load)
- Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
- Fast erase time: 60ms(typ.) and 120ms(max.)/sector (4K-byte per sector) ; 1s(typ.) and 2s(max.)/chip(512Kb)
- Low Power Consumption
- Low active read current: 12mA(max.) at 85MHz, 8mA(max.) at 66MHz and 4mA(max.) at 33MHz
- Low active programming current: 15mA (max.)
- Low active erase current: 15mA (max.)
- Low standby current: 10uA (max.)
- Deep power-down mode 1uA (typical)
- Minimum 100,000 erase/program cycles

SOFTWARE FEATURES

- Input Data Format
- 1-byte Command code
- Block Lock protection
- The BP0~BP1 status bit defines the size of the area to be software protected against Program and Erase instructions.
- Auto Erase and Auto Program Algorithm
- Automatically erases and verifies data at selected sector
- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
- JEDEC 2-byte Device ID
- RES command, 1-byte Device ID

HARDWARE FEATURES

- SCLK Input
- Serial clock input
- SI Input
- Serial Data Input
- SO Output
- Serial Data Output
- WP# pin
- Hardware write protection
- HOLD# pin pause the chip without diselecting the chip
- PACKAGE
- 8-pin SOP (150mil)
- All Pb-free devices are RoHS Compliant

11.3 Absolute Maximum Ratings

Supply voltage range	V_P		1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω				
V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max.	70	mV
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	µV
Stereo application				
Output power at R_L = 32 Ω				
d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	µV

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig.1		
Storage temperature range	T_{stg}	–55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration			
at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig.4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\|\Delta V\|$	–	–	70	mV
Input impedance (at R_S = ∞)	$\|Z_i\|$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig.5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\|Z_i\|$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

14. Integrated DVB-T Receiver

13.1 General Description

CT216T is a highly integrated single chip for DVB-T compliant STB solution. Compared with Cheertek's previous generations of STB receiver devices. CT216T further interates COFDM demodulator USB 2.0 HS host controller, memory card reader, 1/2-bit SPIFlash interface, audio DAC, PWM in/out and SAR-ADC functions. In additiont special enhangements are provided such as MPEG-4 video decoding, 16-bit OSD with anti-

flickering, HW JPEG decoding, flesh tone and black-white extensions, and improvement of small video quality.

CT216T includes COFDM demodulator transport stream de-multiplexer, DVB-CSA compliant de-scrambler, RISC MPUs, MPEG-1/2/4 AV decoder, digital TV encoder, audio DACs, USB 2.0 HS host controller, memory card reader, smart card reader, CI controller and other peripherals.

Cli216T is designed in focus on the market of single tuner input product which makes, it a cost effective solution. Supports include free to air, conditional access for SC (Smart card) and CI portable devices, PVR, LCD TV, and other DVB-T applications.

13.2 Features

COFDM Demodulator

- ETSI EN 300 744 DVB-T NorDig Unified 1.0.3, and D-book compliant
- Automatic spectral inversion, detection
- Integrated ADC
- Direct IF (36.167 MHz or 43.75 MHz) or low IF (4.57 MHz) supported
- Single IF AGC or dual RF/IF AGC controls with ΔΣ modulabon
- Impulsive noise cancellation
- Carrier acquisition range: ±400 kHz (extensible to ±600 kHz in 8MHz BW)
- Adjacent channel interference (ACI) filter,for supporting 6, 7, and 8MHz channels with one 8MHz analog filter
- Co-channel interterence (CCI) supression
- RF signal strength monitor

MPU

- Three 32-bit RISC MPU run up to 166MHz with total 448DMIPS
- 8KB I-Cache and 8KB D-Cache
- Two general purpose timers
- Watchdog timer
- DSU for source level debug

Memory

- 6-bit SDRAM controller supports up to 32MB (16MB for l28-pin)
- Unified memory architecture
- Parallel flash (216-pin only)
- 1/2-bit SPI flash

Transport De-multiplexing

- TS, PES, and ES demultiplexing
- OneTS path
- CI CAM interface (216-pin only)
- 32 general purpose PID filters
- 32 Section filters
- CRC-32 accelerator

- DVB-CSA de-scramblers

Video Decoding and Processing
- MPEG-2 MP@ML
- MPEG-4 SP&ASP
- PAL/NTSC format conversion
- 3:2 pull down
- Zoom in/out from 1/16X to 16X
- HW JPEG decode
- 4/8/16-bit OSD with anti-flickering
- On chip NTSC/PAL TV encoder
- CVBS, S-VHS, and component video
- VBI insertion for Teletext, CC and WSS
- ITU-R BT.601 and ITU-R BT.656 outputs
- Flesh tone extension
- Black/white extension,

Audio Decoding and Processing
- MPEG-1: layer 1/2/3
- MPEG-2: layer 1/2
- Decode MPEG-2 and MPEG-1 audio at sampling frequency of 16K, 22.05K, 24K, 32K, 44.1K, and 48KHz
- Decode CU-DA at sampling frequency of 44.1 KHz
- SPDIF out for AC-3 by-pass
- Embedded 2 channels audio DAC for L/R outputs
- Digital mute control and volume adjustment

OSD(On Screen Display)
- There are total 9 display planes: border; background. video. RS1 (Rectangle Strip 1), RS2, OSD, RS3, RS4, and cursor.
- 4/8l16-bit OSD with anti-flickering and anti-flutter
- Support alpha-blending per color
- Adjustable brightness control in window
- Bitmap OSD
- Support horizontal pixel duplication to enlarge bitmap automatically
- Support sub-region redraw to facilitate bitmap display.

Digitnal TV Encoder
- NTSC-M, PAL-B, D, G, H, I, Nc, M encoding
- Four video DACs to provide 6 configuration output: modes
- Support CVBS, S-VHS. and component video outs
- VBI insertion for Teletext, CC and WSS
- Color burst amplitude control
- Programmable sync. level
- On chip, color-bar generator

High Speed I/O

- USB 2.0 HS host controller
- Memory card reader with SD, MMC, and MS interfaces
- Compliant with SD spec. 1.1 and MMC spec. 4.0 with 1-bit & 4-bit modes.
- Compliant with Memory Stick Pro format spec. 1.02 and Memory stick format spec 1.43 with 1-bit and 4-bit modes.

Peripherals

- Up to 3 full duplex UART with 16-byte FIFO
- 2-wire serial (2WS) in master mode .. .
- Up to 2 IS0-7816 compliant SC (1 in 128-pin, can also be used as UART)
- 5 digits 7-Segrnent LED control
- 5x3 two-dimension key scan
- 2 SAR-ADC input
- 4 PWM input/output
- 1 HW IR command decode
- GPIO

Electrical and Physical Characteristics

- Capable of using single 27MHz clock input crystal
- 1.8V and 3.3V dual power supply
- Power standby mode
- PQFP-128 (CT216T-Z) or LQFP-216 (CT216T-R) package

13.3 Absolute Maximum Rating and Electrical Characteristics

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VDD18, USB_AVD18	DC power supply	1.62	1.98	V
VDD33, AVD33 VCCA, USB_AVD33 PLL_AVD33	DC power supply	3.0	3.6	V
V_{IN}	Input Voltage	VSS-0.3	5.5	V
I_{IN}	Input Current	-10	+10	mA
T_A	Ambient Operating Temperature	0	70	°C
T_{STG}	Storage Temperature	-55	+150	°C
T_{ESD}	ESD Protection (HBM)	-	2000	V

7.2 DC Characteristics

VDD33-VSS=3.3V±10%, VDD18-VSS=1.8V±10%, T_A=25° C, MCLK=64MHz

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PLL_AVD33	Analogue power supply for clock generator		3.0	3.3	3.6	V
VCCA, AVD33 USB_AVD33	Analogue power supply for ADC & DAC		3.0	3.3	3.6	V
VDD33-VSS	Digital power supply for IO buffers		3.0	3.3	3.6	V
VDD18-VSS	Digital power supply for core		1.62	1.8	1.98	V
I_{DD18}	Operating Current @1.8V			TBD		mA
I_{DD33}	Operating Current @3.3V			TBD		mA
I_{DDPLL}	Operating Current of PLL			1		mA
I_{DDDAC}	Operating Current of DAC per channel			40		mA
I_{STBY}	Standby Current	Standby. All DAC are off.		TBD		mA
I_{LK}	Input Leakage		-10		+10	uA
V_{OL}	Output Voltage Low				0.4	V
V_{OH}	Output Voltage High		2.4			V
V_{IH}	Input Voltage High		2.0		5.5	V
V_{IL}	Input Voltage Low		-0.3		0.8	V

15. IC DESCRIPTIONS

15.1. LM1117

15.1.1. General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to as-sure output voltage accuracy to within ±1%. The LM1117 series is available in SOT- 223, TO-220, and TO-252 D-PAK packages. A minimum of 10μF tantalum capacitor is required at the output to improve the transient response and stability.

15.1.2. Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

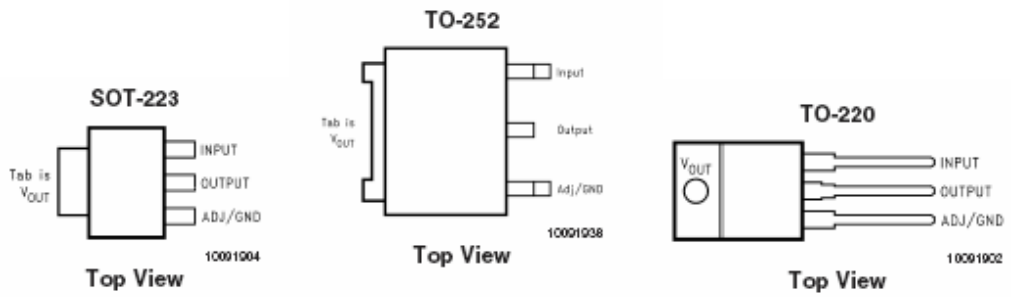
15.1.3. Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators 15
- 32" TFT TV Service Manual 10/01/2005
- Battery Charger
- Battery Powered Instrumentation

15.1.4. Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Input Voltage	V_{IN}		7	V
Lead Temperature (Soldering, 5 Seconds)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	−65	150	℃
Operating Junction Temperature Range	T_{OPR}	0	125	℃

15.1.5. Pinning



15.2. 74HCT4053

15.2.1. General Description

The 74HC4053; 74HCT4053 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4053B. It is specified in compliance with JEDEC standard no. 7A. The 74HC4053; 74HCT4053 is triple 2-channel analog multiplexer/demultiplexer with a common enable input (E). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 and nY1), a common input/output (nZ) and three digital select inputs (Sn). With E LOW, one of the two switches is selected (low-impedance ON-state) by S1 to S3. With E HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. VCC and GND are the supply voltage pins for the digital control inputs (S1 to S3 and E). The VCC to GND ranges are 2.0 V to 10.0 V for 74HC4053 and 4.5 V to 5.5 V for 74HCT4053. The analog inputs/outputs (nY0 and nY1, and nZ) can swing between VCC as a positive limit and VEE as a negative limit. VCC - VEE may not exceed 10.0 V. For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).

15.2.2. Features

- Low ON resistance:
- 80 W (typical) at VCC - VEE = 4.5 V
- 70 W (typical) at VCC - VEE = 6.0 V
- 60 W (typical) at VCC - VEE = 9.0 V
- Logic level translation:
- To enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built in
- Complies with JEDEC standard no. 7A
- ESD protection: HBM EIA/JESD22-A114-C exceeds 2000 V, MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

15.2.3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

15.2.4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{SK}	switch clamping current	$V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V	-	±20	mA

Symbol	Parameter	Conditions		Min	Max	Unit
I_S	switch current	-0.5 V < V_S < V_{CC} + 0.5 V		-	±25	mA
I_{EE}	negative supply current			-	−20	mA
I_{CC}	quiescent supply current			-	50	mA
I_{GND}	ground current			-	−50	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to + 125 °C				
	DIP16 package		[2]	-	750	mW
	SO16 package		[3]	-	500	mW
	SSOP16 package		[4]	-	500	mW
	TSSOP16 package		[4]	-	500	mW
	DHVQFN16 package		[5]	-	500	mW
P_S	power dissipation per switch			-	100	mW

15.2.5. Pinning

Symbol	Pin	Description
2Y1	1	2 independent input/output 1
2Y0	2	2 independent input/output 0
3Y1	3	3 independent input/output 1
3Z	4	3 common input/output
3Y0	5	3 independent input/output 0
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	negative supply voltage
GND	8	ground (0 V)
S3	9	select input 3
S2	10	select input 2
S1	11	select input 1
1Y0	12	1 independent input/output 0
1Y1	13	1 independent input/output 1
1Z	14	1 common input/output
2Z	15	2 common input/output
V_{CC}	16	supply voltage

15.3. NUP4004M5

15.3.1. General Description

This 5-Pin bi-directional transient suppressor array is designed for applications requiring transient overvoltage protection capability. It is intended for use in transient voltage and

ESD sensitive equipment such as computers, printers, cell phones, medical equipment, and other applications. Its integrated design provides bi-directional protection for four separate lines using a single TSOP-5 package. This device is ideal for situations where board space is a premium.

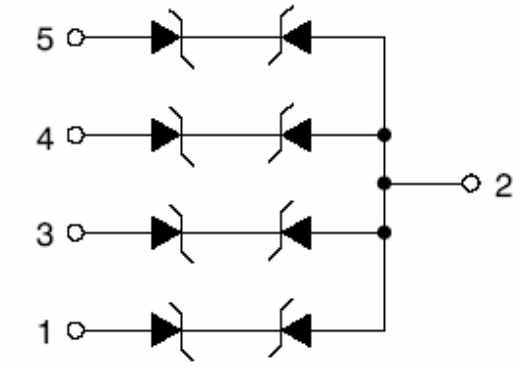
15.3.2. Features

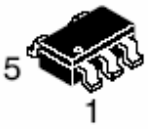
- Bi-directional Protection for Four Lines in a Single TSOP-5 Package
- Low Leakage Current
- Low Capacitance
- Provides ESD Protection for JEDEC Standards JESD22
- Machine Model = Class C
- Human Body Model = Class 3B
- Provides ESD Protection for IEC 61000-4-2, 15 kV (Air), 8 kV (Contact)
- This is a Pb-Free Device

15.3.3. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Lead Solder Temperature – Maximum (10 sec)	T_L	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000−4−2 Air (ESD) IEC 61000−4−2 Contact (ESD)	ESD	16 0.4 30 30	kV

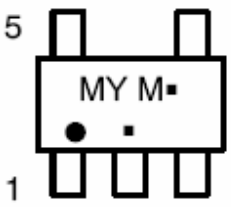
15.3.4. Pinning





TSOP−5
CASE 483

MARKING DIAGRAM



15.4. FDN336P

15.4.1. General Description

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits.This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

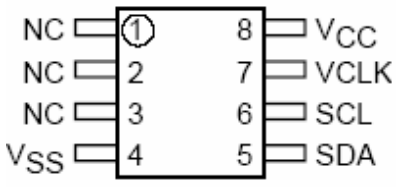
15.4.2. Features

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2.5V to 5.5V SINGLE SUPPLY VOLTAGE
- 400k Hz COMPATIBILITY OVER the FULL RANGE of SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE I2C BUS COMPATIBLE
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

15.4.3. Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1	0 to 70	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

15.4.4. Pinning



SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode

15.5. TL062 -

15.5.1. General Description

Low-power JFET-input operational amplifier

15.5.2. Features

- Very Low Power Consumption
- Typical Supply Current . . . 200 µA (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes VCC+
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/µs Typ

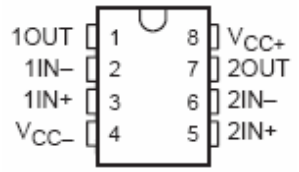
15.5.3. Absolute Maximum Ratings

		TL06_C TL06_AC TL06_BC	TL06_I	TL06_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		–18	–18	–18	V
Differential input voltage, V_{ID} (see Note 2)		±30	±30	±30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Package thermal impedance, θ_{JA} (see Notes 5 and 6)	D (8-pin) package	97	97		°C/W
	D (14-pin) package	86	86		
	N package	80	80		
	NS package	76	76		
	P package	85	85		
	PS package	95	95		
	PW (8-pin) package	149	149		
	PW (14-pin) package	113	113		
Package thermal impedance, θ_{JC} (see Notes 7 and 8)	FK package			5.61	°C/W
	J package			15.05	
	JG package			14.5	
	W package			14.65	
Operating virtual junction temperature, T_J		150	150	150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package			300	°C
Lead temperature 1,6 mm (1/6 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package	260	260		°C
Storage temperature range, T_{stg}		–65 to 150	–65 to 150	–65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

15.5.4. Pinning



15.6. PI5V330

15.6.1. General Description

Pericom Semiconductor.s PI5V series of mixed signal video circuits are produced in the Company.s advanced CMOS low-power technology, achieving industry leading performance. The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch. can be driven from a current output RAMDAC or voltage output composite video source. Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation. The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

15.6.2. Features

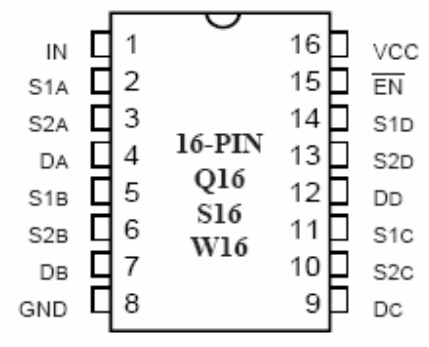
- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: .58 dB
- Ultra-low quiescent power (0.1 µA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
- 16-pin 300-mil wide plastic SOIC (S)
- 16-pin 150-mil wide plastic SOIC (W)
- 16-pin 150-mil wide plastic QSOP (Q)

15.6.3. Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

15.6.4. Pinning



Pin Name	Description
$S1_A$, $S2_A$ $S1_B$, $S2_B$ $S1_C$, $S2_C$ $S1_D$, $S2_D$	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
D_A, D_B, D_C, D_D	Analog Video I/O
GND	Ground
V_{CC}	Power

15.7. AZC099-04S

15.7.1. General Description

AZC099-04S is a high performance and low cost design which includes surge rated diode arrays to protect high speed data interfaces. The AZC099-04S family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZC099-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZC099-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

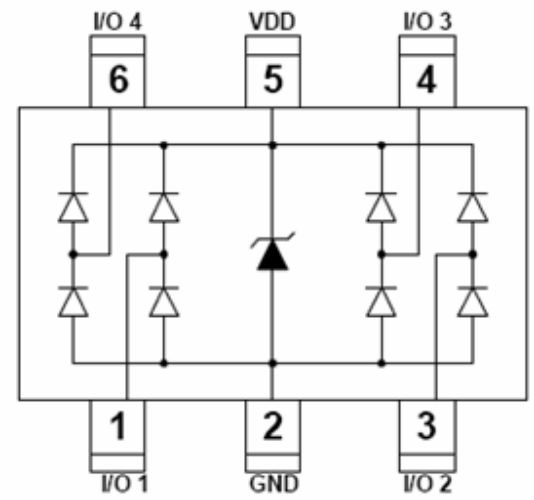
15.7.2. Features

- ESD Protect for 4 high-speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) (5/50ns) Level-3, 20A for I/O, 40A for Power IEC 61000-4-5 (Lightning) 4A (8/20μs)
- 5V operating voltage □□ Low capacitance : 1.0pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology

15.7.3. Absolute Maximum Ratings

PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I_{PP}	5.5	A
Operating Supply Voltage (VDD-GND)	V_{DC}	6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	V

15.7.4. Pinning



15.8. TDA1308

15.8.1. General Description

The TDA1308; TDA1308A is an integrated class-AB stereo headphone driver contained in an SO8, DIP8 or a TSSOP8 plastic package. The TDA1308AUK is available in an 8 bump wafer level chip-size package (WLCSP8). The device is fabricated in a 1 mm Complementary Metal Oxide Semiconductor (CMOS) process and has been primarily developed for portable digital audio applications. The difference between the TDA1308 and the TDA1308A is that the TDA1308A can be used at low supply voltages.

15.8.2. Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
- High signal-to-noise ratio

- High slew rate
- Low distortion
- Large output voltage swing

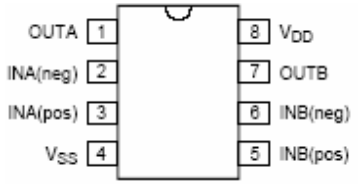
15.8.3. Absolute Maximum Ratings

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			0	8.0	V
$t_{SC(O)}$	output short-circuit duration	T_{amb} = 25 °C; P_{tot} = 1 W		20	-	s
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
V_{esd}	electrostatic discharge voltage	HBM	[1]	−2	+2	kV
		MM	[2]	−200	+200	V

[1] Human body model (HBM): C = 100 pF; R = 1500 Ω; 3 pulses positive plus 3 pulses negative.

[2] Machine model (MM): C = 200 pF; L = 0.5 mH; R = 0 Ω; 3 pulses positive plus 3 pulses negative.

15.8.4. Pinning



Symbol	Pin	Description
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B

15.9. ST3222

15.9.1. General Description

The ST3222 is a 3V powered EIA/TIA-232 and V.28/V.24 communications interface with low power requirements and high data-rate capabilities. ST3222 has a proprietary low dropout transmitter output stage providing true RS-232 performance from 3 to 3.6V power supplies. The device requires only four small 0.1mF standard external capacitors for operating from 3V supply. The ST3222 has two receivers and two drivers. The ST3222 features a 1mA shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers can remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1mA supply current. The device is guaranteed to run at data rates of 250Kbps while maintaining RS-232 output levels.

15.9.2. Features

- 300mA SUPPLY CURRENT
- 250Kbps MINIMUM GUARENTEED DATA RATE
- 6V/ms MINIMUM GUARANTEED SLEW RATE
- MEET EIA/TIA-232 SPECIFICATIONS DOWN TO 3V
- AVAILABLE IN SO-18 AND TSSOP20

15.9.3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to 6	V
V+	Doubled Voltage Terminal	(V_{CC} - 0.3) to 7	V
V-	Inverted Voltage Terminal	0.3 to -7	V
V+ +|V-|		13	V
T_{IN}	Transmitter Input Voltage Range	-0.3 to 6	V
$\overline{SHDN}$	Transmitter Input Voltage Range	-0.3 to 6	V
R_{IN}	Receiver Input Voltage Range	± 25	V
T_{OUT}	Transmitter Output Voltage Range	± 13.2	V
R_{OUT}	Receiver Output Voltage Range	-0.3 to (V_{CC} + 0.3)	V
t_{SHORT}	Transmitter Output Short to GND Time	Continuous	

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied. V+ and V- can have a maximum magnitude of +7V, but their absolute addition can not exceed 13 V.

15.9.4. Pinning

PIN N° (SO-18)	PIN N° (TSSP20)	SYMBOL	NAME AND FUNCTION
1	1	EN	Receiver Enable Control. Drive low for normal operation. Drive high to force the receivers outputs (R_OUT) into a high-impedance state.
2	2	C_1+	Positive Terminal for the first Charge Pump Capacitor
3	3	V+	5.5V Generated By The Charge Pump.
4	4	C_1-	Negative Terminal for the first Charge Pump Capacitor
5	5	C_2+	Positive Terminal for the second Charge Pump Capacitor
6	6	C_2-	Negative Terminal for the second Charge Pump Capacitor
7	7	V-	-5.5V Generated By The Charge Pump.
8	8	$T2_{OUT}$	Second Transmitter Output Voltage
9	9	$R2_{IN}$	Second Receiver Input Voltage
10	10	$R2_{OUT}$	Second Receiver Output Voltage
	11	NC	Not Connected
11	12	$T2_{IN}$	Second Transmitter Input Voltage
12	13	$T1_{IN}$	First Transmitter Input Voltage
	14	NC	Not Connected
13	15	$R1_{OUT}$	First Receiver Output Voltage
14	16	$R1_{IN}$	First Receiver Input Voltage
15	17	$T1_{OUT}$	First Transmitter Output Voltage
16	18	GND	Ground
17	19	V_{CC}	Supply Voltage
18	20	SHDN	Active Low Shutdown Control Input. Drive Low To Shut-down Trnasmittes And Charge Pump

15.10. LM358D

15.10.1. General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a

single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies. The LM358 and LM2904 are available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology.

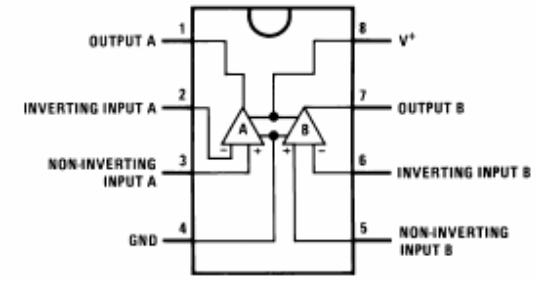
15.10.2. Features

- Available in 8-Bump micro SMD chip sized package,
- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply: Single supply: 3V to 32V or dual supplies: ±1.5V to ±16V
- Low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing

15.10.3. Absolute Maximum Ratings

	LM158/LM258/LM358 **LM158A/LM258A/LM358A**
Supply Voltage, V^+	32V
Differential Input Voltage	32V
Input Voltage	–0.3V to +32V
Power Dissipation (Note 1)	
Molded DIP	830 mW
Metal Can	550 mW
Small Outline Package (M)	530 mW
micro SMD	435mW
Output Short-Circuit to GND	
(One Amplifier) (Note 2)	
$V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA
Operating Temperature Range	
LM358	0°C to +70°C
LM258	–25°C to +85°C
LM158	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature, DIP	
(Soldering, 10 seconds)	260°C
Lead Temperature, Metal Can	
(Soldering, 10 seconds)	300°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods surface mount devices.	
ESD Tolerance (Note 10)	250V

15.10.4. Pinning



15.11. 74LCX244

15.11.1. General Description

The LCX244 contains eight non-inverting buffers with 3-STATE outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX244 is designed for low voltage (2.5V or 3.3V) VCC applications with capability of interfacing to a 5V signal environment. The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

15.11.2. Features

- 5V tolerant inputs and outputs
- 2.3V to 3.6V VCC specifications provided
- 6.5ns Tpd max. (VCC=3.3V), 10µA ICCmax.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- ±24mA output drive (VCC=3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance:Human body model>2000V, Machine model>200V
- Leadless DQFN package

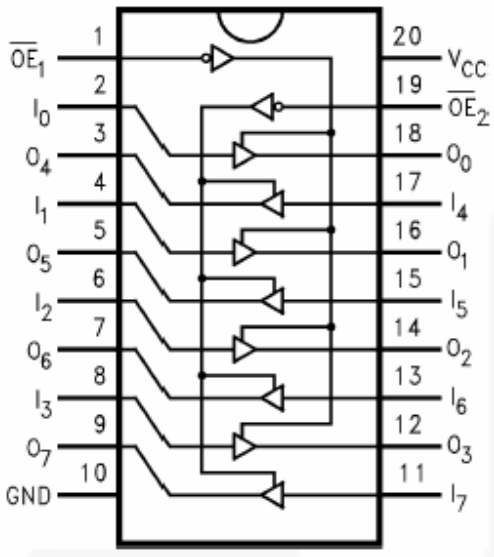
15.11.3. Absolute Maximum Ratings

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State(3)	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

3. I_O Absolute Maximum Rating must be observed.

15.11.4. Pinning



Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

15.12. 74LCX245

15.12.1. General Description

The LCX245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) VCC applications with capability of interfacing to a 5V signal environment. The T/R input determines the direction of data flow through the device. The OE input disables both the A and B ports by placing them in a high impedance state.
The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

15.12.2. Features

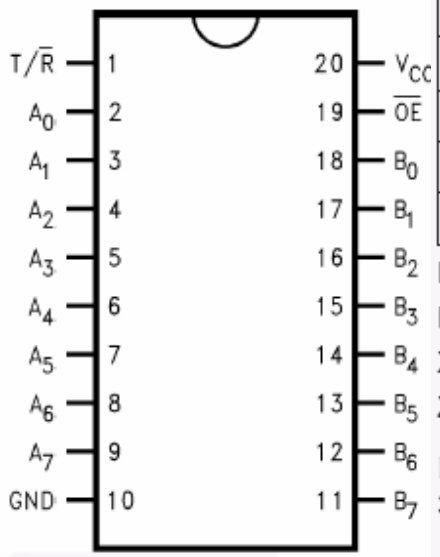
- 5V tolerant inputs and outputs
- 2.3V to 3.6V VCC specifications provided
- 7.0ns tPDmax. (VCC=3.3V), 10µA ICCmax.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- ±24mA output drive (VCC=3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance: Human body model>2000V, Machine model>200V
- Leadless DQFN package

15.12.3. Absolute Maximum Ratings

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State(4)	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:
4. I_O Absolute Maximum Rating must be observed.

15.12.4. Pinning



Inputs		Outputs
OE	T/$\overline{R}$	
L	L	Bus B_0 – B_7 Data to Bus A_0 – A_7
L	H	Bus A_0 – A_7 Data to Bus B_0 – B_7
H	X	HIGH Z State on A_0 – A_7, B_0 – B_7(3)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Note:
3. Unused bus terminals during HIGH Z State must be held HIGH or LOW.

15.13. FSA3157

15.13.1. General Description

The NC7SB3157 / FSA3157 is a high-performance, single- pole / double-throw (SPDT) analog switch or 2:1 multiplexer/ de-multiplexer bus switch. The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-beforemake select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V VCC operating range.

The control input tolerates voltages up to 5.5V, independent of the VCC operating range.

15.13.2. Features

- Useful in both analog and digital applications
- Space-saving, SC70 6-lead surface mount package
- Ultra-small, MicroPak™ Pb-free leadless package
- Low On Resistance: <10Ω on typical at 3.3V VCC
- Broad VCC operating range: 1.65V to 5.5V
- Rail-to-rail signal handling
- Power-down, high-impedance control input
- Over-voltage tolerance of control input to 7.0V
- Break-before-make enable circuitry
- 250 MHz, 3dB bandwidth

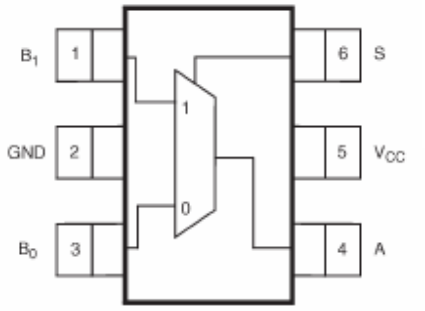
15.13.3. Absolute Maximum Ratings

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_S	DC Switch Voltage(1)	–0.5V to V_{CC} +0.5V
V_{IN}	DC Input Voltage(1)	–0.5V to +7.0V
I_{IK}	DC Input Diode Current at V_{IN} < 0V	–50mA
I_{OUT}	DC Output Current	128mA
I_{CC}/I_{GND}	DC V_{CC} or Ground Current	±100mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
T_J	Junction Temperature Under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation at +85°C	180mW
ESD	Electrostatic Discharge, Human Body Model	4000V

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

15.13.4. Pinning



Pin Names	Description
A, B_0, B_1	Data Ports
S	Control Input

15.14. FMS6145

15.14.1. General Description

The FMS6145 Low-Cost Video Filter (LCVF) is intended to replace passive LC fi lters and drivers with a low-cost integrated device. Five 4th-order fi lters provide improved image quality compared to typical 2nd or 3rd-order passive solutions. The FMS6145 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required. The outputs can drive AC- or DC-coupled single (150Ω) or dual (75Ω) loads. DC coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output.

15.14.2. Features

- Five 4th-order 8MHz (SD) fi lters
- Drives single,AC- or DC-coupled, video loads (2Vpp, 150Ω)
- Drives dual, AC- or DC-coupled, video loads (2Vpp, 75Ω)
- Transparent input clamping
- AC- or DC-coupled inputs
- AC- or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Robust 8kV ESD protection
- Lead-free TSSOP-14 package

15.14.3. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
Output Channel - Any One Channel (Do Not Exceed)		50	mA

15.14.4. Pinning

Pin #	Name	Type	Description
1	IN1	Input	Video input, channel 1
2	IN2	Input	Video input, channel 2
3	IN3	Input	Video input, channel 3
4	V_{CC}	Input	+5V supply, do not float
5	IN4	Input	Video input, channel 4
6	IN5	Input	Video input, channel 5
7, 8	NC		No Connect
9	OUT5	Output	Filtered video output, channel 5
10	OUT4	Output	Filtered video output, channel 4
11	GND	Output	Must be tied to ground, do not float
12	OUT3	Output	Filtered video output, channel 3
13	OUT2	Output	Filtered video output, channel 2
14	OUT1	Output	Filtered video output, channel 1

15.15. MT48LC4M16A2TG8E

15.15.1. General Description

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 16,777,216-bit banks is organized as 4,096 rows by 1,024 columns by 4 bits. Each of the x8's 16,777,216-bit banks is organized as 4,096 rows by 512 columns by 8 bits. Each of the x16's 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then ollowed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row).

15.15.2. Features

- PC66-, PC100- and PC133-compliant
- 143 MHz, graphical 4 Meg x 16 option
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and AutO Refresh Modes
- Self Refresh Modes: standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

15.15.3. Absolute Maximum Ratings

Voltage on V_{DD}, $V_{DD}Q$ Supply
Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature,
T_A (commercial) ..... 0°C to +70°C
Operating Temperature,
T_A (industrial) ..... -40°C to +85°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W

15.15.4. Pinning

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
16, 17, 18	WE#, CAS#, RAS#	Input	Command Inputs: WE#, CAS# and RAS# (along with CS#) define the command being entered.
39	x4, x8: DQM	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0-DQ7 and DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
15, 39	x16: DQML, DQMH		
20, 21	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
23-26, 29-34, 22, 35	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A9 [x4]; A0-A8 [x8]; A0-A7 [x16]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0-DQ15	x16: I/O	Data Input/Output: Data bus for x16 (4, 7, 10, 13, 42, 45, 48, 51 are NCs for x8; and 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, 53 are NCs for x4).
2, 5, 8, 11, 44, 47, 50, 53	DQ0-DQ7	x8: I/O	Data Input/Output: Data bus for x8 (2, 8, 47, 53 are NCs for x4).
5, 11, 44, 50	DQ0-DQ3	x4: I/O	Data Input/Output: Data bus for x4.
36, 40	NC	–	No Connect: These pins should be left unconnected.
3, 9, 43, 49	VccQ	Supply	DQ Power: Isolated DQ power on the die for improved noise immunity.
6, 12, 46, 52	VssQ	Supply	DQ Ground: Isolated DQ ground on the die for improved noise immunity.
1, 14, 27	Vcc	Supply	Power Supply: +3.3V ±0.3V.
28, 41, 54	Vss	Supply	Ground.

15.16. MP1583

15.16.1. General Description

The MP1583 is a step-down regulator with a built in internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20μA of supply current.

The MP1583 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

15.16.2. Features

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20μA Shutdown Mode
- Fixed 385KHz frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 23V operating Input Range
- Output Adjustable From 1.22 to 21V
- Under Voltage Lockout
- Available in 8 pin SOIC Package
- 3A Evaluation Board Available

15.16.3. Absolute Maximum Ratings

Supply Voltage V_{IN}	-0.3V to 28V
Switch Voltage V_{SW}	-1V to V_{IN}+0.3V
Boost Voltage V_{BS}	V_{SW}-0.3V to V_{SW}+6V
All Other Pins	-0.3V to 6V
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to 150°C

15.16.4. Pinning

#	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side n-channel MOSFET switch. Connect a 4.7nF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. (Note: Connect the exposed pad on backside to Pin 4).
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.222V. See *Setting the Output Voltage*
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See *Compensation*
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. For automatic startup, leave EN unconnected.
8	SS	Soft Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.

15.17. MP2112

15.17.1. General Description

The MP2112 is a 1MHz constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. It is ideal for powering portable equipment that powered by a single cell Lithium-Ion (Li+) battery. The MP2112 can supply 1A of load current from a 2.5V to 6V input voltage. The output voltage can be regulated as low as 0.6V. The MP2112 can also run at 100% duty cycle for low dropout applications.
The MP2112 is available in a space-saving 6-pin QFN package.

15.17.2. Features

- High Efficiency: Up to 95%
- 1MHz Constant Switching Frequency
- 1A Available Load Current
- 2.5V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Current Mode Control
- Short Circuit Protection
- Thermal Fault Protection
- <0.1μA Shutdown Current
- Space Saving 3mm x 3mm QFN6 Package

15.17.3. Absolute Maximum Ratings

V_{IN} to GND ..... –0.3V to +6.5V
V_{SW} to GND..... –0.3V to V_{IN} +0.3V
V_{FB}, V_{EN} to GND..... –0.3V to +6.5V
Junction Temperature.....+150°C
Lead Temperature .....+260°C
Storage Temperature .....–65°C to +150°C

15.17.4. Pinning

Pin #	Name	Description
1	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
2	GND	Ground.
3	SW	Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.
4	VINB	Supply Input-Power.
5	VINA	Supply Input-Analog.
6	EN	Enable Input.

15.18. STLITE49M

15.18.1. General Description

The ST7LITE49M is a member of the ST7 microcontroller family. All ST7 devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set. The ST7LITE49M features FLASH memory with byte-by-byte In-Circuit Programming (ICP) and In-Application Programming (IAP) capability. Under software control, the ST7LITE49M device can be placed in Wait, Slow, or Halt mode, reducing power consumption when the application is in idle or standby state. The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes. The ST7LITE49M features an on-chip Debug Module (DM) to support In-Circuit Debugging (ICD). For a description of the DM registers, refer to the ST7 ICC Protocol Reference Manual.

15.18.2. Features

- Memories: 4 Kbytes single voltage extended Flash (XFlash) Program memory with Read-out protection In-Circuit Programming and In-Application programming (ICP and IAP) Endurance: 10K write/erase cycles guaranteed Data retention: 20 years at 55 °C, 384 bytes RAM, 128 bytes data EEPROM with read-out protection, 300K write/erase cycles guaranteed, data retention: 20 years at 55 °C.
- Clock, Reset and Supply Management: 3-level low voltage supervisor (LVD) for main supply and an auxiliary voltage detector (AVD) for safe power-on/off, Clock sources: Internal trimmable 8 MHz RC oscillator, auto wake-up internal low power, low frequency oscillator, crystal/ceramic resonator or external clock, Five power saving modes: Halt, Active-Halt, Auto Wake-up from Halt, Wait and Slow
- I/O Ports: Up to 24 multifunctional bidirectional I/Os, 8 high sink outputs
- 5 timers: Configurable watchdog timer, Dual 8-bit Lite Timers with prescaler, 1 real time base and 1 input capture, Dual 12-bit Auto-reload Timers with 4 PWM outputs, input capture, output compare, dead-time generation and enhanced one pulse mode functions
- Communication interface: I²C multimaster interface
- A/D converter: 10 input channels
- Interrupt management: 13 interrupt vectors plus TRAP and RESET
- Instruction set: 8-bit data manipulation, 63 basic instructions with illegal opcode detection, 17 main addressing modes, 8 x 8 unsigned multiply instructions
- Development tools: Full HW/SW development package, DM (Debug Module)

15.18.3. Absolute Maximum Ratings

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	7.0	V
V_{IN}	Input voltage on any pin(1)(2)	V_{SS}-0.3 to V_{DD}+0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *Section 13.8.3 on page 156*	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)		

15.18.4. Pinning

Pin Number		Pin Name	Type	Level		Port / Control						Main function (after reset)	Alternate function
						Input				Output			
LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD[1]	PP		
1	5	PA3 (HS)/ATPWM1	I/O	C_T	HS	x	ei0			x	x	Port A3 (HS)	ATPWM1
2	6	PA4 (HS)ATPWM2/MCO	I/O	C_T	HS	x				x	x	Port A4 (HS)	ATPWM2/MCO
3	7	PA5 (HS)ATPWM3	I/O	C_T	HS	x				x	x	Port A5 (HS)	ATPWM3
4	8	PA6 (HS)/I2CDATA	I/O	C_T	HS	x		ei0		T		Port A6 (HS)	I2CDATA
5	9	PA7 (HS)/I2CCLK	I/O	C_T	HS	x				T		Port A7 (HS)	I2CCLK
6	10	RESET					x			x		Reset	
8	12	V_{DD}[2]	S									Digital Supply Voltage	
9	13	V_{SS}[2]	S									Digital Ground Voltage	
10	14	OSC1	I									Resonator oscillator inverter input or External clock input	
11	15	OSC2	O									Resonator oscillator output	
12	16	V_{SSA}[2]	S									Analog Ground Voltage	
13	17	V_{DDA}[2]	S									Analog Supply Voltage	

Pin Number		Pin Name	Type	Level		Port / Control						Main function (after reset)	Alternate function
						Input				Output			
LQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD[1]	PP		
14	18	PB0/AIN0	I/O	C_T		x	ei1		x	x	x	Port B0	AIN0
15	19	PB1/AIN1/CLKIN	I/O	C_T		x			x	x	x	Port B1	AIN1/External clock source
16	20	PB2/AIN2	I/O	C_T		x			x	x	x	Port B2	AIN2
17	21	PB3/AIN3	I/O	C_T		x			x	x	x	Port B3	AIN3
18	22	PB4/AIN4	I/O	C_T		x			x	x	x	Port B4	AIN4
19	23	PB5/AIN5	I/O	C_T		x			x	x	x	Port B5	AIN5
20	24	PB6/AIN6	I/O	C_T		x			x	x	x	Port B6	AIN6
21	25	PB7/AIN7	I/O	C_T		x			x	x	x	Port B7	AIN7
22	26	PC0/AIN8	I/O	C_T		x	ei2		x	x	x	Port C0	AIN8
23	27	PC1/AIN9	I/O	C_T		x			x	x	x	Port C1	AIN9
24	28	PC2/ICCDATA	I/O	C_T		x				x	x	Port C2	ICCDATA
25	29	PC3/ICCCLK	I/O	C_T		x	x			x	x	Port C3	ICCCLK
26	30	PC4/LTIC	I/O	C_T		x	ei2			x	x	Port C4	LTIC
27	31	PC5	I/O	C_T		x				x	x	Port C5	
28	32	PC6	I/O	C_T		x				x	x	Port C6	
29	1	PC7/BREAK	I/O	C_T		x				x	x	Port C7	BREAK
30	2	PA0 (HS)	I/O	C_T	HS	x	ei0			x	x	Port A0 (HS)	
31	3	PA1 (HS)/ATIC	I/O	C_T	HS	x				x	x	Port A1 (HS)	ATIC
32	4	PA2 (HS)/ATPWM0	I/O	C_T	HS	x				x	x	Port A2 (HS)	ATPWM0

1. In the open-drain output column, T defines a true open-drain I/O (P-Buffer and protection diode to V_{DD} are not implemented).
2. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.

15.19. MAX809LTR

15.19.1. General Description

The MAX809 and MAX810 are cost-effective system supervisor circuits designed to monitor VCC in digital systems and provide a reset signal to the host processor when necessary. No external components are required. The reset output is driven active within 10 _sec of VCC falling through the reset voltage threshold. Reset is maintained active for a timeout period which is trimmed by the factory after VCC rises above the reset threshold. The MAX810 has an active-high RESET output while the MAX809 has an active-low RESET output. Both devices are available in SOT-23 and SC-70 packages. The MAX809/810 are optimized to reject fast transient glitches on the VCC line. Low supply current of 0.5 _A (VCC = 3.2 V) makes these devices suitable for battery powered applications.

15.19.2. Features

- Precision VCC Monitor for 1.5 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.2 V to 4.9 V Available in 100 mV Steps
- Four Guaranteed Minimum Power-On Reset Pulse Width Available (1 ms, 20 ms, 100 ms, and 140 ms)
- RESET Output Guaranteed to VCC = 1.0 V.
- Low Supply Current
- Compatible with Hot Plug Applications
- VCC Transient Immunity
- No External Components
- Wide Operating Temperature: -40°C to 105°C
- Pb-Free Packages are Available

15.19.3. Absolute Maximum Ratings

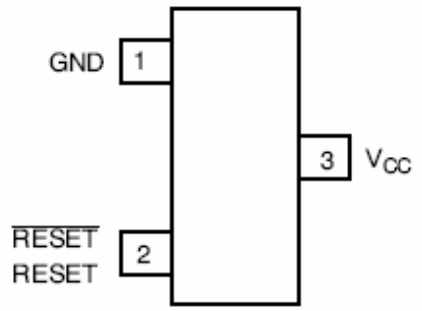
Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} to GND)	V_{CC}	-0.3 to 6.0	V
RESET Output Voltage (CMOS)		-0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}		20	mA
Output Current, $\overline{RESET}$		20	mA
dV/dt (V_{CC})		100	V/μsec
Thermal Resistance, Junction-to-Air (Note 1) SOT-23 SC-70	$R_{\theta JA}$	301 314	°C/W
Operating Junction Temperature Range	T_J	-40 to +105	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{sol}	+260	°C
ESD Protection Human Body Model (HBM): Following Specification JESD22-A114 Machine Model (MM): Following Specification JESD22-A115		 2000 200	V
Latchup Current Maximum Rating: Following Specification JESD78 Class II Positive Negative	$I_{Latchup}$	 200 200	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This based on a 35x35x1.6mm FR4 PCB with 10mm^2 of 1 oz copper traces under natural convention conditions and a single component characterization.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

15.19.4. Pinning



Pin No.	Symbol	Description
1	GND	Ground
2	$\overline{\text{RESET}}$ (MAX809)	$\overline{\text{RESET}}$ output remains low while V_{CC} is below the reset voltage threshold, and for a reset timeout period after V_{CC} rises above reset threshold
2	RESET (MAX810)	RESET output remains high while V_{CC} is below the reset voltage threshold, and for a reset timeout period after V_{CC} rises above reset threshold
3	V_{CC}	Supply Voltage (Typ)

16. SERVICE MENU SETTINGS

In order to reach service menu, First Press **"MENU"** Then press the remote control code, which is **"4725"**. In DTV mode, first press **"MENU**" and select **"TV SETUP"**. Then, press **"4725"**.

16.1. Video Setup

Panel Info <.....>

32_LC_SAC1

Blue Background <.....>

*If "Menu" selected, **"Blue Background"** item is seen in **"Feature"** menu.*

*If "Yes" selected, **"Blue Background"** is on and not seen in **"Feature"** menu*

Film Mode <.....>

*If "Yes" selected, **"**Film Mode**"** feature is active.*

Dynamic Contrast <.....>

*If "Yes" selected, **"**Dynamic Contrast**"** feature is active.*

Game Mode <.....>

*If "Yes" selected, **"**Game Mode**"** feature is active*

SRGB For PC <.....>

If "Yes" selected, PCs can use SRGB option.

Dynamic Noise Reduction<.....>

*If "Yes" selected, **"**Dynamic Noise Reduction**"** feature is active*

WSS Option<.....>

If "Yes" selected, WSS Option can be used

16.2. AudioSetup

BG<.....>

Europe

New Zelland
Australia
No

DK<.....>
I<.....>
L<.....>
Equalizer <.....>
*If "Yes" selected, **"Equalizer"** item is seen in **"Sound"** menu.*
Headphone <.....>
*If "Yes" selected, **"Headphone"** item is seen in **"Sound"** menu.*
Power On/Off Melody <.....>
If "Yes" selected, when power on/off conditions, the power on/off melody can be heard.
Dynamic Bass <.....>*Value between 0 to 12*
Effect<.....> *Value between 0 to 7*
Audio Delay ,offset <.....> *Value between 0 to 190*
Audio Setup Cont...2
Carrier mute<.....> *Value between 0 to 28*
Headphone Sound Select <.....>
Always Active Select
Always Inactive Select
Menu
Always Main Menu
Always PIP/PAP Window
Sound Mode Detect Time <.....> *Value between 0 to 255*
Noise Reduction Threshold <.....> *Value between 0 to 255*
Noise Reduction Time <.....> *Value between 0 to 15*
AVL Attack Time <.....> *Value between 0 to 255*
AVL Release Time <.....> *Value between 0 to 255*
Prescales (AVL On)
FM Prescale<.....> *Value between 0 to 255*
AM Prescale <.....> *Value between 0 to 255*
NICAM Prescale <.....> *Value between 0 to 255*
SCART Prescale <.....> *Value between 0 to 255*
FAV Prescale <.....> *Value between 0 to 255*
DTV Prescale <.....> *Value between 0 to 255*
HDMI Prescale <.....> *Value between 0 to 255*
YPbPr/PC Prescale <.....> *Value between 0 to 255*
An. USB Prescale <.....> *Value between 0 to 255*
Dig. USB Prescale <.....> *Value between 0 to 255*
Prescales (AVL Off)
FM Prescale<.....> *Value between 0 to 255*
AM Prescale <.....> *Value between 0 to 255*
NICAM Prescale <.....> *Value between 0 to 255*
SCART Prescale <.....> *Value between 0 to 255*
FAV Prescale <.....> *Value between 0 to 255*
DTV Prescale <.....> *Value between 0 to 255*
HDMI Prescale <.....> *Value between 0 to 255*
YPbPr/PC Prescale <.....> *Value between 0 to 255*

An. USB Prescale <.....> *Value between 0 to 255*
Dig. USB Prescale <.....> *Value between 0 to 255*

Clipping Levels (AVL On)

FM Clipping <.....> *Value between 0 to 255*
AM Clipping <.....> *Value between 0 to 255*
NICAM Clipping <.....> *Value between 0 to 255*
SCART Clipping <.....> *Value between 0 to 255*
FAV Clipping <.....> *Value between 0 to 255*
DTV Clipping <.....> *Value between 0 to 255*
HDMI Clipping <.....> *Value between 0 to 255*
YPbPr/PC Clipping <.....> *Value between 0 to 255*
An. USB Clipping <.....> *Value between 0 to 255*
Dig. USB Clipping <.....> *Value between 0 to 255*

Clipping Levels (AVL Off)

FM Clipping <.....> *Value between 0 to 255*
AM Clipping <.....> *Value between 0 to 255*
NICAM Clipping <.....> *Value between 0 to 255*
SCART Clipping <.....> *Value between 0 to 255*
FAV Clipping <.....> *Value between 0 to 255*
DTV Clipping <.....> *Value between 0 to 255*
HDMI Clipping <.....> *Value between 0 to 255*
YPbPr/PC Clipping <.....> *Value between 0 to 255*
An. USB Clipping <.....> *Value between 0 to 255*
Dig. USB Clipping <.....> *Value between 0 to 255*

16.3. Service Scan/Tuning Setup

First Search for L/L' <.....>
ATS Delay Time (ms) <.....> *Value between 0 to +200*
Main Tuner Setup

Tuner Type

LC_TDTC_GXX1D
Thomson DTT7543X
Philips TD1318AF-3
Samsung DTOs403LH172A
Generic (Analog Only)

Control Byte <.....> *Value between 0 to +255*
BSW1 <.....> *Value between 0 to +255*
BSW2 <.....> *Value between 0 to +255*
BSW3 <.....> *Value between 0 to +255*
Low-Mid – Low Byte <.....>
Low-Mid – High Byte <.....>
Mid-High – Low Byte <.....>
Mid-High – High Byte <.....>

S Band TOP <.....>
VIF TOP <.....> *Value between 0 to +15*
VIF TOP SECAM <.....> *Value between 0 to +15*
VIF TOP DK<.....> *Value between 0 to +15*
Synch Threshold<.....> *Value between 0 to +40*

16.4. Options

Options-1

Power Up

Standby

Last state

TV Open Mode

Source

1st TV

Last Tv

First APS <.....>

If "Yes" selected, first time TV opens by asking APS.

APS Volume <.....> *Value between 0 to +63*

Burn In Mode <.....>

If "Yes" selected, TV opens with Burn-In mode. This mode is used in manufacturing.

APS Test

Autostore <.....>

If "Yes" selected, Channel is automatically stored.

Unicode Enabled <.....>

If "Yes" selected,Unicode characters can be read in the USB Files.

Options-2

Source List menu <.....>

If "Yes" selected, Sorce List Menu appears on the screen when press "source" button.

RS232 for B2B <.....>

If "Yes" selected, Remote Control commandsthe TV via RS232 and vice versa.

RC Select <.....>

RC Group 1

RC Group 2

RC Group 3

RC Group 4

RC Group 5

RC Group 6

Double Digit Key <.....>

If "Yes" selected, Double Digit Button on RC activates.

Protection <.....>

If "Yes" selected,short circuit protection activates.

Led Type <.....>

1 Led 1 Color

1 Led 2 Color

2 Led 2 Color

1 Led 3 Color

2 Led 3 Color

200 Programme <.....>

If "Yes" selected, totaly 200 programmes can be used.

TouchPad <.....>

If "Yes" selected, TouchPad can be used.

Teletext Options

TXT Darkness <.....> *Value between 0 to +63*

TXT Type <.....>

- ***Fasttext&Toptext***
- ***No***
- ***Default***
- ***Fastext***
- ***Toptext***

TXT Language <.....>

- ***Menu***
- ***West***
- ***East***
- ***Cyrillic***
- ***Turk/Gre***
- ***Arabic***
- ***Persian***
- ***Auto***

No Txt Warning <.....>

If "Yes" selected, "No Txt Transmission" warning appears on the screen when pressing txt button from RC.

Txt Subtitle <.....>

If "Yes" selected, Teletext subtitles can be seen.

Optional Features

Default Zoom <.....>

- ***Menu***
- ***16:9***
- ***4:3***
- ***Panaromic***
- ***14:9 Zoom***

Menu Timeout <.....>

- ***Menu***
- ***15 Sec***
- ***30 Sec***
- ***60 Sec***
- ***No Time***

Backlight <.....>

If "Yes" selected, ***"Backlight"*** *feature is active.*

100 Step Slider <.....>

If "Yes" selected, 64 step sliders will become 100 step sliders.

Analog USB Enabled <.....>

If "Yes" selected, ***"Analog USB"*** *option is active.*

Menu Double Size <.....>

If "Yes" selected, menu sizes increases.

CEC Enable <.....>

If "Yes" selected, ***"CEC"*** *feature is active.*

Digital USB Hotplug <.....>

If "Yes" selected, ***"Digital USB Hotplug"*** *feature is active.*

PIP Options

Pip <.....>

AV PIP

No PIP

PC PIP

Hotel Options <.....>

Hotel TV <.....>

*If "Yes" selected, **"Hotel TV"** feature is active.*

IR Smartloader <.....>

*If "Yes" selected, **"IR Smartloader"** feature is active.*

16.5. External Source Settings

TV <.....>
DTV <.....>
Ext 2 <.....>
Ext 2 S <.....>
FAV <.....>
BAV <.....>
S-Video <.....>
HDMI 1 <.....>
HDMI 2 <.....>
HDMI 3 <.....>
HDMI 4 <.....>
YPbPr <.....>
PC <.....>

16.6. Preset

User Ad.j
ADC Adj.
Service Adj.
All Adj.
Init Factory Channels.

16.7. NVM Edit

NVM-edit addr. (hex)
NVM-edit data (hex)
NVM-data dec

16.8. Programming

HDMI DDC Update Mode <.....>
HDCP Key Update Mode <.....>
Software Bypass <.....>

If "On" selected, speaker effects are bypassed.

LVDS Clock Step <.....> *Value between 0 to +255*
Memory Clock Step <.....> *Value between 0 to +255*
DTV Download <.....>

If "On" selected, DTV software can be updated from SCART.

DSUB9 Download <.....>

If "On" selected, DTV software can be updated from DSUB9.

16.9. Diagnostic

Eeprom I2C
Tuner I2C
IF I2C
HDMI I2C
DTV RS232

16.10. Product Info

17. SOFTWARE UPDATE DESCRIPTION

16.1 17MB35 Analog Part Software Update With Bootloader Procedure

1.1 The File Types Used By The Bootloader

All file types that used by the bootloader software are listed below:

1. The Binary File : It has ".bin" extension and it is the tv application. Its size is 1920 Kb.

2. The Config Binary File : It has ".cin extension and it is the config of the tv application. Its size may be 64 Kb or a few times 64 Kb.

3. The Test Script File : It has ".txt" extension and it is the test script that is parsed and executed by the bootloader. It don't have to be any times of 64 Kb.

4. The Test Binary File : It has ".tin" extension and it is used and written by the test groups. It is run to understand the problem part of the hardware.

Alltough a file that is used by the bootloader can be had any one of these extensions, its name has to be "VESTEL_S" and it has to be located in the root directory of the usb device.

1.2 Usage of The Bootloader

1. The starting to pass through : The chassis is only powered up.
2. The starting to download something : When chassis is powered up the menu key has to be pushed.Before the chassis is powered up and if any usb device is plugged to the usb port, the programme is downloaded from usb firstly.

Any usb device is plugged to usb port , user must open hyperterminal in the pc and connect pc to chassis via Mstar debug tool and any one of scart,dsub9 or I2c connectors. Serial connection settings are listed below:

- Bit per second: 115200
- Data bits: 8

- Parity: None
- Stop bits: 1
- Flow control: None

In this case the bootloader sofware puts “C” character to uart. After repeating “C” characters are seen in the hyperterminal user can send any file to chassis by selecting Transfer -> Send File menu item and choosing “**1K Xmodem**” from protocol section.

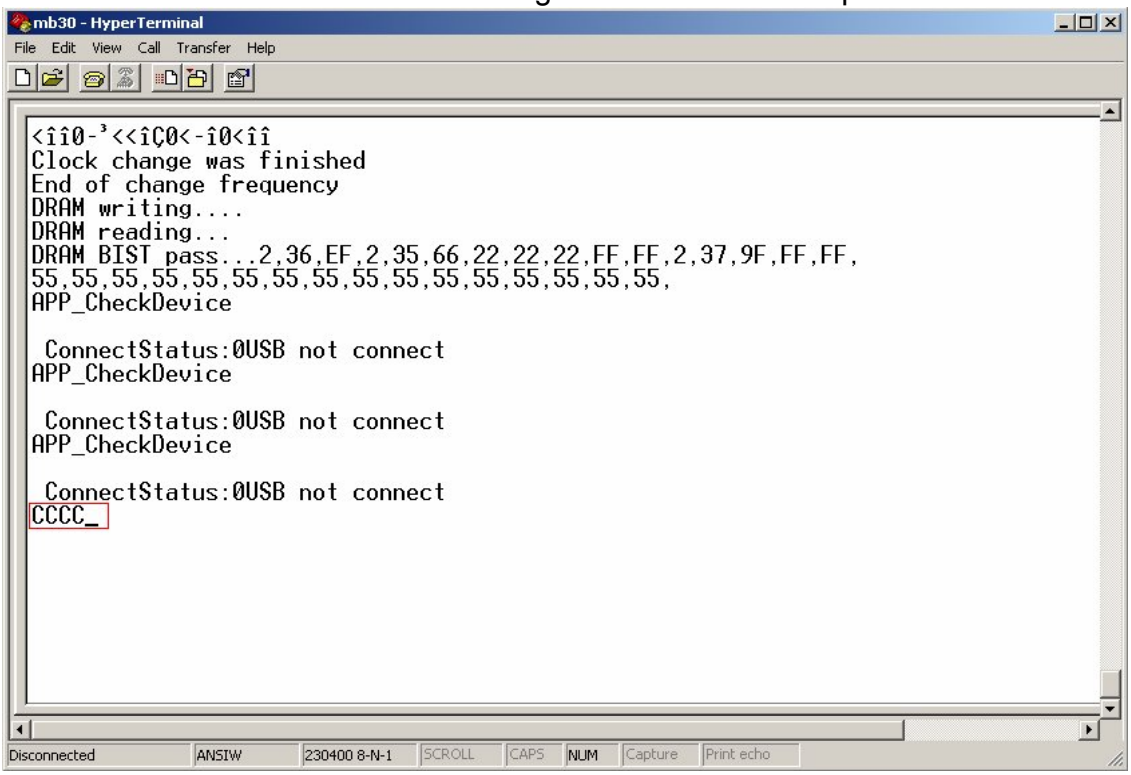


Figure 1. The Sample Output Before Sending The File

2. EEProm update

To Update eeprom content via uart scart,dsub9 or i2c with Mstar tool can used.
Serial connection settings are listed below:

- Bit per second: 9600
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Programming menu item is choosed in the service menu and switch “HDCP Key Update Mode” from off to on.

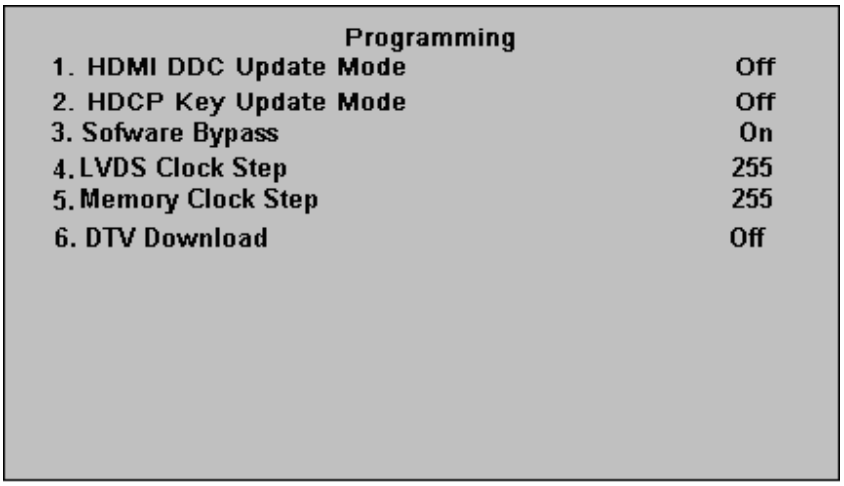


Figure 2. The Programming Service Menu

After then you must see Xmodem menu in the hyperterminal.To download hdcp key press k or to download eeprom content press w.

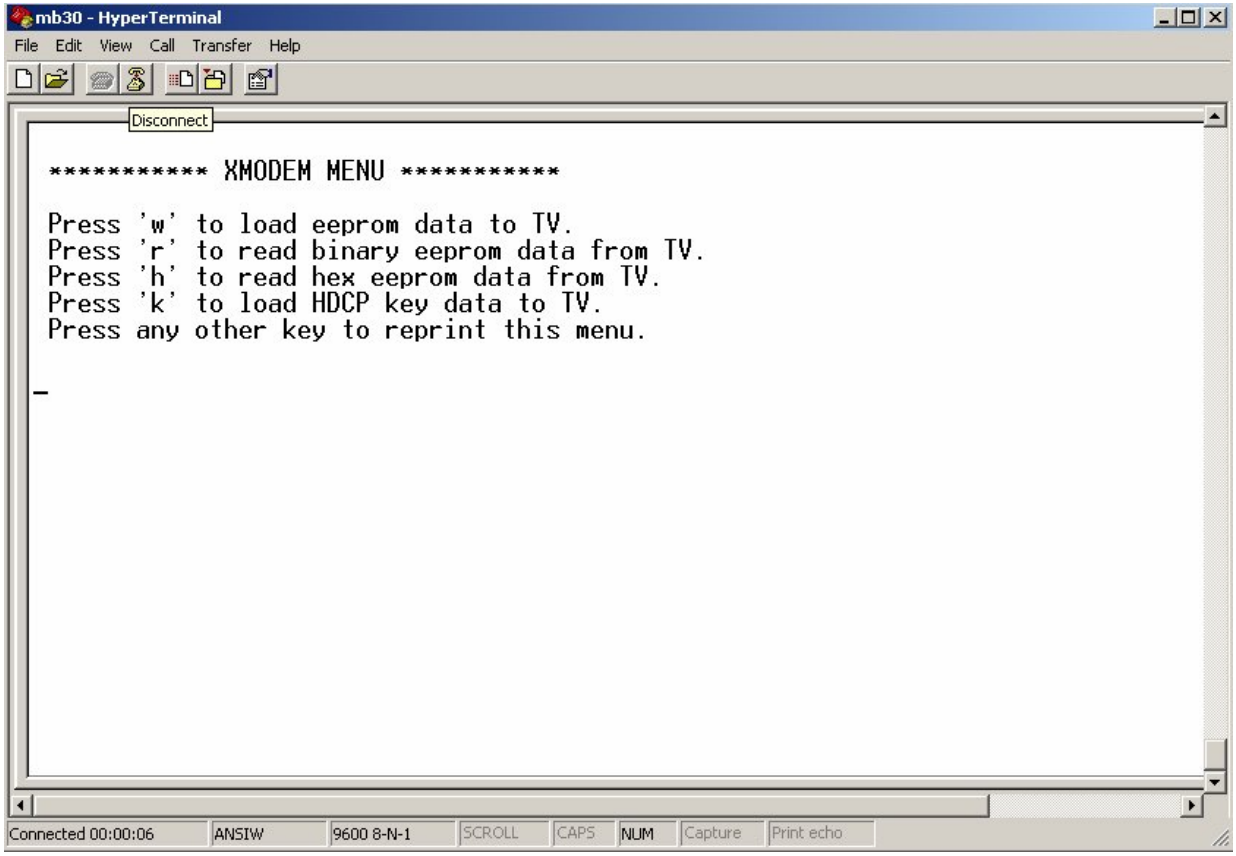


Figure 3. Xmodem Menu

If the repeated “C” characters are seen you can transfer file content via select Transfer->Send File and choose “**Xmodem”** protocol and click the “Send” button.

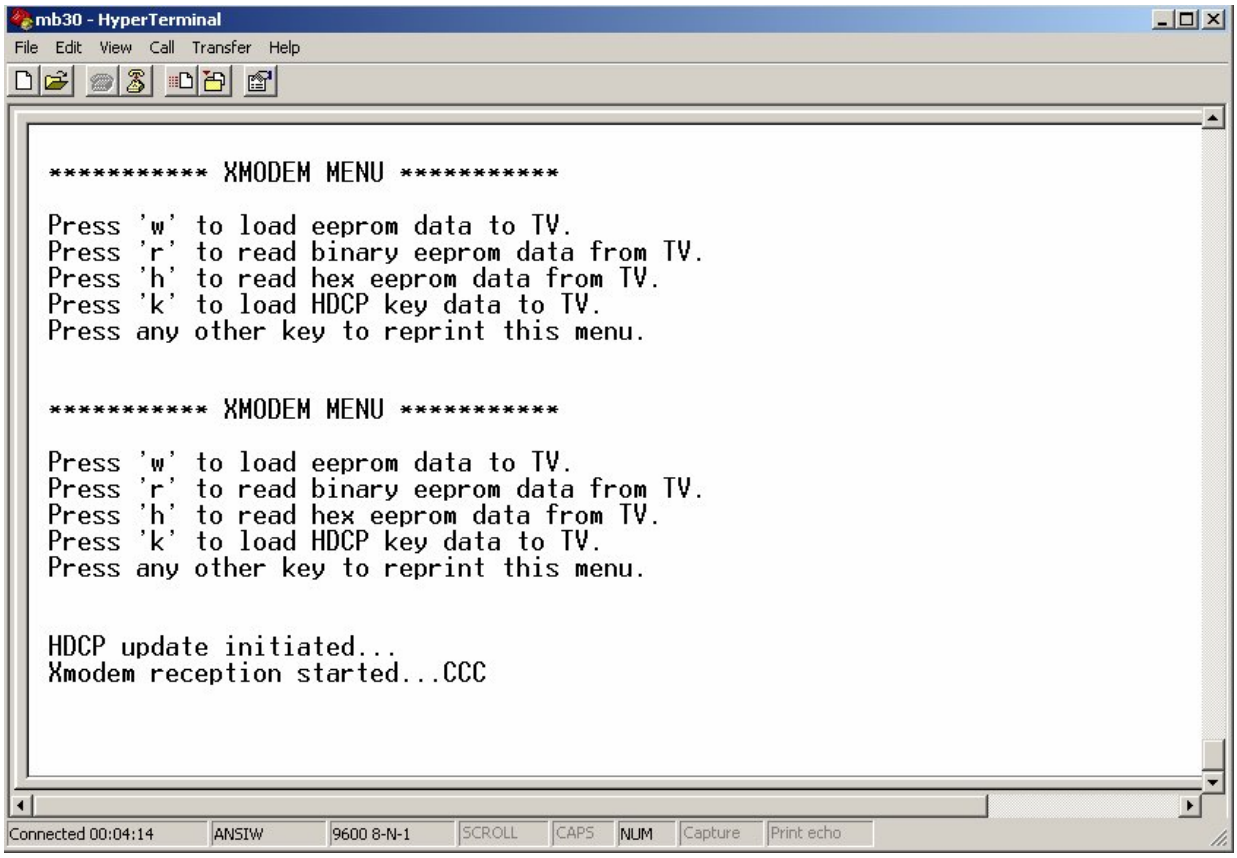


Figure 4. The Starting To Send

16.2 17MB30 HDCP key upload procedure.

1) Turn on TV set.
2) Open a COM connection using fallowing parameters and select ISP COM Port No

Baud Rate: 9600 bps
Data Bits: 8
Stop Bits: 1
Parity: None
Flow Control: None

3) Enter service menu by pressing “4” “7” “2” 5” consecutively while main menu is open
4) Select “9. Programming”
5) Select “HDMI HDCP Update Mode” yes.
6) On Hyper Terminal Window press “k”
7) Click on send file under Transfer Tab.
8) Select Xmodem and choose the HDCP key to be uploaded.
9) Press send button
10) Restart TV set

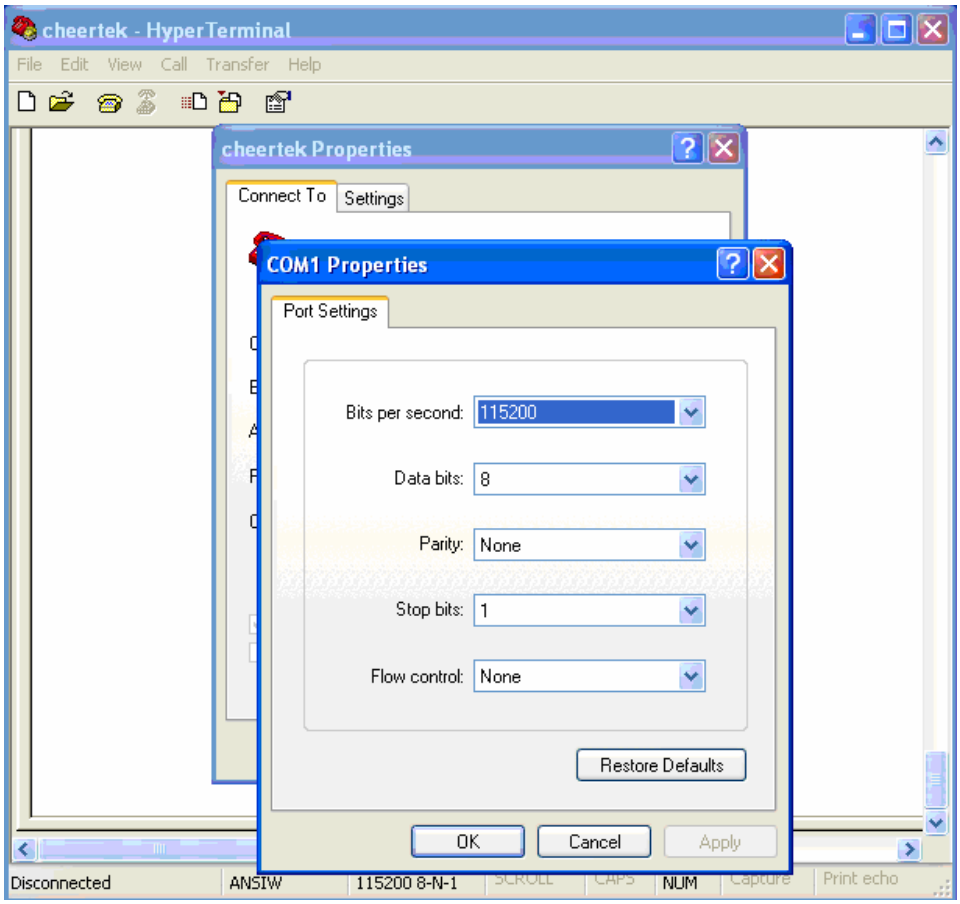
16.3 17MB35 Digital Software Update From SCART

Adjusting DTV Download Mode:

1. Power on the TV.
2. Exit the Stby Mode.
3. Enter the “Tv Menu”.
4. Enter “4725” for jumping to “Service Settings”.
5. Select “8. Programming” step.
6. Change “6. DTV Download” to “On”.
7. Switch to the Stby mode.

Adjusting HyperTerminal:

1. Connect the “MB35 SCART Interface” to SCART1 (bottom SCART plug).
2. Also connect the “MB35 SCART Interface” to PC.
3. Open “HyperTerminal”.
4. Determine the “COM” settings listed and showed below.
   - Bit per second: 115200
   - Data bits: 8
   - Parity: None
   - Stop bits: 1
   - Flow control: None

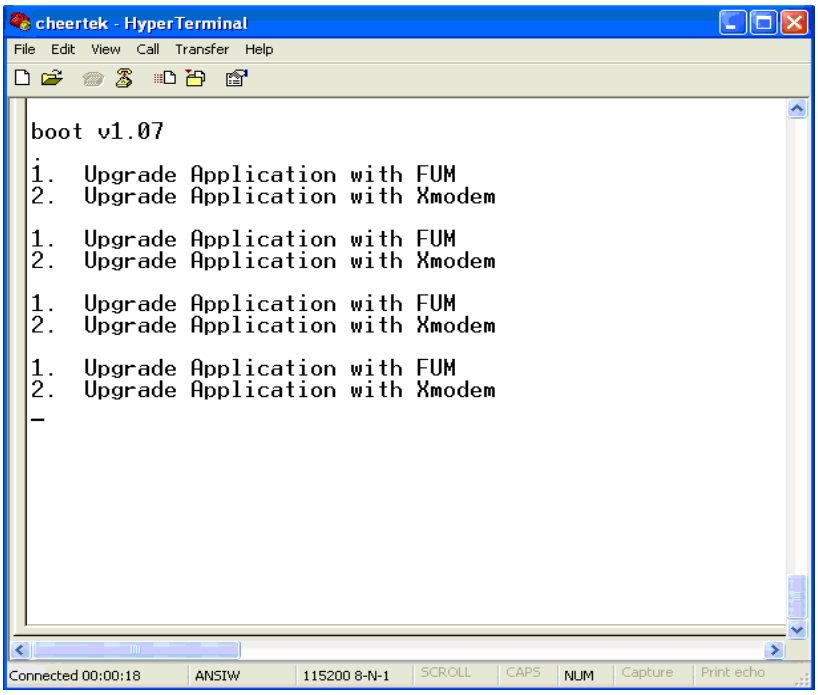


COM Properties Window

6. Click “OK”.

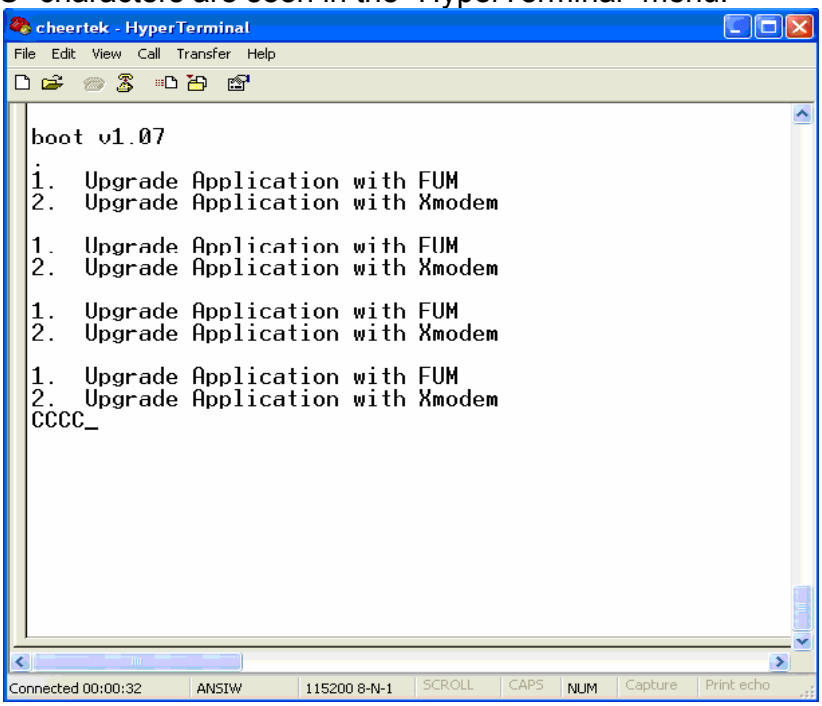
Software Updating Procedure

1. In the HyperTerminal Menu, click the “Connect” button.
2. Exit the Stby Mode.
3. The “Space” button on the keyboard must be pressed, when the following window can be seen.



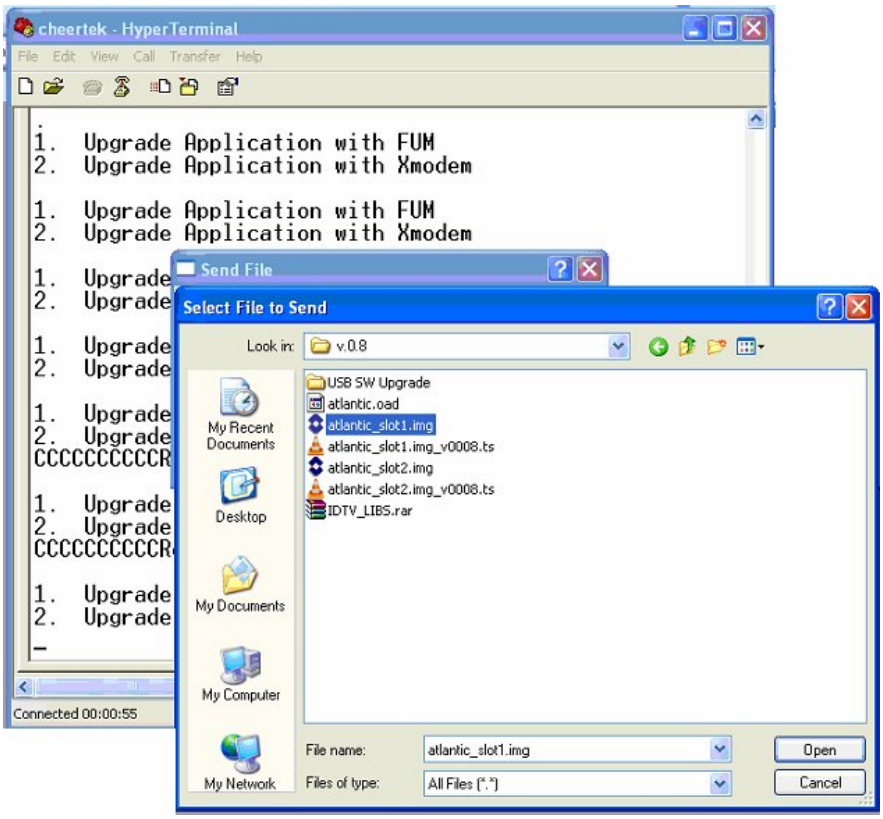
Selection Window

4. Press the “2” button on the keyboard for choosing “2. Upgrade Application with Xmodem”.
5. Repeating “C” characters are seen in the “HyperTerminal” menu.

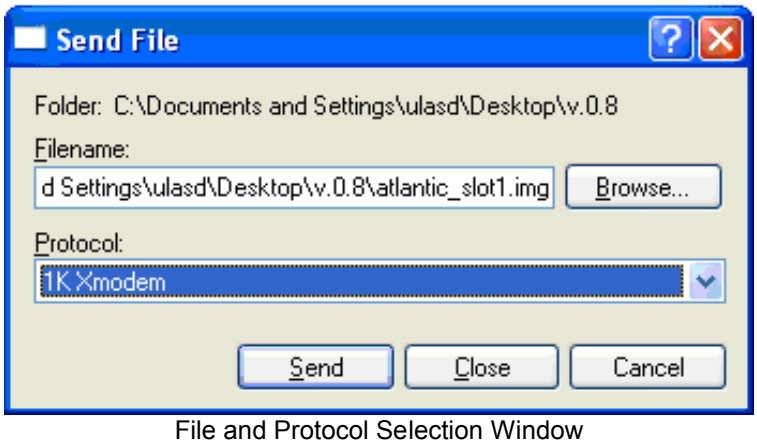


The Sample Output Before Sending The File

6. Click the “Send” button on the HyperTerminal
7. Select the “Filename **xxxx**_slot1.img” using “Browse”.
8. Choose the “1K Xmodem” from “Protocol” option.

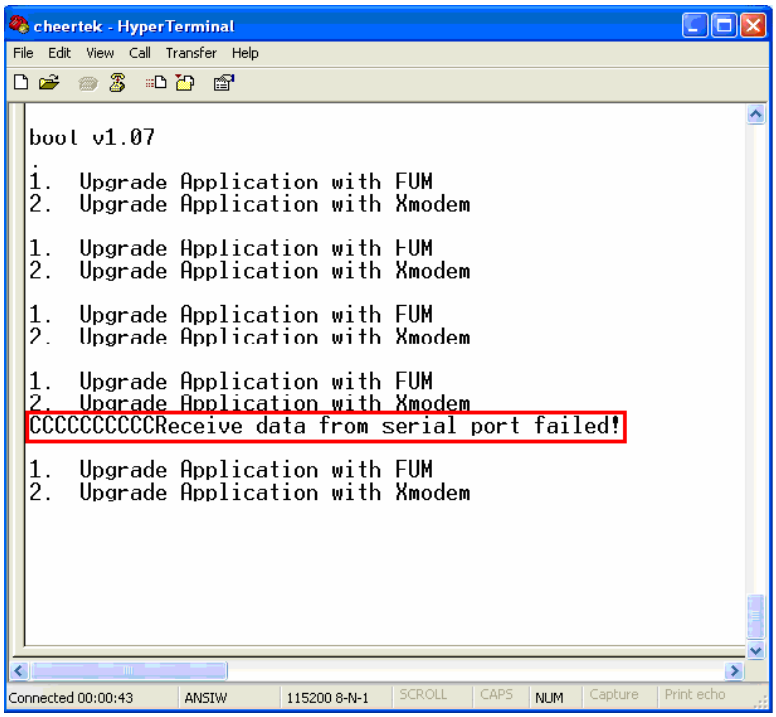


Selection of File



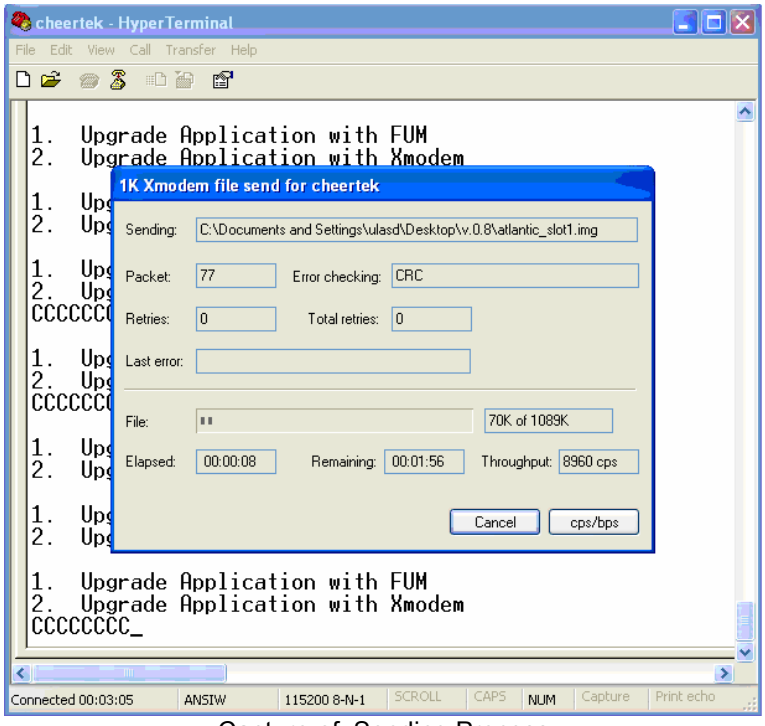
File and Protocol Selection Window

Note: In the Software updating Procedure section, when the first “C” character is seen, the filename selection process must be finished before 10 seconds. If the process can not be finished, the file sending operation will be cancelled. The following figure shows this situation.



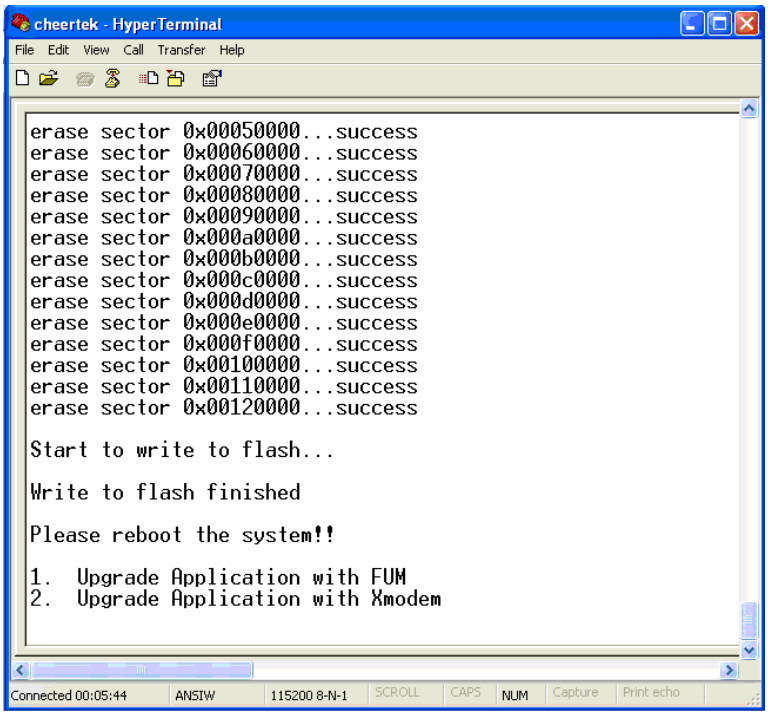
Capture of Receving Data Failing

9. When sending the file the following window must be seen.



Capture of Sending Process

10. After the sending process the following HyperTerminal window must be seen.

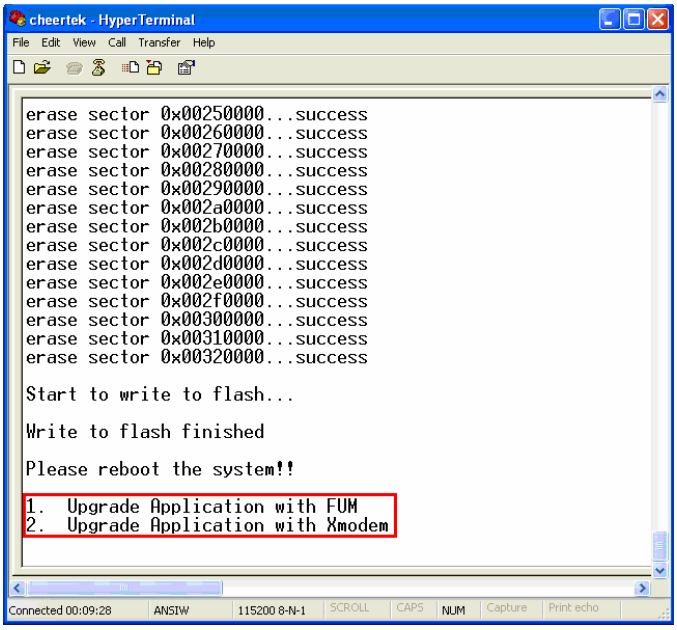


Capture of End of The Sending Process

11. For sending second program file, the Software Updating Procedure must be repeated from the step **X**. Select the “Filename **xxxx**_slot2.img” using “Browse”.
12. After sending the second program file, the Software Updating Procedure will be succesful.

Note: After the File Sending Process,

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem, options must be seen.



End of The Sending Process

Checking Of The New Software
1. Turn off and on the TV.
2. Enter the “Setup” submenu in the “DTV Menu”.
3. Choose the “Configuration” option.
4. For controlling new software, check the “Receiver Upgrade” option.

16.4 17MB35 Digital Software Update From USB

Software upgrade is possible via USB disk by folowing the steps below.

1. Copy the bin file, including higher version than the software loaded in flash, into the USB flash memory root directory. This file should be named up.bin.
2. Insert the USB disk.
3. Digital module performs version and CRC check. If version and CRC check is successful, then a message prompt appears to notify user about new version. If the user confirms loading of new version, upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash and then a system reset is performed.
5. After the reset, digital module starts with new software.

Revert operation:

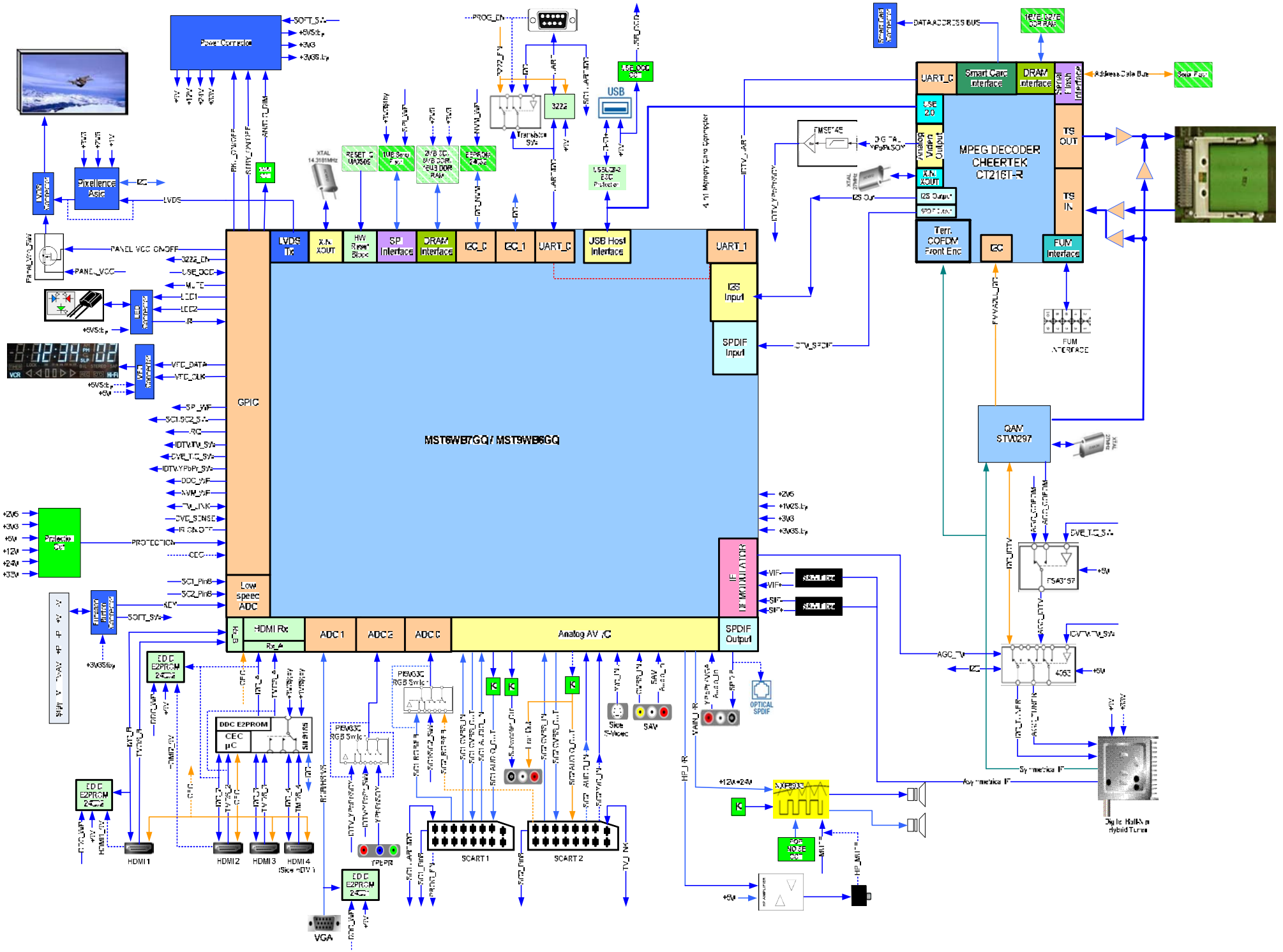
With revert operation, it is possible to *downgrade* the software.
Revert operation is very similar to upgrade process. In the revert operation, file name should be f_up.bin. Also user confirmation is not asked.

1. Copy the bin file into the USB flash memory root directory. This file should be named force_upgrade.bin.
2. Insert the USB disk.
3. A lower version than the software in flash can be loaded with revert operation. Digital module performs only CRC check. If CRC check is successful, then force_upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash.
5. A message prompt is displayed to notify user about end of revert process.
6. Power off/on is required to start digital module with the new software.

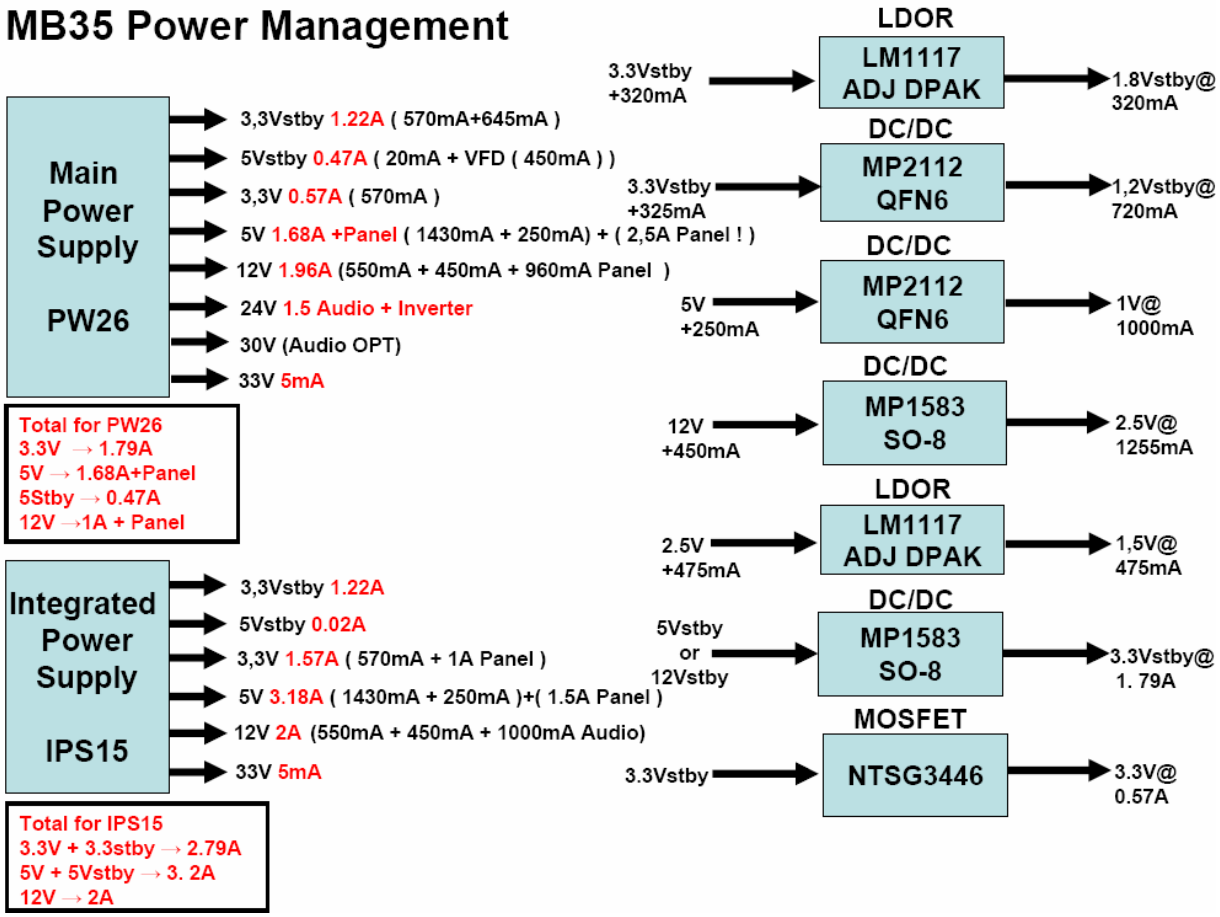
For controlling new software, check the “Receiver Upgrade” option.

18. BLOCK DIAGRAMS

18.1. General Block Diagram

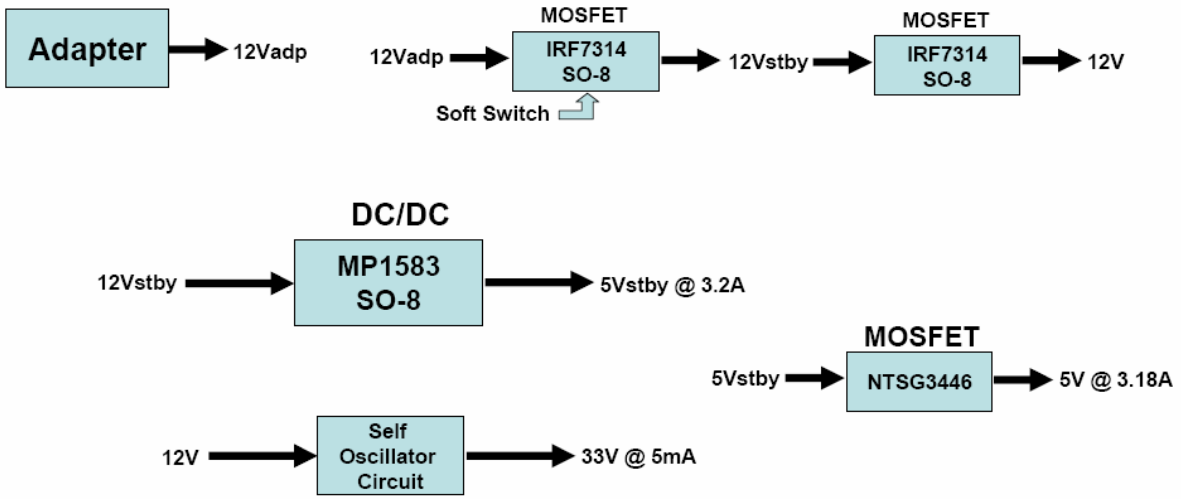

MST6WB7GQ/ MST9WB6GQ
GPIC
Low speed ADC
LVDS Tx
XIN XOUT
HW Reset Block
SPI Interface
DRAM Interface
I2C_0
I2C_1
UART_0
USB Host Interface
UART_1
I2S Input
SPDIF Input
HDMI Rx
ADC 1
ADC 2
ADC 0
Analog AV I/C
SPDIF Output
IF DEMODULATOR
MPEG DECODER CHEERTEK CT2161T-R
UART_0
Smart Card Interface
DRAM Interface
Serial Flash Interface
USB 2.0
Analog Video Output
XIN XOUT
I2S Out
SPDIF Out
TS OUT
TS IN
Terr. COFDM Front End
ISC
FUM Interface
QAM STV0297
Power Connector
Pixelence Asic
USB
3222
Transistor SW
Protection ckt
Audio Amp
HDMI1
HDMI2
HDMI3
HDMI4
VGA
SCART1
SCART2
YPbPr
OPTICAL SPDIF
DDC E2PROM
CEC µC
Side S-Video
SAV
Asymetrical IF
Digital Hybrid Tuner

18.2. Power Management

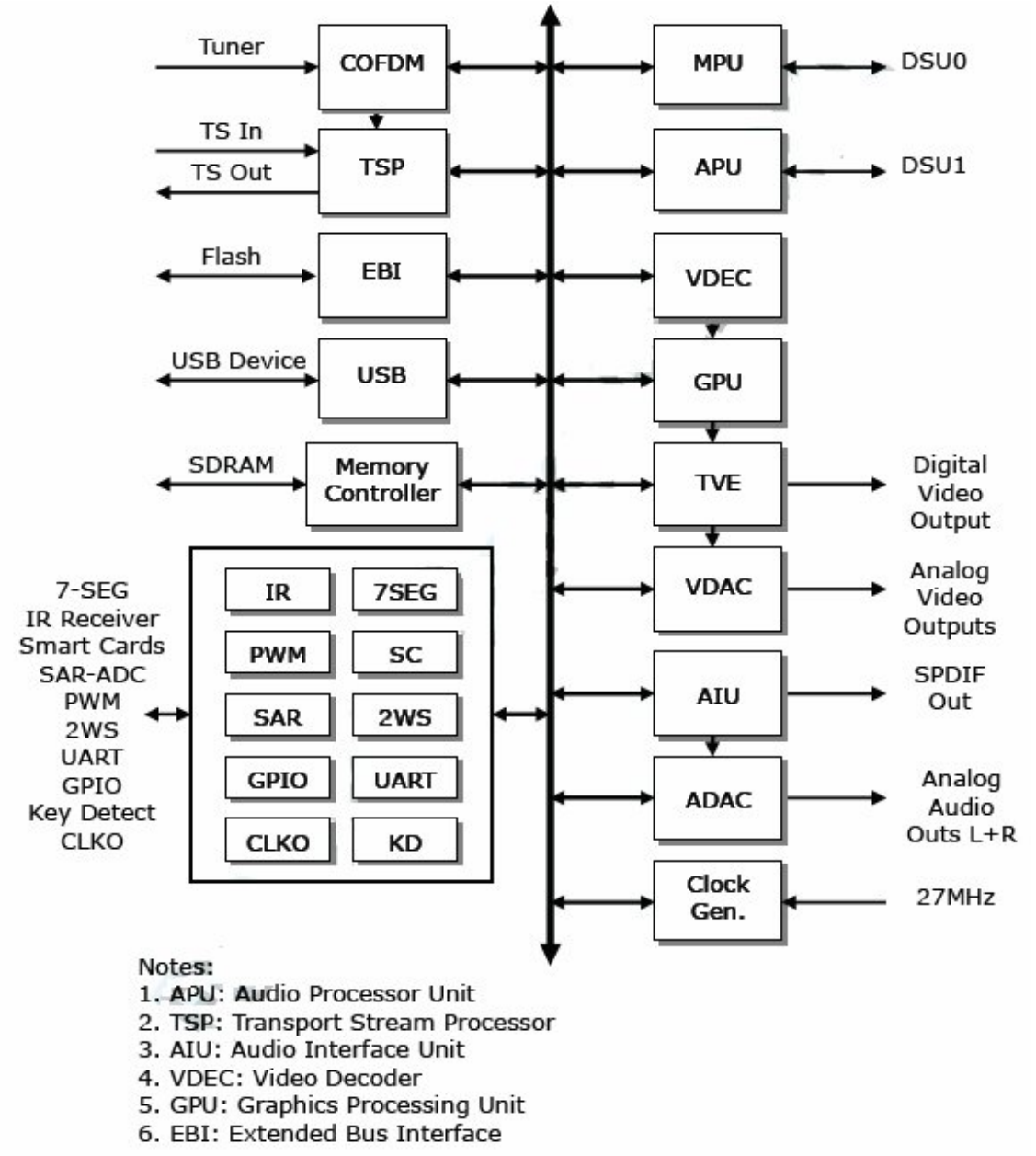


OPTIONS:

•MOBIL & DVD Options (Adapter or Car Battery)

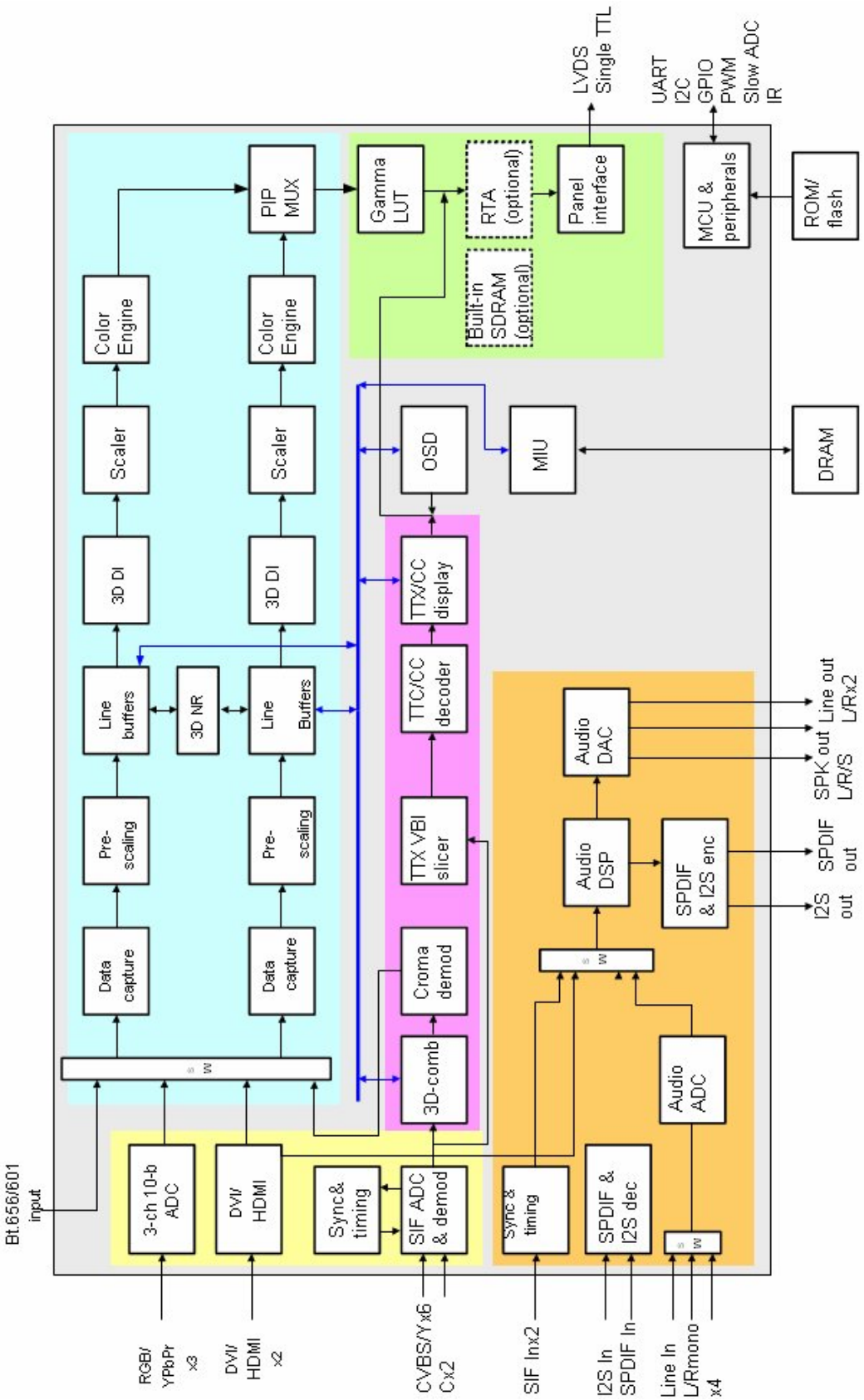


18.3. Integrated DVB-T Receiver Block Diagram



Notes:
1. APU: Audio Processor Unit
2. TSP: Transport Stream Processor
3. AIU: Audio Interface Unit
4. VDEC: Video Decoder
5. GPU: Graphics Processing Unit
6. EBI: Extended Bus Interface

18.4. MSTAR Block Diagram



LG

TU102 TDTC-G101D

AIF 12 — ANALOG_IF
DIF1 11 — DIGITAL_IF-
DIF2 10 — DIGITAL_IF+
IF_AGC 9 — IF_AGC_DVB_IN
AS 8 — ADDRESS_SEL_TUNER
NC 7
B2 6 — 5V_TUN
SDA 5 — SDA_TUNER
SCL 4 — SCL_TUNER
RF_AGC 3 — RF_AGC
B1 2 — 33V_TUNER
ANT_PWR 1 — ACT_ANT

Samsung/Thomson

TU101 DTOS403LH172A

IFOUT- 11 — L116 1u, C626 47p 50V — DIGITAL_IF-
IFOUT+ 10 — DIGITAL_IF+
VT 9 — 33V_TUNER
IF_AGC 8 — IF_AGC_DVB_IN
+5V 7 — 5V_TUN
AIF_OUT 6 — ANALOG_IF
SDA 5 — SDA_TUNER
SCL 4 — SCL_TUNER
SAS 3 — ADDRESS_SEL_TUNER
RF_AGC 2 — RF_AGC
BA 1 — ACT_ANT

S104

TP151

ACTIVE ANTENNA

5V_TUN — R482 4R7 — 2R1 — TH101

OVER_CUR_DETECT — R502 10K — 330R F234 — R501 10K — 5V_TUN

R622 1K — Q102 FDN336P — BC848B Q115 — R503 10K — ANT_CTRL

ACT_ANT — C359 10U 10V — R504 10K

D121 1N4148 — R111 12K — RF_AGC_A — T_AGC — C448 47U 16V N.C.

IF_AGC_DVB_IN — R505 10K — IF_AGC_DVB — 10V 100N C136

This part must be placed near the tuner

SCL_TUNER — R126 47R — SCL_TUN — C586 47P 50V

SDA_TUNER — R127 47R — SDA_TUN — C587 47P 50V

TUNER SUPPLY OPSION

8V_VCC — F116 330R — C600 47U 16V — U123 LM1117 (IN, OUT, GND, VOUT) — TP158 — 5V_TUN

C360 10U 10V — C134 100N 10V — Near Tuner supply pin

R408 1K — 330R — R460 330R — S105 — 1K

!!!En az 1.8 cm2 altta ve üstte soğutma alanı bırakılmalı.

AGC AND I2C SWITCH PART

Connect if "33V Integrated Tuner" is used!

33V_TUNER — R624 1K — C532 1U 50V — F159 330R — NC — 5V_TUN

F158 330R — 33V_VCC

S102 — 5V_VCC — C128 100N 10V

U115 74HCT4053

SCL_TUN_DVB — SCL_TUN
SCL
RF_AGC_DVB — SDA_TUN
RF_AGC — SDA_TUN_DVB
RF_AGC_A — SDA — S101
S103
10V 100N C137 NEAR THE TUNER
R254 4K7 — 5V_VCC

Q116 BC848B — R595 22K — IDTV_SW

OPSIONAL COIL

ANALOG_IF — L111 1U — L113 1U — C545 10N 16V — R680 56R — Q144 BF799

R252 4K7 — R623 1K — C135 100N 10V — R483 1K2 — L101 1U — L114 1U — R735 680R — R125 47R

R384 10R

SIF_CTL — R209 100K — Q140 BSN20 — R210 100K N.C.

8V_VCC — R380 220R — C520 47U 16V

R473 6K8 — R231 3K3 — 5V_TUN — 5V_TUN

C546 10N 16V — BA782 D145 — Z101 K9656M (IN1, OUT1, IN2, OUT2, GND) — SIFP — SIFM

R474 6K8 — 5V_TUN — R564 2K2

C547 10N 16V — Z102 K3958M (IN1, OUT1, IN2, OUT2, GND) — L104 2U2 N.C. — VIFM — VIFP

WARNING!!! Saw filter outputs must be close the chip

V-1 e gecerken yapilan updateler

Video SAW filitre cikislari caprazlandı

C467 10U 10V — C132 100N 10V — 3V3_STBY — F187 330R

C611 220n 6V3 — C133 220n 10V — C597 220P 50V — C620 100p 50V

U138 MST6WB7GQ-3

WARNING!!! This part must be close to chip

C363 10U 10V — C131 100N 10V

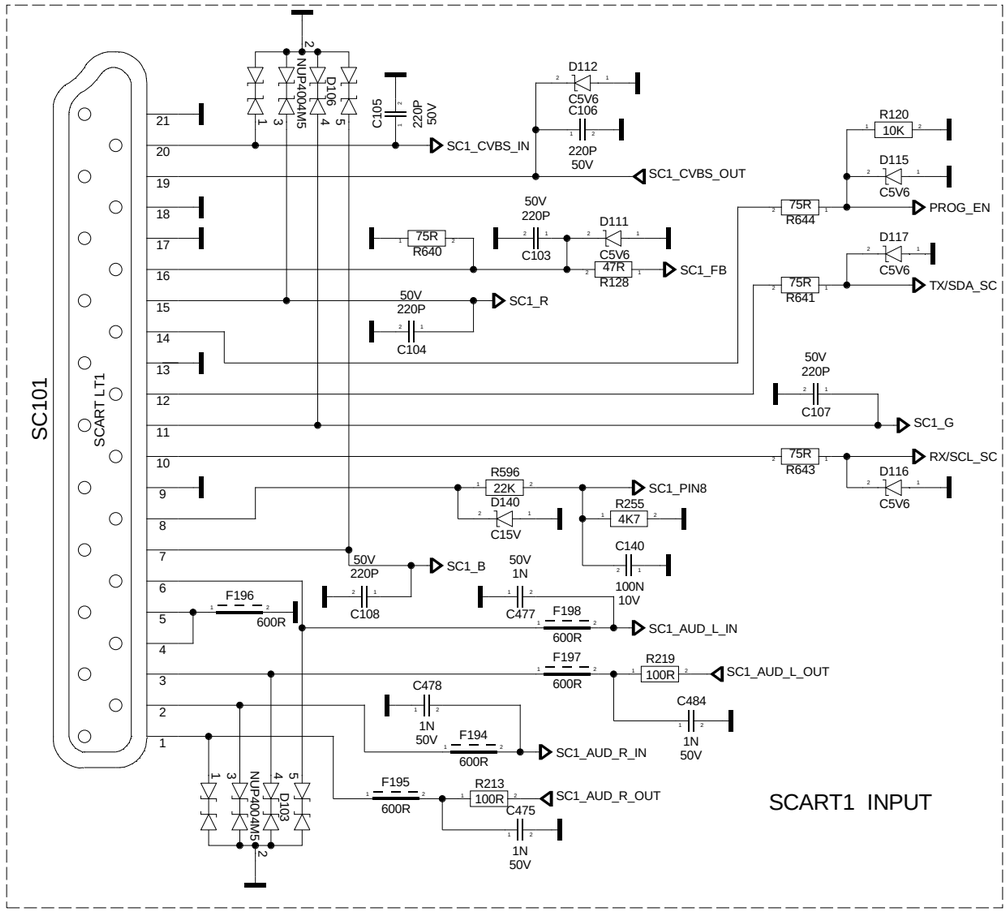
3V3_VCC — F184 330R — C364 10U 10V — C130 100N 10V

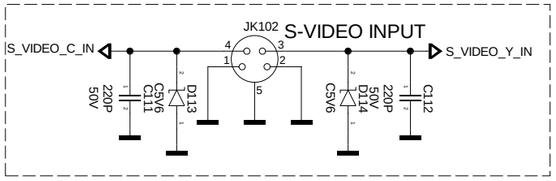
C361 10U 10V — C129 100N 10V

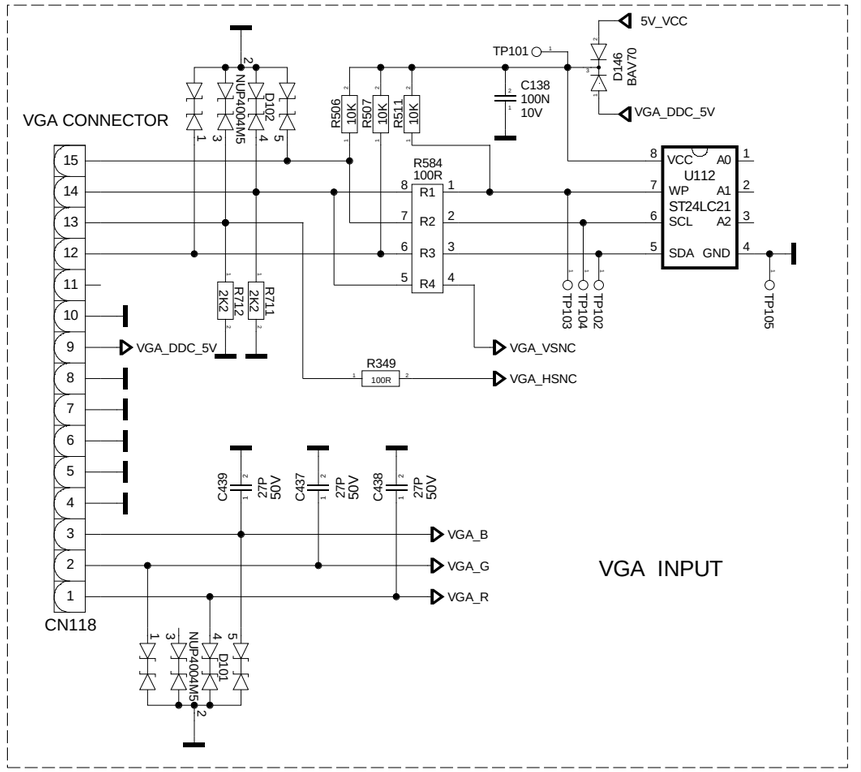
3V3_VCC — F185 330R

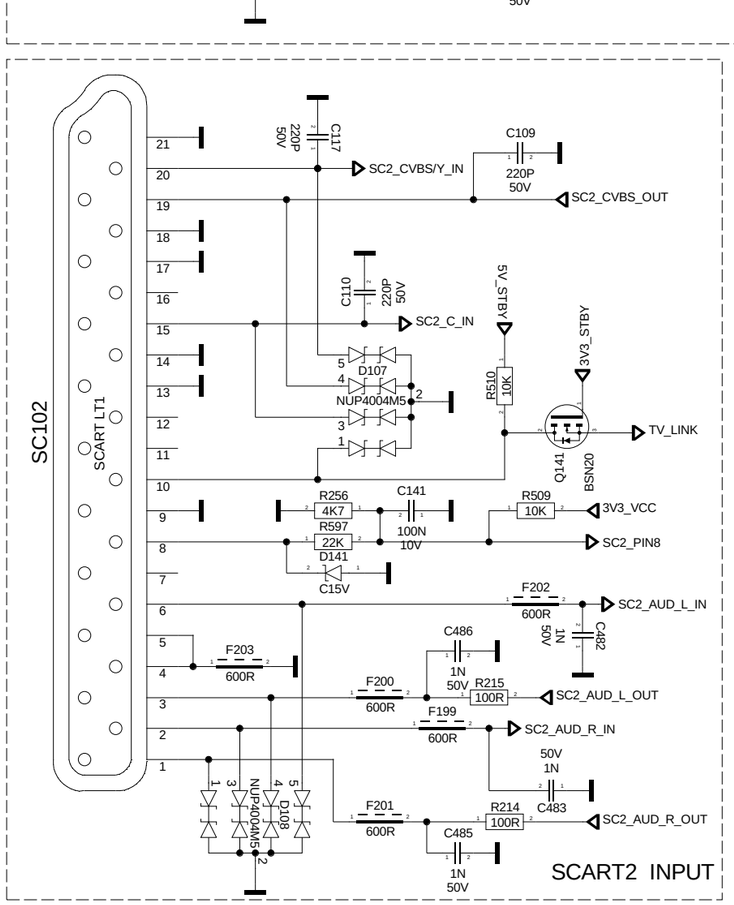
5V_TUN — F186 330R — C510 100N 10V — 4K7 R253 — T_AGC

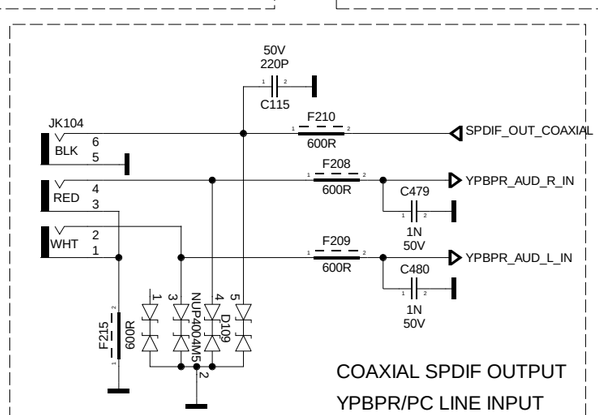
VESTEL	PROJECT NAME : 17MB35-1		A3
SCH NAME : ANALOG IF		SHEET: 1	OF: 12
DRAWN BY : ÖNDER GENÇ		4-16-2008_14:01	

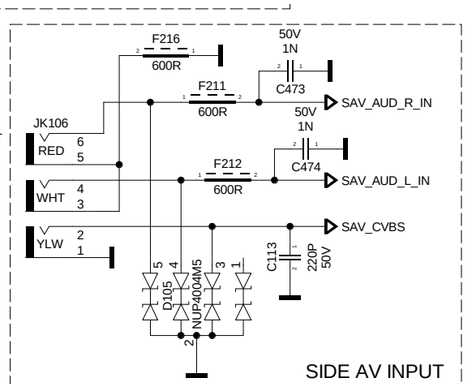


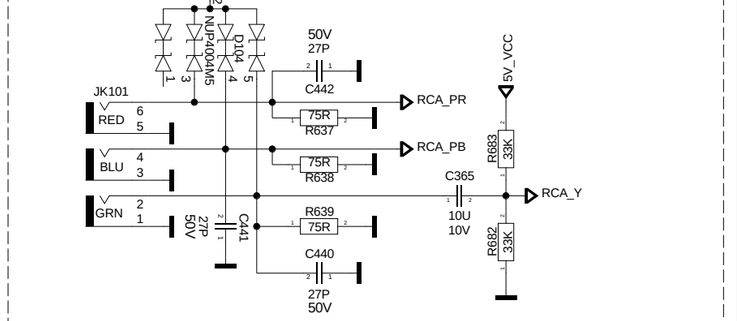


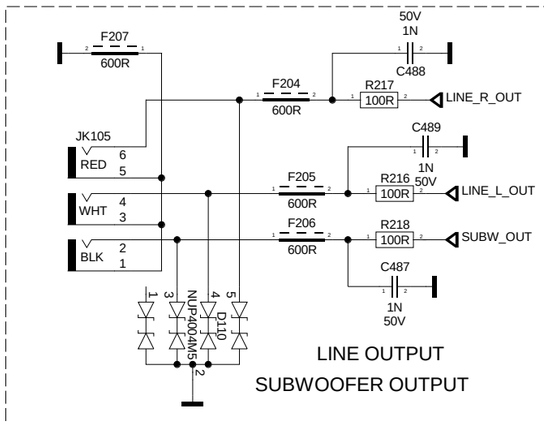


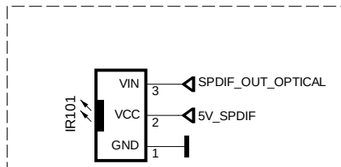


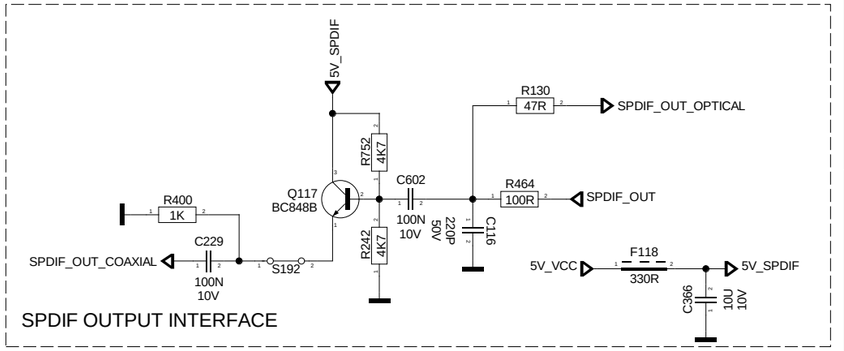












VESTEL	PROJECT NAME : 17MB35-1		A3
SCH NAME : A/V INTERFACE		SHEET: 2	OF: 12
DRAWN BY : GORKEMKGO		4-16-2008_14:01	

VIDEO TERMINATIONS AND DIFFERENTIAL TRACING

Place 75R termination resistors close to Paulo reference GNDs

SC2_C_IN — R651 75R — R143 47R — 16V 47N C432 — C0
SC2_CVBS/Y_IN — R650 75R — R142 47R — C434 47N 16V — Y0
S_VIDEO_C_IN — R653 75R — R145 47R — 16V 47N C423 — C1
S_VIDEO_Y_IN — R652 75R — R144 47R — C422 47N 16V — Y1
SC1_CVBS_IN — R654 75R — R146 47R — C424 47N 16V — CVBS1
R773 470R — C612 1N — SOGIN0
SAV_CVBS — R649 75R — R141 47R — C433 50V 47N 16V — CVBS2
DVB_CVBS — R664 75R — R140 47R — C435 47N 16V — CVBS3
SC1_B — R665 75R — R137 47R — C421 47N 16V — BIN0P
SC1_G — R667 75R — R138 47R — C418 47N 16V — GIN0P
SC1_R — R666 75R — R139 47R — C417 47N 16V — RIN0P
SW_PB — R656 75R — R149 47R — C428 47N 16V — BIN2P
SW_Y — R657 75R — R148 47R — C426 47N 16V — GIN2P
R403 470R — C490 1N 50V — SOGIN2
SW_PR — R655 75R — R147 47R — C427 47N 16V — RIN2P
VGA_B — R659 75R — R150 47R — C429 47N 16V — BIN1P
VGA_G — R658 75R — R151 47R — C431 47N 16V — GIN1P
R404 470R — C491 1N 50V — SOGIN1
VGA_R — R660 75R — R152 47R — C430 47N 16V — RIN1P

U138 MST6WB7GQ-3

VGA_HSNC	17	HSYNC1	AVDD_AU_1	74	AVDD_AU
VGA_VSNC	18	VSYNC1	GND5	75	
C152 100N 10V	19	VCLAMP	AUVRM	76	
C151 100N 10V	20	REFP	AUVRP	77	
C150 100N 10V	21	REFM	AUVAG	78	C368 C344 1U 16V
BIN1P	22	BIN1P	AVDD_AU_2	79	AVDD_AU
SOGIN1	23	SOGIN1	LINE_IN_0L	80	LINE_IN_0L
GIN1P	24	GIN1P	LINE_IN_0R	81	LINE_IN_0R
RIN1P	25	RIN1P	LINE_IN_1L	82	LINE_IN_1L
R133 47R — C420 47N 16V	26	BIN0M	LINE_IN_1R	83	LINE_IN_1R
BIN0P	27	BIN0P	AUCOM	84	C149 — S106
R134 47R — C419 47N 16V	28	GIN0M	LINE_IN_2L	85	100N 10V — LINE_IN_2L
GIN0P	29	GIN0P	LINE_IN_2R	86	LINE_IN_2R
SOGIN0	30	SOGIN0	LINE_IN_3L	87	LINE_IN_3L
RIN0P	31	RIN0P	LINE_IN_3R	88	LINE_IN_3R
AVDD_33 — C143 100N 10V	32	AVDD_33_3	LINE_IN_MONO	89	R686 33K
	33	GND3	LINE_OUT_3L	90	DSP_CH2_L
	34	HSYNC0	LINE_OUT_3R	91	DSP_CH2_R
SC1_FB	35	VSYNC0	LINE_OUT_2L	92	DSP_CH4_L
R687 33K	36	VSYNC2	LINE_OUT_2R	93	DSP_CH4_R
BIN2P	37	BIN2P	LINE_OUT_1L	94	DSP_CH1_L
SOGIN2	38	SOGIN2	LINE_OUT_1R	95	DSP_CH1_R
GIN2P	39	GIN2P	LINE_OUT_0L	96	DSP_CH3_L
RIN2P	40	RIN2P	LINE_OUT_0R	97	DSP_CH3_R
C1	41	C1			
Y1	42	Y1			
C0	43	C0			
Y0	44	Y0			
CVBS3	45	CVBS3			
CVBS2	46	CVBS2			
CVBS1	47	CVBS1			
R132 47R — R512 10K — R131 47R — C425 47N 16V — C416 47N 16V	48	VCOM1			
	49	CVBS0			
	50	VCOM0			
AVDD_33 — C144 100N 10V	51	AVDD_33_4			
	52	CVBSOUT1			
	53	CVBSOUT0			
	54	GND4			

CVBS1_OUT — R350 100R
CVBS0_OUT — R351 100R

AVDD_AU DECOUPLING CAPACITORS

AVDD_AU — C142 100N 10V — Pin79
Pin74 — C145 100N 10V
F120 330R — 3V3_VCC

AUDIO PREAMPLIFIERS

Place close to Paulo

SUBW_R — R741 20K — C333 1U 16V
SUBW_L — R740 20K — C334 1U 16V
8V_VCC — F218 600R — C513 100n 16V
R679 82K — C146 10V 100N
R466 1K8 — R465 1K8
R693 33K — C376 10V 10U — SUBW_OUT
C522 220N 16V — C521 220N 16V
U119 TL062 (OUT1, VDD, IN1-, OUT2, V+, IN1+, IN2-, VSS, IN2+)
BC848B Q122 — R523 10K — POP_MUTE
R749 3K3

SC1_AUD_R_OUT — C375 10V 10U — C121 220P 50V — R678 82K
R692 33K — R691 33K — C374 10V 10U — SC1_AUD_L_OUT
C120 220P 50V — R677 82K
SC_1_R — C332 1U 16V — R739 20K
U118 TL062 (OUT1, VDD, IN1-, OUT2, V+, IN1+, IN2-, VSS, IN2+)
R738 20K — C335 1U 16V — SC1_L
C512 100n 16V — F217 600R — 8V_VCC

SC2_AUD_R_OUT — C373 10U 10V — R156 47R
R689 33K — R154 47R — C370 10V 10U — SC2_AUD_L_OUT
R690 33K
LINE_R_OUT — C372 10V 10U — R155 47R
POP_MUTE — R522 10K — Q121 BC848B — R751 3K3
C119 50V 220P — R676 82K
8V_VCC — F219 600R — C511 100n 16V
R153 47R — C371 10V 10U — LINE_L_OUT
C118 50V 220P — R675 82K
Q120 BC848B — R521 10K — POP_MUTE — R750 3K3
SC2/LINE_OUT_R — C331 1U 16V — R737 20K
U117 TL062 (OUT1, VDD, IN1-, OUT2, V+, IN1+, IN2-, VSS, IN2+)
R736 20K — C330 1U 16V — SC2/LINE_OUT_L

V+ — C327 1U 16V — C367 10U 10V — R684 33K — R685 33K — 8V_VCC

AUDIO INPUT VOLTAGE DIVISION AND DC BLOCK

Place close to Paulo

LINE_IN_0L	C340 1U 16V — R513 10K	R607 22K	SC1_AUD_L_IN
LINE_IN_0R	C341 1U 16V — R514 10K	C493 1N 50V — R606 22K	SC1_AUD_R_IN
LINE_IN_1L	C338 1U 16V — R515 10K	C492 1N 50V — R605 22K	SC2_AUD_L_IN
LINE_IN_1R	C339 1U 16V — R516 10K	C495 1N 50V — R603 22K	SC2_AUD_R_IN
LINE_IN_2L	C336 1U 16V — R517 10K	C494 1N 50V — R601 22K	YPBPR_AUD_L_IN
LINE_IN_2R	C337 1U 16V — R518 10K	C497 1N 50V — R600 22K	YPBPR_AUD_R_IN
LINE_IN_3L	C343 1U 16V — R519 10K	C496 1N 50V — R599 22K	SAV_AUD_L_IN
LINE_IN_3R	C342 1U 16V — R520 10K	C498 1N 50V — R598 22K	SAV_AUD_R_IN
		C499 1N 50V	

DVB/YPBPR SWITCH

DVB/YPBPR_SW — R627 1K
DVB_PR — R661 75R
SW_PR
DVB_Y — C444 27P 50V — R662 75R
C443 27P 50V
S109 S110 — RCA_PR
RCA_Y — S108 S112
SW_Y
U129 PI5V330 (IN, S1A, S2A, DA, S1B, S2B, DB, GND; VCC, EN, S1D, S2D, DD, S1C, S2C, DC)
10V 100N — C147 — F151 330R — 5V_VCC
RCA_PB — S107 S111 — SW_PB
DVB_PB — C445 27P 50V — R663 75R

SCART VIDEO OUTPUT AMPLIFIERS

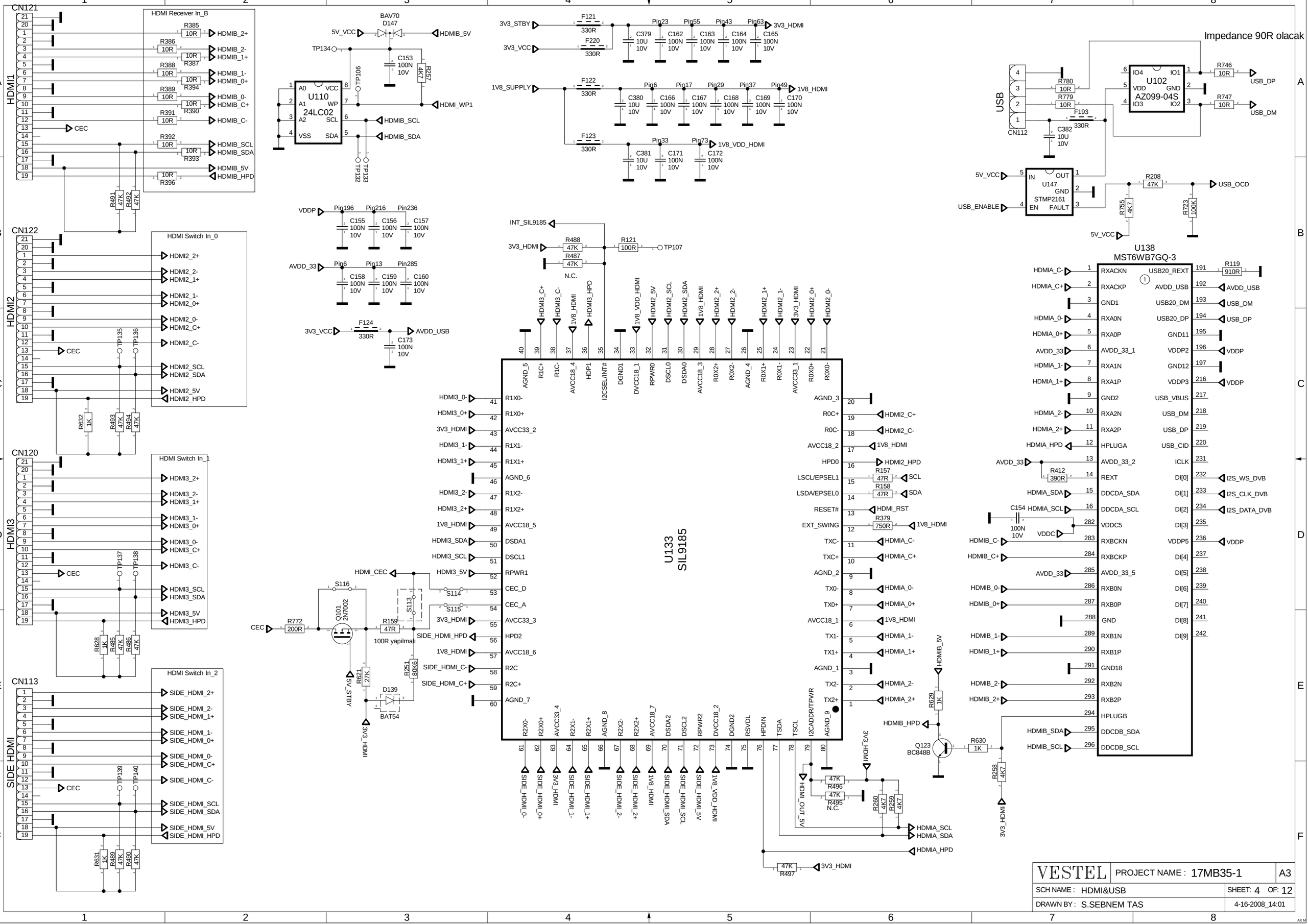
5V_VCC — F119 330R — C326 1U 16V
Q146 BC858B — R402 470R — R674 39K — Q119 BC848B — C378 10U 10V — CVBS0_OUT
SC1_CVBS_OUT — R646 75R — R620 300R — R777 75R — R221 100R — R467 15K
Q145 BC858B — R401 470R — R673 39K — Q118 BC848B — C377 10U 10V — CVBS1_OUT
SC2_CVBS_OUT — R645 75R — R619 300R — R778 75R — R220 100R — R468 15K
GAIN_SW1 — R753 4k7 — Q154 2N7002
GAIN_SW2 — R754 4k7 — Q155 2N7002

AUDIO OUTPUT FILTERS

Place close to Paulo

DSP_CH2_L	R228 100R	C555 10N 16V — 22K R419	HP_L
DSP_CH2_R	R229 100R	C554 10N 16V — 22K R420	HP_R
DSP_CH4_L	R224 100R	C550 10N 16V — 22K R415	SC2/LINE_OUT_L
		R626 1K — C329 1U 16V	SUBW_L
DSP_CH4_R	R225 100R	C551 10N 16V — 22K R416	SC2/LINE_OUT_R
		R625 1K — C328 1U 16V	SUBW_R
SC_1_R	R790 100R		SC2/LINE_OUT_R
SC1_L	R791 100R		SC2/LINE_OUT_L
DSP_CH1_L	R227 100R	C553 10N 16V — 22K R418	MAIN_L
DSP_CH1_R	R226 100R	C552 10N 16V — 22K R417	MAIN_R
DSP_CH3_L	R223 100R	C549 10N 16V — 22K R414	SC1_L
DSP_CH3_R	R222 100R	C548 10N 16V — 22K R413	SC_1_R

VESTEL	PROJECT NAME : 17MB35-1		A3
SCH NAME : A/V INTERFACE		SHEET: 3	OF: 12
DRAWN BY : GORKEMKGO		4-16-2008_14:01	


CN121
HDMI1
HDMI Receiver In_B
HDMIB_2+
HDMIB_2-
HDMIB_1+
HDMIB_1-
HDMIB_0+
HDMIB_0-
HDMIB_C+
HDMIB_C-
CEC
HDMIB_SCL
HDMIB_SDA
HDMIB_5V
HDMIB_HPD
CN122
HDMI2
HDMI Switch In_0
HDMI2_2+
HDMI2_2-
HDMI2_1+
HDMI2_1-
HDMI2_0+
HDMI2_0-
HDMI2_C+
HDMI2_C-
CEC
HDMI2_SCL
HDMI2_SDA
HDMI2_5V
HDMI2_HPD
CN120
HDMI3
HDMI Switch In_1
HDMI3_2+
HDMI3_2-
HDMI3_1+
HDMI3_1-
HDMI3_0+
HDMI3_0-
HDMI3_C+
HDMI3_C-
CEC
HDMI3_SCL
HDMI3_SDA
HDMI3_5V
HDMI3_HPD
CN113
SIDE HDMI
HDMI Switch In_2
SIDE_HDMI_2+
SIDE_HDMI_2-
SIDE_HDMI_1+
SIDE_HDMI_1-
SIDE_HDMI_0+
SIDE_HDMI_0-
SIDE_HDMI_C+
SIDE_HDMI_C-
CEC
SIDE_HDMI_SCL
SIDE_HDMI_SDA
SIDE_HDMI_5V
SIDE_HDMI_HPD
BAV70
D147
5V_VCC
HDMIB_5V
TP134
C153 100N 10V
R257 4K7
HDMI_WP1
U110
24LC02
HDMIB_SCL
HDMIB_SDA
TP90
TP132
TP133
3V3_STBY
3V3_VCC
F121 330R
F220 330R
C379 10U 10V
C162 100N 10V
C163 100N 10V
C164 100N 10V
C165 100N 10V
Pin23
Pin55
Pin43
Pin63
3V3_HDMI
1V8_SUPPLY
F122 330R
C380 10U 10V
C166 100N 10V
C167 100N 10V
C168 100N 10V
C169 100N 10V
C170 100N 10V
Pin6
Pin17
Pin29
Pin37
Pin49
1V8_HDMI
F123 330R
C381 10U 10V
C171 100N 10V
C172 100N 10V
Pin33
Pin73
1V8_VDD_HDMI
VDDP
C155 100N 10V
C156 100N 10V
C157 100N 10V
Pin196
Pin216
Pin236
AVDD_33
C158 100N 10V
C159 100N 10V
C160 100N 10V
Pin6
Pin13
Pin285
3V3_VCC
F124 330R
C173 100N 10V
AVDD_USB
INT_SIL9185
3V3_HDMI
R488 47K
R487 47K
N.C.
R121 100R
TP107
HDMI3_C+
HDMI3_C-
1V8_HDMI
HDMI3_HPD
1V8_VDD_HDMI
HDMI2_5V
HDMI2_SCL
HDMI2_SDA
1V8_HDMI
HDMI2_2+
HDMI2_2-
HDMI2_1+
HDMI2_1-
3V3_HDMI
HDMI2_0+
HDMI2_0-
U133
SIL9185
AGND_5
R1C+
R1C-
AVCC18_4
HDP1
I2CSEL/INT#
DGND1
DVCC18_1
RPWR0
DSCL0
DSDA0
AVCC18_3
R0X2+
R0X2-
AGND_4
R0X1+
R0X1-
AVCC33_1
R0X0+
R0X0-
HDMI3_0-
HDMI3_0+
3V3_HDMI
HDMI3_1-
HDMI3_1+
R1X0-
R1X0+
AVCC33_2
R1X1-
R1X1+
AGND_6
R1X2-
R1X2+
AVCC18_5
DSDA1
DSCL1
RPWR1
CEC_D
CEC_A
AVCC33_3
HPD2
AVCC18_6
R2C
R2C+
AGND_7
AGND_3
R0C+
R0C-
AVCC18_2
HPD0
LSCL/EPSEL1
LSDA/EPSEL0
RESET#
EXT_SWING
TXC-
TXC+
AGND_2
TX0-
TX0+
AVCC18_1
TX1-
TX1+
AGND_1
TX2-
TX2+
I2CADDR/TPWR
AGND_9
HDMI2_C+
HDMI2_C-
1V8_HDMI
HDMI2_HPD
SCL
SDA
HDMI_RST
1V8_HDMI
HDMIA_C-
HDMIA_C+
HDMIA_0-
HDMIA_0+
1V8_HDMI
HDMIA_1-
HDMIA_1+
HDMIA_2-
HDMIA_2+
R2X0-
R2X0+
AVCC33_4
R2X1-
R2X1+
AGND_8
R2X2-
R2X2+
AVCC18_7
DSDA2
DSCL2
RPWR2
DVCC18_2
DGND2
RSVDL
HPDIN
TSDA
TSCL
I2CADDR/TPWR
AGND_9
SIDE_HDMI_0-
SIDE_HDMI_0+
3V3_HDMI
SIDE_HDMI_1-
SIDE_HDMI_1+
SIDE_HDMI_2-
SIDE_HDMI_2+
1V8_HDMI
SIDE_HDMI_SDA
SIDE_HDMI_SCL
SIDE_HDMI_5V
1V8_VDD_HDMI
HDMI_CEC
S116
S114
S115
S113
Q101
2N7002
CEC
R772 200R
R159 47R
100R yapilmali
SIDE_HDMI_HPD
1V8_HDMI
SIDE_HDMI_C-
SIDE_HDMI_C+
R621 27K
R251 80K6
D139
BAT54
5V_STBY
3V3_HDMI
HDMI_OUT_5V
R496 47K
R495 47K
N.C.
R260 4K7
R259 4K7
HDMIA_SCL
HDMIA_SDA
HDMIA_HPD
R497 47K
3V3_HDMI
HDMIB_5V
R629 1K
HDMIB_HPD
Q123
BC848B
R630 1K
R258 4K7
3V3_HDMI
Impedance 90R olacak
USB
CN112
R780 10R
R779 10R
F193 330R
C382 10U 10V
U102
AZ099-04S
IO1
IO2
IO3
IO4
VDD
GND
R746 10R
R747 10R
USB_DP
USB_DM
5V_VCC
U147
STMP2161
IN
OUT
GND
EN
FAULT
USB_ENABLE
R208 47K
R755 4K7
R723 100K
USB_OCD
U138
MST6WB7GQ-3
HDMIA_C-
HDMIA_C+
HDMIA_0-
HDMIA_0+
AVDD_33
HDMIA_1-
HDMIA_1+
HDMIA_2-
HDMIA_2+
HDMIA_HPD
RXACKN
RXACKP
GND1
RXA0N
RXA0P
AVDD_33_1
RXA1N
RXA1P
GND2
RXA2N
RXA2P
HPLUGA
AVDD_33_2
REXT
DDCDA_SDA
DDCDA_SCL
VDDC5
RXBCKN
RXBCKP
AVDD_33_5
RXB0N
RXB0P
GND
RXB1N
RXB1P
GND18
RXB2N
RXB2P
HPLUGB
DDCDB_SDA
DDCDB_SCL
USB20_REXT
AVDD_USB
USB20_DM
USB20_DP
GND11
VDDP2
GND12
VDDP3
USB_VBUS
USB_DM
USB_DP
USB_CID
ICLK
DI[0]
DI[1]
DI[2]
DI[3]
VDDP5
DI[4]
DI[5]
DI[6]
DI[7]
DI[8]
DI[9]
R119 910R
R412 390R
C154 100N 10V
VDDC
HDMIB_C-
HDMIB_C+
HDMIB_0-
HDMIB_0+
HDMIB_1-
HDMIB_1+
HDMIB_2-
HDMIB_2+
HDMIB_SDA
HDMIB_SCL
I2S_WS_DVB
I2S_CLK_DVB
I2S_DATA_DVB
VDDP
VESTEL
PROJECT NAME : 17MB35-1
A3
SCH NAME : HDMI&USB
SHEET: 4 OF: 12
DRAWN BY : S.SEBNEM TAS
4-16-2008_14:01

LED&VFD

CN106 1 2 3 4 5 6 7 8 9 10

5V_STBY
D130 C5V6 R552 10K 3V3_STBY
F228 600R VFD_CSB
D149 C5V6 R527 10K 3V3_STBY
F229 600R F230 600R VFD_CLK_STBY
VFD_DATA_STBY

CN119 1 2 3 4 5

S119 3V3_STBY
S118 5V_STBY
S198 3V3_LPW
R526 10K D148 C5V6 3V3_STBY
F225 600R IR_MAIN
C608 27P 50V

R421 10K Q130 BC848B R528 10K
Q148 BC858B
Q149 BC858B R531 10K
Q131 BC848B R422 10K
LED2 LED1

3V3_LPW S197 R382 220R
3V3_STBY S117
5V_STBY S125 R381 220R

3V3_LPW 3V3_STBY
R759 4K7 R265 4K7
STBY_ON/OFF
STBY_ON/OFF_NOT R608 22K Q125 BC848B

VDDP C175 100N 10V C177 100N 10V C176 100N 10V PIN108 PIN272 PIN226
VDDC C178 100N 10V PIN110

C598 220P 50V D150 C5V6 F231 600R MECH_SWITCH
LPW da 3v3 zener secilecek
D152 C5V6 D151 C5V6 C174 100N 10V
R167 47R F188 600R KEYBOARD_STBY
F227 600R 3V3_STBY
F226 600R 3V3_LPW
CN114 1 2 3 4

U138 MST6WB7GQ-3

3V3_STBY R277 4K7	55	GPIOL[0]	
LED1	56	GPIOL[1]	
3V3_STBY R276 4K7 LED2	57	GPIOL[2]	
PDP_DISP_EN R160 47R	58	GPIOL[3]	
SIF_CTL	59	GPIOL[4]	
STBY_ON/OFF_NOT S193 R267 4K7	60	XOUT	
3V3_STBY R748 47R	61	XIN	
C447 27P 50V X104 14.31818MHZ R110 1M C446 27P 50V	98	GPIOD[0]	
3V3_VCC FRC_RST R758 4K7	99	GPIOD[1]	
PROG_EN	100	GPIOD[2]	
USB_DIG_OCD	101	GPIOD[3]	
DVB_RESET 3V3_VCC R274 4K7	102	GPIOD[4]	
3V3_VCC R756 4k7 GAIN_SW2	103	GPIOD[5]	
GAIN_SW1	104	GPIOD[6]	
3V3_VCC R757 4k7	105	GPIOD[7]	
3V3_VCC R288 4K7 DVB/YPBPR_SW	106	GPIOD[8]	
3V3_VCC R269 4K7 DVB_IRQ	107	GPIOD[9]	
VDDP	108	VDDP1	
	109	GND6	
VDDC	110	VDDC1	
3V3_VCC R269 4K7 IDTV_SW	111	GPIOD[10]	
3V3_STBY R270 4K7 PROTECT	112	GPIOD[11]	
NVM_WP	113	GPIOD[12]	
3V3_STBY R271 4K7 VFD_CLK_STBY	114	GPIOD[13] 5V_TOLERANT	
	115	GPIOD[14]	
INT_SIL9185	116	GPIOD[15]	
HDMI_WP1	117	GPIOD[16]	
VFD_DATA_STBY	118	GPIOD[17] 5V_TOLERANT	
HDMI_CEC	149	GPIOR[0]	
HDMIB_5V R395 1k	150	GPIOR[1] 5V_TOLERANT	
HDMI_OUT_5V	151	GPIOR[2]	
3V3_STBY R283 4K7 PROTECT_PANEL	152	GPIOR[3]	
3V3_VCC R264 4K7 ANT_CTRL	153	GPIOR[4]	
VFD_CSB	154	GPIOR[5] 5V_TOLERANT	
PIX_INT0	155	GPIOR[6]	
PIX_INT1	156	GPIOR[7]	
3V3_VCC R266 4K7 PIX_RESET	157	GPIOR[8]	
USB_OCD	158	GPIOR[9]	
PDP_IRQ R166 47R	159	GPIOR[10]	

N.C. 4K7 R293 3V3_STBY	204	SAR0	
KEYBOARD_STBY_OUT	205	SAR1	
SC1_PIN8	206	SAR2	
SC2_PIN8 R742 20K	207	SAR3	
For Internal CPU Selection BACKLIGHT_DIM	208	PWM0	
For Internal CPU Selection 4K7 R279 3V3_STBY	209	PWM1	
R524 10K 3V3_STBY	210	DDCR_SDA	SDA
4K7 R287 3V3_STBY	211	DDCR_SCL	SCL
4K7 R286 3V3_STBY	212	DDCA_SDA	TX/SDA
4K7 R289 3V3_STBY	213	DDCA_SCL	RX/SCL
4K7 R290 3V3_STBY	214	INT	TV_LINK
10K R532 3V3_STBY	215	IRIN	IR_IN
4K7 R294 3V3_STBY	221	GPIOB[0]	SW_UPDATE_SELECT
R165 47R	222	GPIOB[1]	HP_DETECT
4K7 R275 3V3_VCC	223	PWM2	
	224	PWM3	AMP_MUTE
4K7 R278 3V3_STBY	225	GND14	
VDDP	226	VDDP4	
OPTION2	227	GPIOT[0]	
	228	GPIOT[1]	
4K7 R291 3V3_VCC	229	GPIOT[2]	DVB_RXD
R161 47R	230	GPIOT[3]	DVB_TXD
R162 47R 4K7 R292 3V3_VCC	243	HWRESET	
VDDP	272	VDDP7	
	273	GND17	
4K7 R273 3V3_STBY	274	GPIOE[3]	HDMI_RST
4K7 R285 3V3_STBY	275	GPIOE[2]	RS232_ENABLE
4K7 R261 3V3_STBY	276	GPIOE[1]	SDA_NVM
4K7 R262 3V3_STBY	277	GPIOE[0]	SCL_NVM
USB_ENABLE	278	GPIOM[0]	
R760 4K7 5V_VCC	279	GPIOM[1]	
	280	GPIOM[2]	
	281	GPIOM[3]	

R724 100K 10V 100N C182
R356 100R TP159 D155 1N4148
1 2 GND RST VCC MAX810 MAX809LTR U130 3
10V 100N C183 3V3_STBY
Reset IC supplyi 3V3 stbyden alindi

KEYBOARD & TOUCHPAD

DSUB-9 CN104 1 2 3 4 5 6 7 8 9

RS232 AND PROGRAMMING PART

RS232/RXD
RS232/TXD
TX/SDA R169 47R
RX/SCL R168 47R
U140 ST3222
NC1 R2OUT 10
T2IN R2IN 9
T1IN T2OUT 8
NC2 V- 7 C526 100N 25V
R1OUT C2- 6 C525 100N 25V
R1IN C2+ 5
T1OUT C1- 4
GND V+ 3 C523 100N 25V C524 100N 25V 3V3_STBY
VCC C1+ 2
SHDN EN 1
3V3_STBY C179 100N 10V
R530 10K 3V3_STBY
Q129 BC848B R529 10K R633 1K RS232_ENABLE

5V_STBY S120 N.C. CN110 1
RX/SCL R164 47R 2
TX/SDA R163 47R 3
4

DEBUG SOCKET

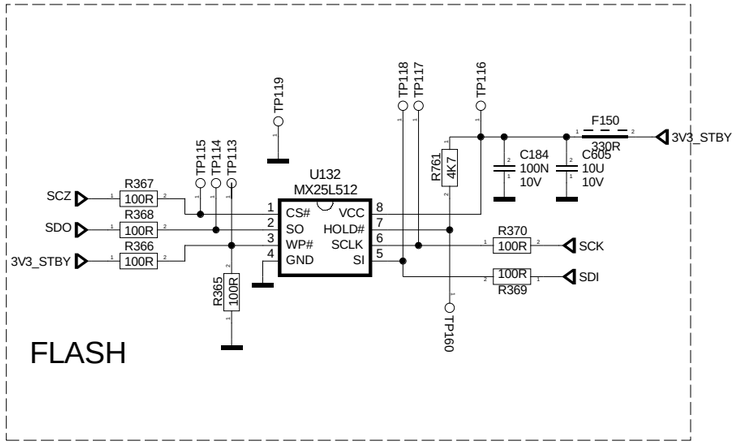
RS232_ENABLE	
0	ACTIVE
1	T-OUT AND R-OUT HIGH-Z
PROG_EN	
0	HC4052 DISABLE
1	HC4052 ENABLE
SW_UPDATE_SELECT	
0	DVB_SW_UPDATE
1	ANALOG_SW_UPDATE

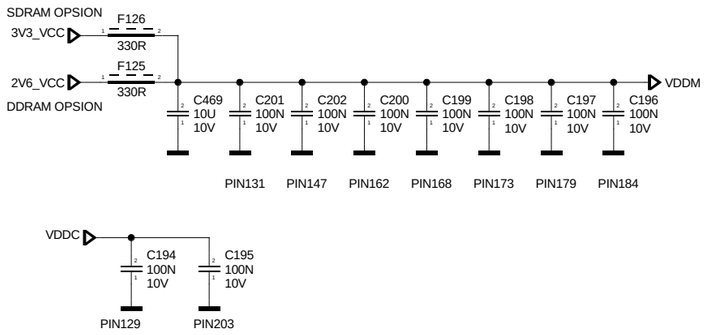
PROG_EN R280 4K7 Q128 BC848B
5V_STBY R281 4K7
U127 M74HC4052
UART0_RXD0 1 2Y0 VCC 16 C180 100N 10V 5V_STBY
RX/SCL_SC 3 2Y2 1Y2 15
RX/SCL 5 2Y1 1Y0 11 UART0_TXD0
6 E VEE 7 GND 8
2Z 1Z 13 TX/SDA_SC
2Y3 1Y1 14 TX/SDA
2Y1 1Y0 12 UART0_TXD0
E S0 10 SW_UPDATE_SELECT
VEE S1 9
GND
4K7 R284 5V_STBY

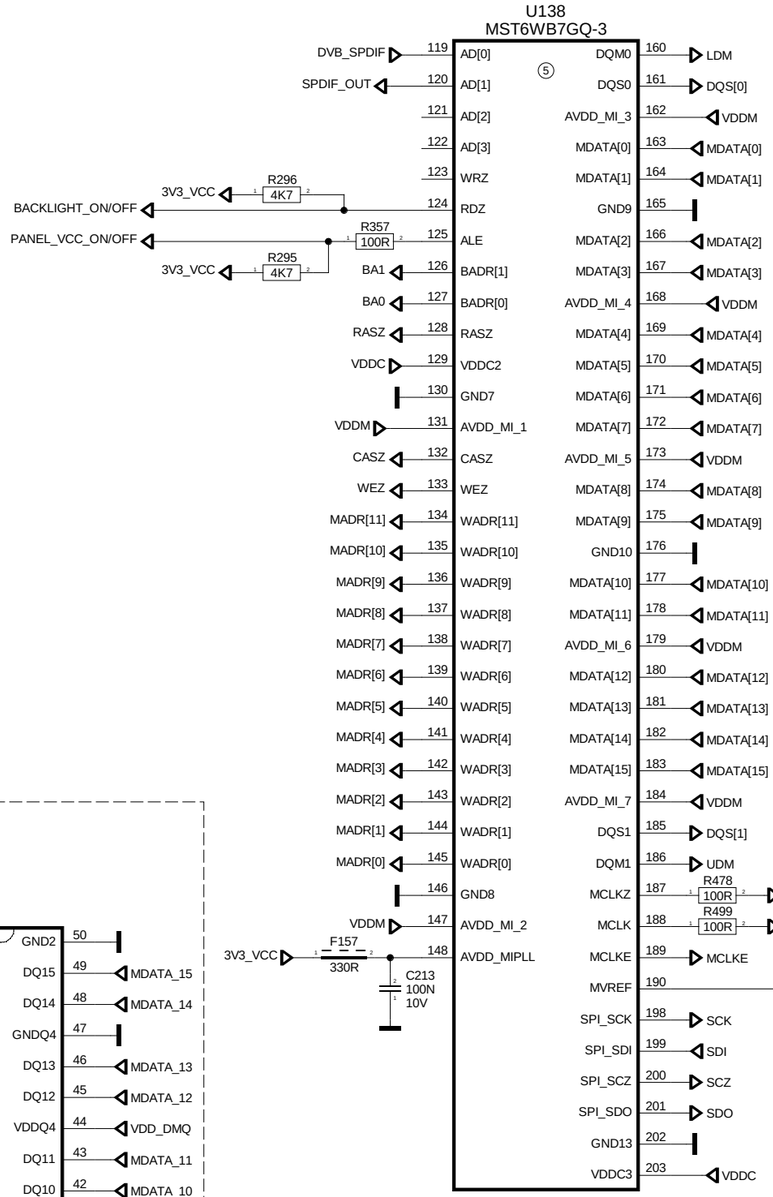
S122 3V3_VCC
S121 5V_VCC
R745 1K
PDP_IRQ S195
R233 4K7 Q147 BC858B
C530 220P 50V
S123
R352 100R
R353 100R
R354 100R
R355 100R
DIMMING
BACKLIGHT_DIM S194
R232 4K7 Q126 BC848B
C529 220P 50V
S196
R234 4K7 Q127 BC848B
C531 220P 50V
MEGA_DCR
C383 10U 10V

U103 24C32
E0 VCC 8 C181 100N 10V 3V3_STBY
E1 WC 7 NVM_WP
E2 SCL 6 SCL_NVM
VSS SDA 5 SDA_NVM
TP111
TP110 TP109 TP108 TP112

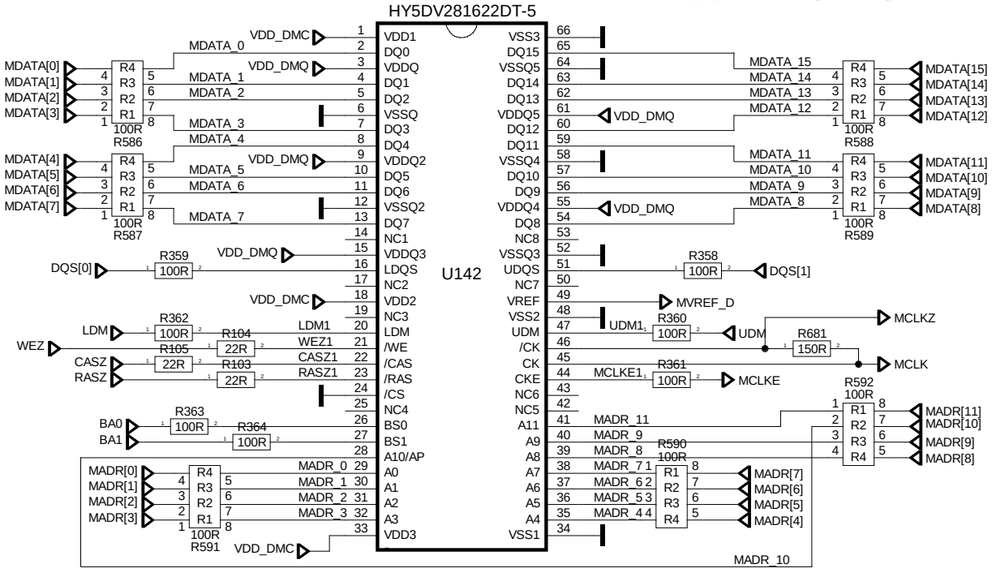
VESTEL	PROJECT NAME : 17MB35-1	A3
SCH NAME : CONTROLLER	SHEET: 5	OF: 12
DRAWN BY : ÖNDER GENÇ	4-16-2008_14:01	



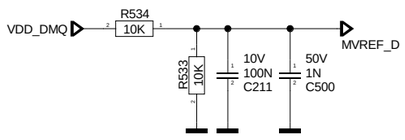


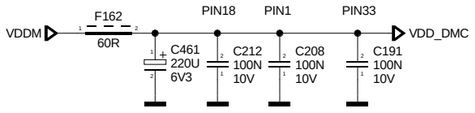


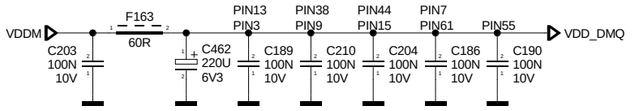
DDRAM OPTION



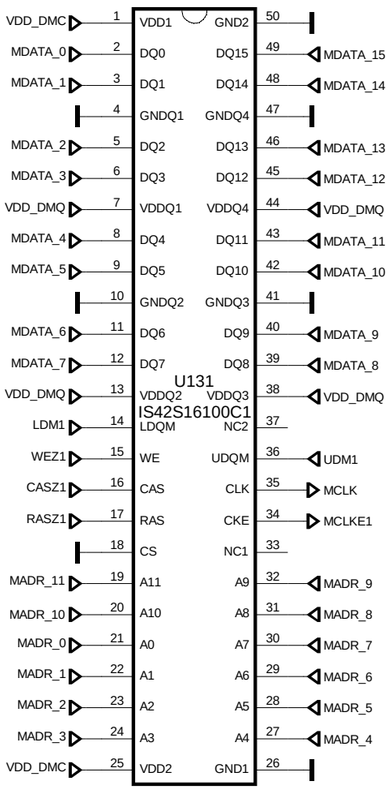
WARNING!!!DON'T USE VIA FOR DQS,MCLK,MCLKZ AND DATA SIGNALS





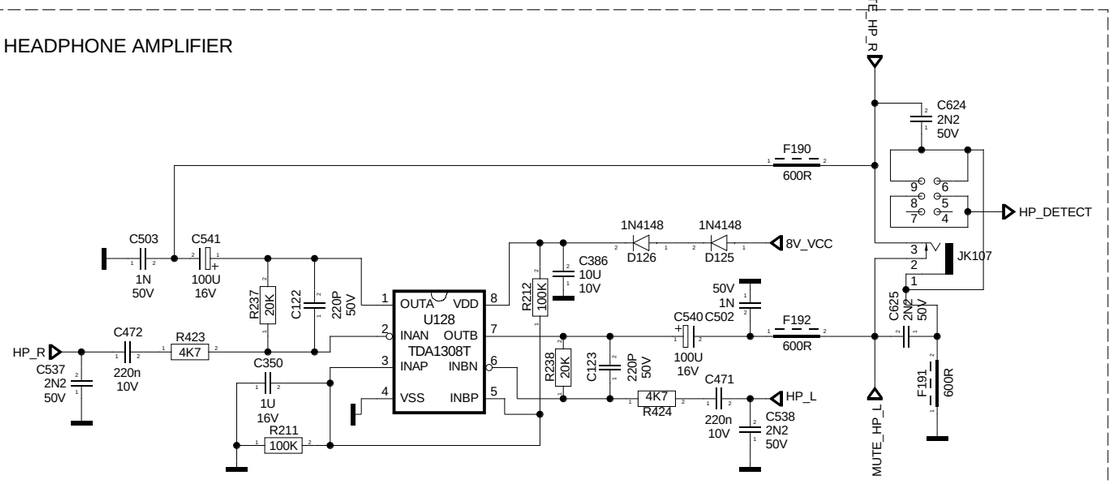


SDRAM OPTION

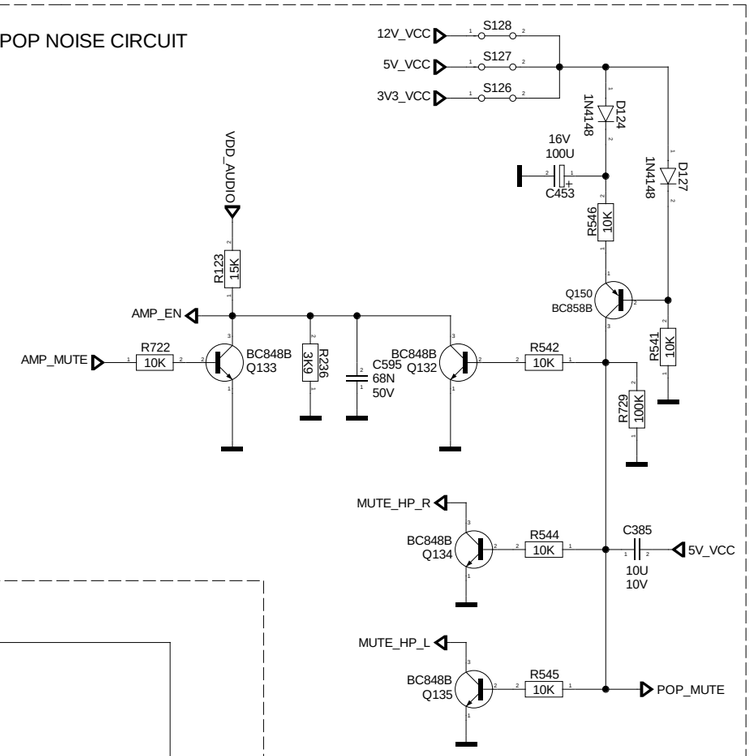


VESTEL	PROJECT NAME : 17MB35-1	A3
SCH NAME : MEMORY INTERFACE	SHEET: 6 OF: 12	
DRAWN BY : ÖNDER GENÇ	4-16-2008_14:01	

HEADPHONE AMPLIFIER

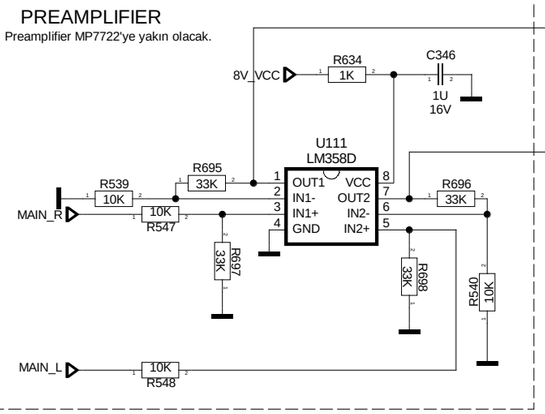


POP NOISE CIRCUIT

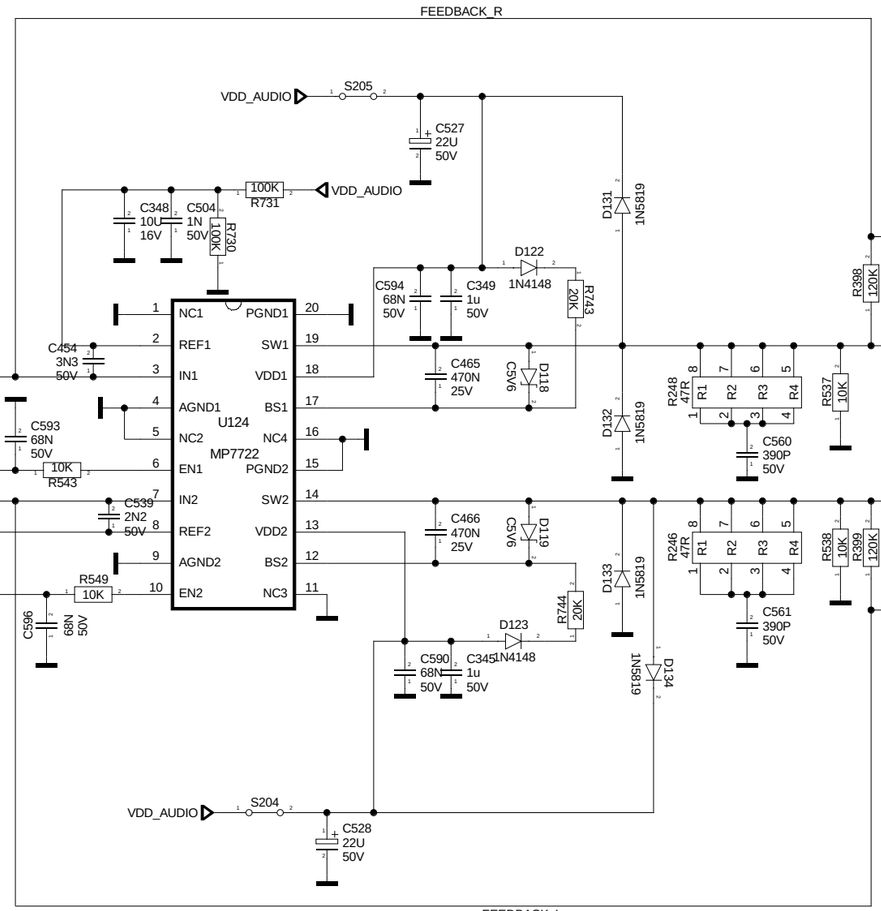


PREAMPLIFIER

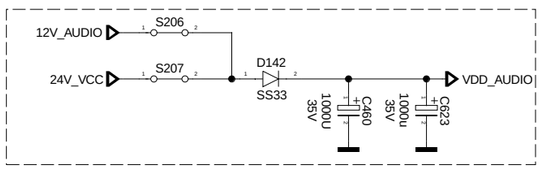
Preamplifier MP7722'ye yakın olacak.



FEEDBACK_R



FEEDBACK_L



VESTEL	PROJECT NAME : 17MB35-1	A3
SCH NAME : AUDIO		SHEET: 7 OF: 12
DRAWN BY : S.SEBNEM TAS		4-16-2008_14:01

ST QAM DEMODULATOR

U109
STV0297E

CAB/TER IF AGC SWITCH

U135 FSA3157

* only TER opt

BUF1=MPEG Out to CI

U108 74LCX245

* opt:with Cable
* opt:without Cable

BUF4=CI to MPEG IN

U105 74LCX245

* opt:with Cable
* opt:without Cable

BUF2=QAM to CI

U107 74LCX245

* opt:with Cable
* opt:without Cable

BUF3=QAM to MPEG_IN

U106 74LCX245

* opt:with Cable
* opt:without Cable

TS ROUTING

BUF B1/B4

U126 74LCX244

* opt:with Cable

BUF B2/B3

U125 74LCX244

* opt:with Cable

CI SOCKET

CN116

I2C ADDRESS
WRITE=38
READ=39

VESTEL	PROJECT NAME : 17MB35-1	A3
SCH NAME : DVB QAM & CI		SHEET: 8 OF: 12
DRAWN BY : ULAS DERELI		4-16-2008_14:01

CHEERTEK

MPEG DECODER

U104
CT216T-R

FUM Interface

CN109
R180 33R
MPEG_TS_OUT_D0
MPEG_TS_OUT_SYNC
FUM_EN
MPEG_TS_OUT_CLK
DSU_TXD0
DSU_RXD0
F130 330R
5V_DVB
UART0_TXD0
UART0_RXD0
R406 10K
3V3D_DVB
R307 4K7
MPEG_TS_OUT_VALID

CI CONTROL SIGNALS

CI_PWR_CTRL
R308 4K7
CI_CD
CI_RST
CI_WAIT
CI_OE
CI_WE
R434 33R
R435 33R
R436 33R
R433 33R
TS_SW4
TS_SW3
CI_REG
CI_IREQ
CI_IOWR
CI_IORD
TS_SW2
CI_CE
TS_SW1
CI_CD
CI_RST
CI_WAIT
CI_OE
CI_WE
CI_CE

SMART CARD INTERFACE

SM_PWR_EN
R306 4K7
1V8D_DVB
SM_CD
SM_RST
SM_DATA
SM_CLK
R189 33R

DVB VIDEO FILTER&AMP

U139
FMS6145
ENC_CVBS
ENC_PR
ENC_PB
ENC_Y
5V_VCC
F138 330R
R462 75R
R456 75R
R455 75R
R454 75R
C278 100N 10V
R461 75R
C124 220p 50V
DVB_CVBS
R457 75R
C139 220p 50V
DVB_PR
R458 75R
C102 220p 50V
DVB_PB
R459 75R
C101 220p 50V
DVB_Y

SDRAM

U134
MT48LC4M16A2TG8E
3V3_SDRAM_DVB
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
MDQM
MWE
MCAS
MRAS
MBS0
MBS1
MA10
MA0
MA1
MA2
MA3
MD15
MD14
MD13
MD12
MD11
MD10
MD9
MD8
MCLK_SDRAM
MA12
MA11
MA9
MA8
MA7
MA6
MA5
MA4

Comm.Port

GPG0 CAB/TER_AGC_SW
AVSS_3
AVO3 ENC_CVBS
AVD33_3 3V3A_DVB
AVO2 ENC_PR
AVSS_2
AVO1 ENC_PB
AVD33_2 3V3A_DVB
AVO0 ENC_Y
AVSS_1
FSADJ R198 470R
VREF C266 100N 10V
AVD33_1 3V3A_DVB
AUDIO_DAC_VMID C239 100N 10V
AUDIO_DAC_L TP122 C353 100U 16V
AUDIO_DAC_R TP120
GPC15/SPDIF R317 100R DVB_SPDIF
GPA0/CLKO/PCMACK
HAD8/PD0/GPOE8
HAD9/PD1/GPOE9
VDD18_2 1V8D_DVB
HAD10/PD2/GPOE10
HAD11/PD3/GPOE11
HAD12/PD4/GPOE12
HAD13/PD5/GPOE13
HAD14/PD6/GPOE14
HAD15/PD7/GPOE15
HA19/VSYN/GPOF19
HA18/HSYN/GPOF18
GPA7/PWM3/PCMSD/SCXO
GPA6/PWM2/PCMWS/SCXI
GPA5/PWM1/PCMCLK/TX2
GPA4/PWM0/PCMACK/RX2
UART0_TX/GPOC0 UART0_TXD0
UART0_RX UART0_RXD0
SAR_ADC_IN1
SAR_ADC_IN0
VDD33_3 3V3D_DVB
VSS_2
OSCI 27MHZ_IN
OSCO XTAL_OUT
GPC1/COFDM_ERR TP123
GPA12/AGC_RF
GPA11/AGC_IF
GPA15/SDA
GPA14/SCL
AVSS_PLL_2
VLFQ
AVD33_PLL
VLFM
AVSS_PLL_1
VCCA
VSSA
VCCAX

CVBS/YPbPr Video Outputs ==>

I2S Output ==>

27MHz VCXO

3V3_VCC
3V3D_DVB
F137 330R
C294 10u 10V
C245 100N 10V
C246 100N 10V
C247 100N 10V
C243 100N 10V
3V3_SDRAM_DVB
C244 100N 10V
C272 100N 10V
C236 100N 10V
C237 100N 10V
R789 1M
X102 27MHZ
C296 27P 50V
C297 27P 50V
U116
PI6CX100-27
X1
NC1
VIN
GND
X2
NC2
VDD
CLKOUT
XTAL_OUT
S130
XTAL_PWM
R774 10K
C606 1U 16V
S199
R201 47R
27MHZ_IN
C281 1U 16V
C389 10P 50V

DIGITAL USB

USB_DIG_DP
USB_DIG_DM
R525 10R
R550 10R
U113
AZ099-04S
IO1
GND
IO2
IO4
VDD
IO3
F131 330R
F152 330R
C161 10U 10V
CN125
USB_DIG_OCD
R551 47K
R553 100K
R763 4K7
5V_VCC
U148
STMP2161
OUT
GND
FAULT
IN
EN
5V_VCC
USB_ENABLE

IF_AGC_COFDM

R316 100R
R320 100R
SDA_TUN_DVB
R318 100R
SCL_TUN_DVB
C302
C303 1N
3V3A_PLL_DVB
* Layout Req.
1N
3V3A_ADC_DVB
R326 1K2
R328 1K2
R348 10K
C250 100N 10V
C249 100N 10V
R371 10K
C248 100N 10V
IF_AGC_COFDM
C354 100U 16V
C277 100N 10V
3V3D_DVB
IDTV_SW
BC847B
Q153
R762 4K7
CI 5V Switch Circuit
Q106
BSH103
5V_VCC
F139 330R
TP160
CI_PWR
C241 100N 10V
C290 10u 10V
C242 100N 10V
3V3_VCC
F132 330R
C288 10u 10V
C261 100N 10V
C262 100N 10V
C260 100N 10V
C263 100N 10V
3V3D_DVB
12V_VCC
R330 47K
R329 47K
3V3_VCC
F133 330R
C289 10u 10V
C273 100N 10V
C259 100N 10V
C258 100N 10V
3V3A_DVB
R347 10K
R377 10K
Q107
BC847B
CI_PWR_CTRL
DIGITAL_IF-
F134 330R
1V8_VCC
C295 10u 10V
C256 100N 10V
C257 100N 10V
C264 100N 10V
1V8D_DVB

RAM DATA BUS

R442 33R
R441 33R
R439 33R
R186
R438 33R
R315 100R
MCLK_SDRAM
3V3D_DVB

RAM ADDRESS BUS

R452 33R
R193
R451 33R
R443 33R
1V8D_DVB
R445 33R
R187
R444 33R
R446 33R
R437 33R
R450 33R

CI ADDRESS BUS

CI_A14
CI_A13
CI_A12
CI_A11
CI_A10
CI_A9
CI_A8
CI_A7
CI_A6
CI_A5
CI_A4
CI_A3
CI_A2
CI_A1
CI_A0

CI DATA BUS

CI_D7
CI_D6
CI_D5
CI_D4
CI_D3
CI_D2
CI_D1
CI_D0

SERIAL FLASH

CN107
3V3D_DVB
R500 4K7
DSU_TXD0
SMART CARD INTERFACE
CN22
C395 100N 10V
C396 100N 10V
SM_CD
SM_DATA
SM_RST
SM_CLK
SM_PWR_EN
F144 330R
F143 330R
3V3_VCC
5V_VCC
SERIAL FLASH
U114
MX25L512
CS#
SO
WP#
GND
VCC
HOLD#
SCLK
SI
R190 33R
R182 33R
SF_CS
SF_DO
R376 10K
R372 10K
R373 10K
TP154
TP153
TP124
C293 10u 10V
C240 100N 10V
F142 330R
3V3_VCC
R191 33R
R192 33R
SF_CLK
SF_DIO
TP141
TP155
TP156
TP152
C601 15p 50V
SF_CS
SF_DO
SF_CLK
SF_DIO

MPEG DEC TS OUTPUT

MPEG_TS_OUT_D0
MPEG_TS_OUT_D1
MPEG_TS_OUT_D2
MPEG_TS_OUT_D3
MPEG_TS_OUT_D4
MPEG_TS_OUT_D5
MPEG_TS_OUT_D6
MPEG_TS_OUT_D7
MPEG_TS_OUT_VALID
MPEG_TS_OUT_CLK
MPEG_TS_OUT_SYNC

MPEG DEC TS INPUT

MPEG_TS_IN_D7
MPEG_TS_IN_D6
MPEG_TS_IN_D5
MPEG_TS_IN_D4
MPEG_TS_IN_D3
MPEG_TS_IN_D2
MPEG_TS_IN_D1
MPEG_TS_IN_D0
MPEG_TS_IN_CLK
MPEG_TS_IN_VALID
MPEG_TS_IN_SYNC

USB_DIG_DM / USB_DIG_DP

R432 33R
I2S_DATA_DVB
I2S_WS_DVB
I2S_CLK_DVB
XTAL_PWM
C269 100N 10V
100R
R319
RF_AGC_DVB
C300 1n 50V
C301 1n 50V
C268 100N 10V
C267 100N 10V
C255 100N 10V
C265 100N 10V
C291 10u 10V
10K
R788
R785
3V3_VCC
S214
DIGITAL_IF-
390nH
L115
C619 1U
47p 50V
Place after QAM
S215
DIGITAL_IF+
C276 100N 10V
C274 100N 10V
C275 100N 10V
C286 10u 10V
C285 10u 10V
F141 330R
1V8_VCC
F140 330R
3V3_VCC

DVB RESET

3V3D_DVB
R375 10K
RESET_DVB
DVB_RESET
R185 33R
C251 100N 10V
USB Connector GND

VESTEL	PROJECT NAME : 17MB35-1	A3
SCH NAME : DVB MPEG DECODER & SDRAM	SHEET: 9 OF: 12	
DRAWN BY : ULAS DERELI	4-16-2008_14:01	

A/D DIMMING SELECTION

CN117

W/IDTV Option

U137 MP1583

VFD

U136 MP1583

17PW26 CONNECTOR

U145 MP2112

U144 MP2112

U122 LM1117

VFD OPTION

PAULO DECOUPLING CAPACITORS

U121 LM1117

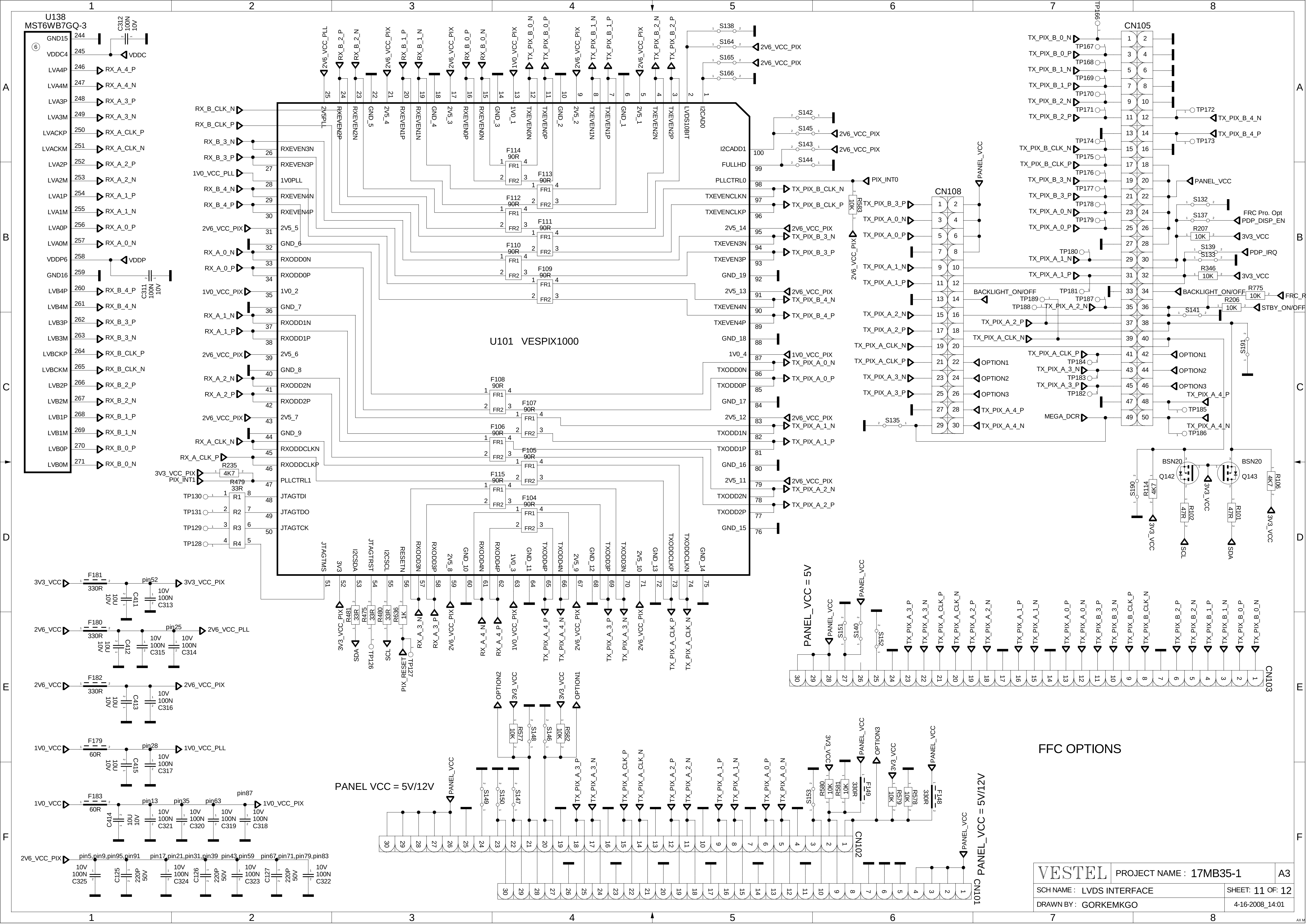
SHORT CCT PROTECTION

PANEL SUPPLY SWITCH

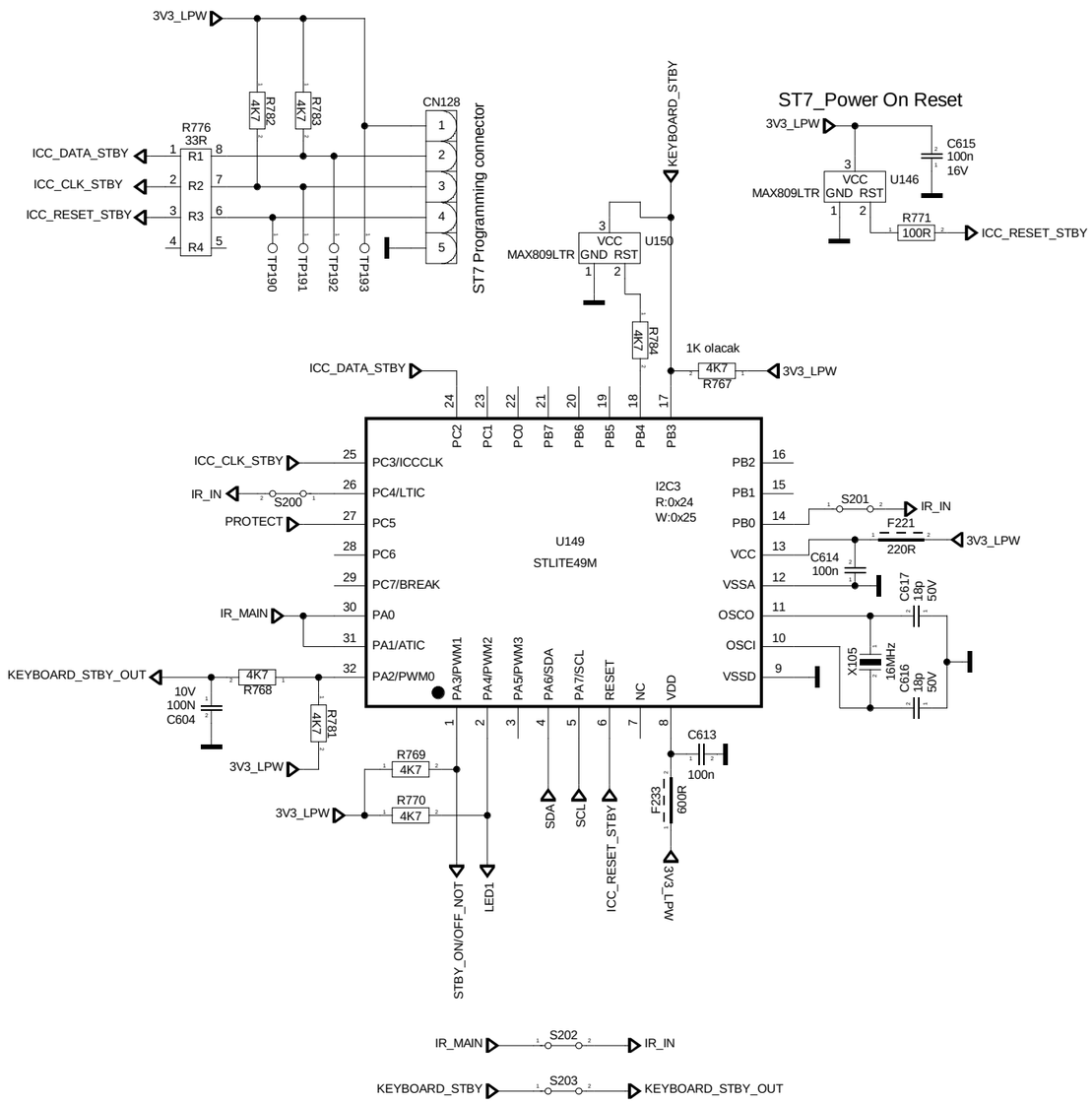
CN126

17IPS15 CONNECTOR

VESTEL	PROJECT NAME : 17MB35-1		A3
SCH NAME : MB34 POWER		SHEET: 10 OF: 12	
DRAWN BY : GORKEMKGO		4-16-2008_14:01	



U138
MST6WB7GQ-3
U101 VESPIX1000
CN105
CN108
CN103
CN102
CN101
FFC OPTIONS
PANEL VCC = 5V/12V
PANEL_VCC = 5V
PANEL_VCC = 5V/12V
FRC Pro. Opt
PDP_DISP_EN
PDP_IRQ
BACKLIGHT_ON/OFF
STBY_ON/OFF
MEGA_DCR
BSN20
Q142
Q143
3V3_VCC
2V6_VCC
1V0_VCC
3V3_VCC_PIX
2V6_VCC_PLL
2V6_VCC_PIX
1V0_VCC_PLL
1V0_VCC_PIX
VESTEL
PROJECT NAME : 17MB35-1
A3
SCH NAME : LVDS INTERFACE
SHEET: 11 OF: 12
DRAWN BY : GORKEMKGO
4-16-2008_14:01



IC altina yerlestirilebilinir

VESTEL	PROJECT NAME : 17MB35-1		A3
SCH NAME : STBY UCONTROLLER		SHEET: 12 OF: 12	
DRAWN BY : MB35 HW GROUP		4-16-2008_14:01