

T-4007-05

KS54AHCT 174/175
KS74AHCT

Hex/Quad D-type Flip-Flops with Clear

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 KS74AHCT: -40°C to $+85^{\circ}\text{C}$
 KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

The '174 contains six, and the '175 contains four D-type flip-flops all sharing a common clock and a common clear. The '174 features single rail outputs for every flip-flops whereas the '175 has complementary outputs.

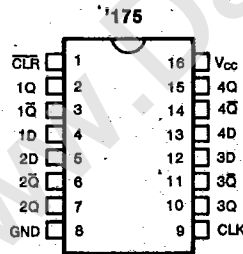
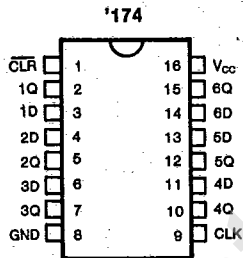
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS

FUNCTION TABLE



(Each Flip-Flop)

Inputs			Outputs	
CLR	CLK	D	Q	Q̄†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q ₀	Q̄ ₀

† '175 only

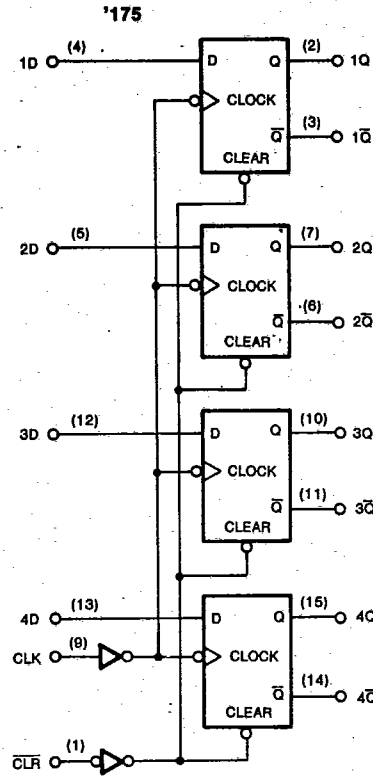
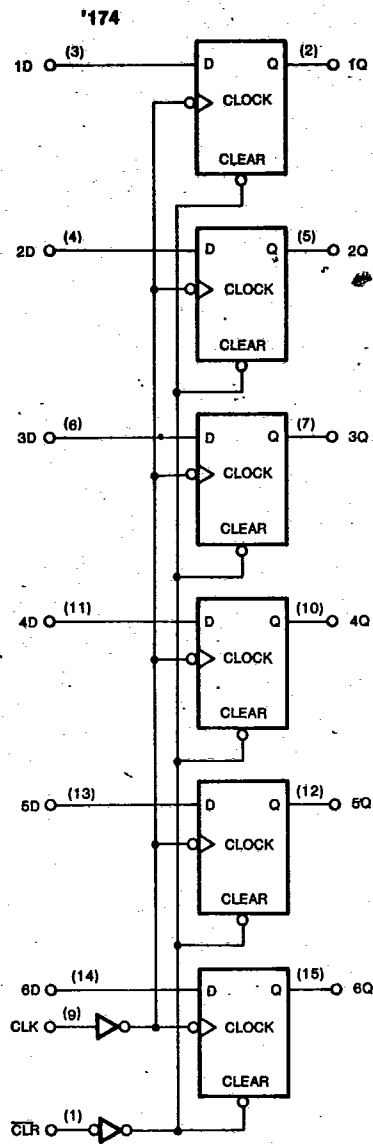


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KS54AHCT 174/175
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Hex/Quad D-type Flip-Flops
with Clear T-46-07-05

LOGIC DIAGRAMS



KS54AHCT 174/175
KS74AHCT

Hex/Quad D-type Flip-Flops
with Clear T-46-07-05

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{stg} -65°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}
 Operating Temperature
 Range KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
 Input Rise & Fall Times, t_r , t_f Max 500 ns
 * Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ C$			Unit	
			Typ	KS74AHCT $T_a = -40^\circ C$ to $+85^\circ C$	KS54AHCT $T_a = -55^\circ C$ to $+125^\circ C$		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu A$ $I_O = -4mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu A$ $I_O = 4mA$ $I_O = 8mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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KS54AHCT
KS74AHCT **174/175****Hex/Quad D-type Flip-Flops
with Clear T-46-07-05****AC ELECTRICAL CHARACTERISTICS** (Input $t_r, t_f \leq 2$ ns, AHCT174, AHCT175)

Characteristic	Symbol	Conditions†	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	f_{max}	$C_L = 50\text{pF}$	70	50		40		MHz
Propagation Delay, CLK to Q or \bar{Q}	t_{PLH}		11		17		20	ns
	t_{PHL}		11		17		20	ns
Propagation Delay, $\bar{\text{CLR}}$ to Q or \bar{Q}	t_{PLH}		12		21		25	ns
	t_{PHL}		12		21		25	ns
Setup Time before CLK†	Data	t_{su}	6	10		15		ns
	$\bar{\text{CLR}}$ Inactive		4	6		8		ns
Hold Time, Data after CLK†		t_{h}	-3	0		0		ns
Pulse Width	CLK High or Low	t_w	6	10		15		ns
	$\bar{\text{CLR}}$ Low		6	10		15		ns
Input Capacitance		C_{IN}	5					pF
Power Dissipation Capacitance*		C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{\text{PD}} V_{CC}^2 f + I_{CC} V_{CC}$.

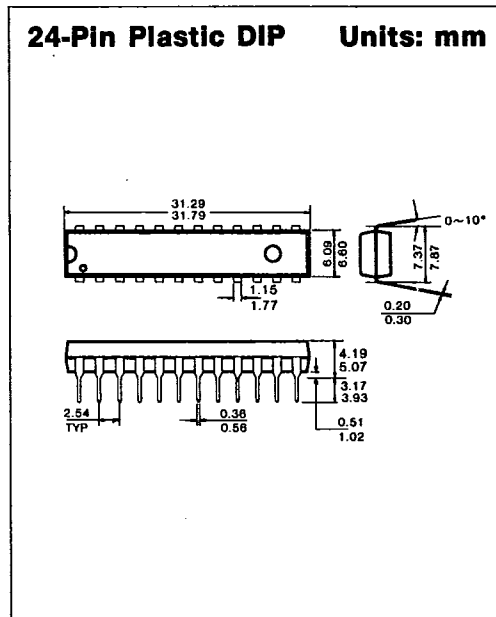
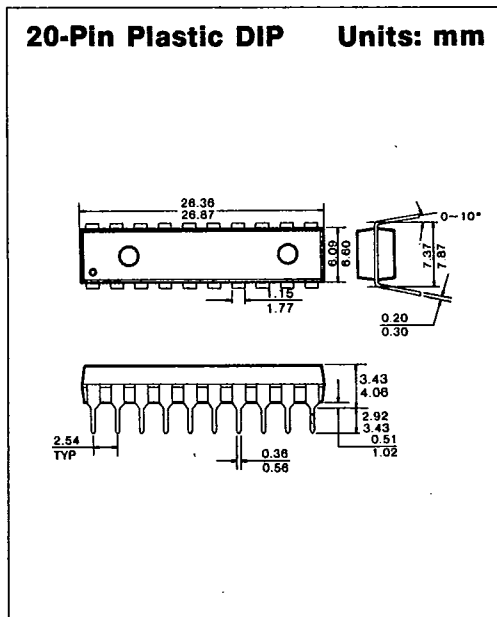
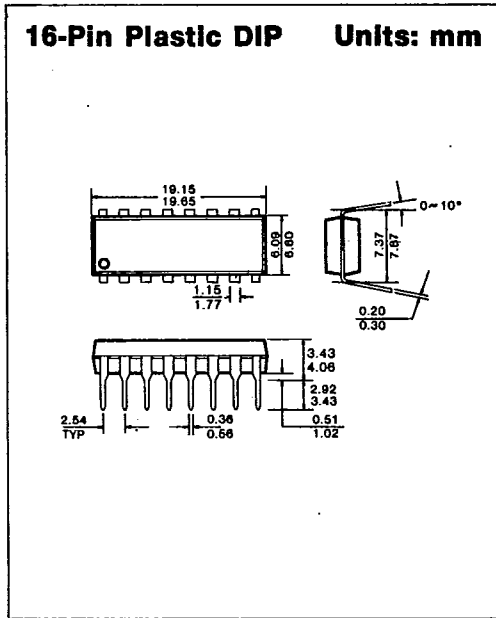
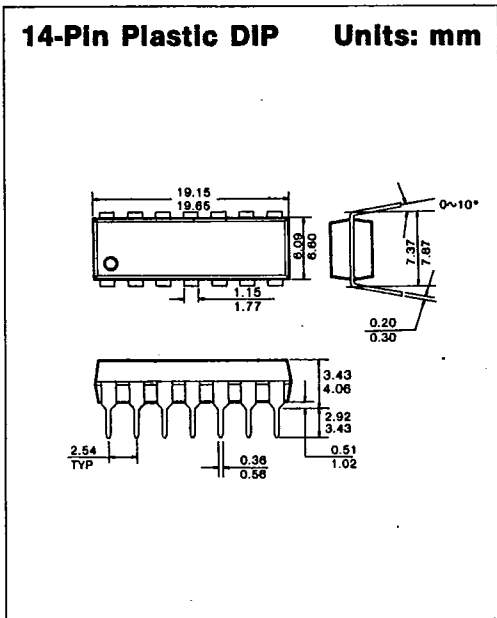
† For AC switching test circuits and timing waveforms see section 2.



PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES

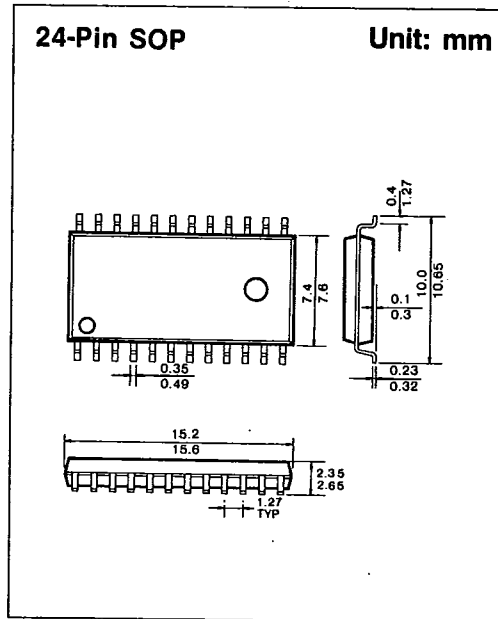
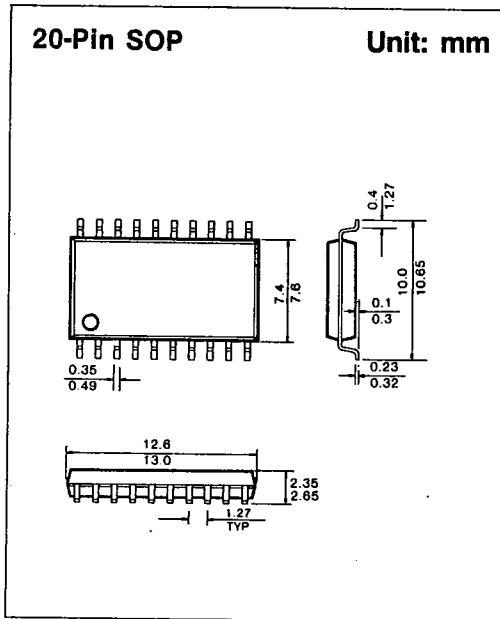
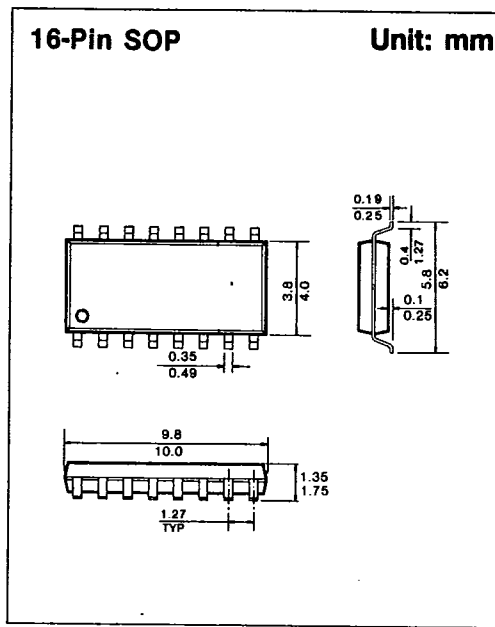
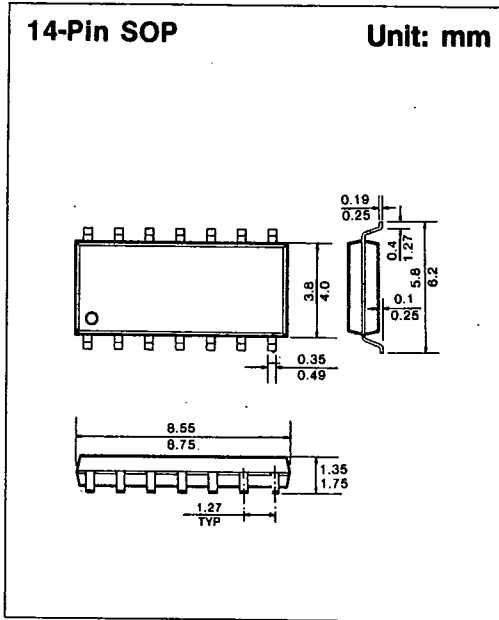


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PACKAGE DIMENSIONS

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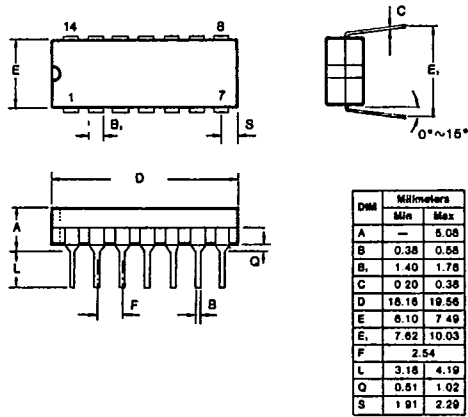


PACKAGE DIMENSIONS

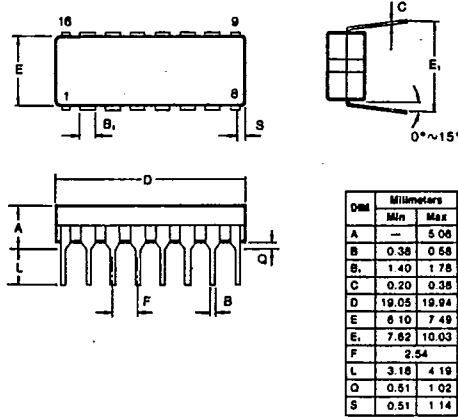
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2. CERAMIC PACKAGES

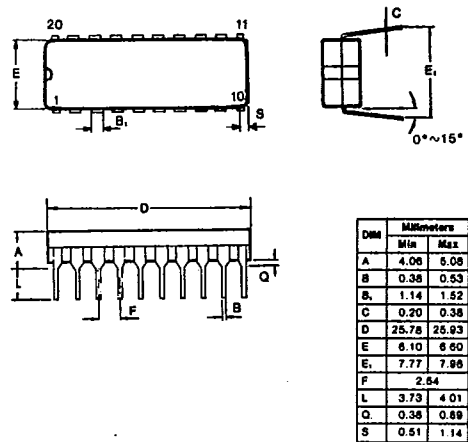
14-Pin Ceramic DIP Units: mm



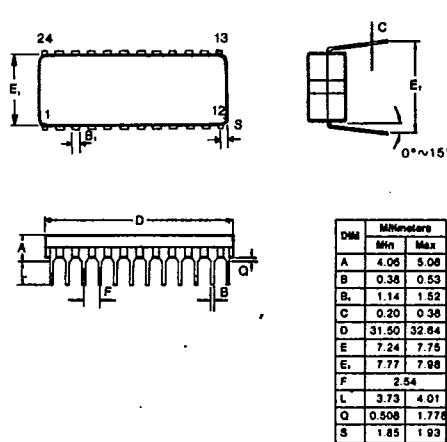
16-Pin Ceramic DIP Units: mm



20-Pin Ceramic DIP Units: mm



24-Pin Ceramic DIP Units: mm



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