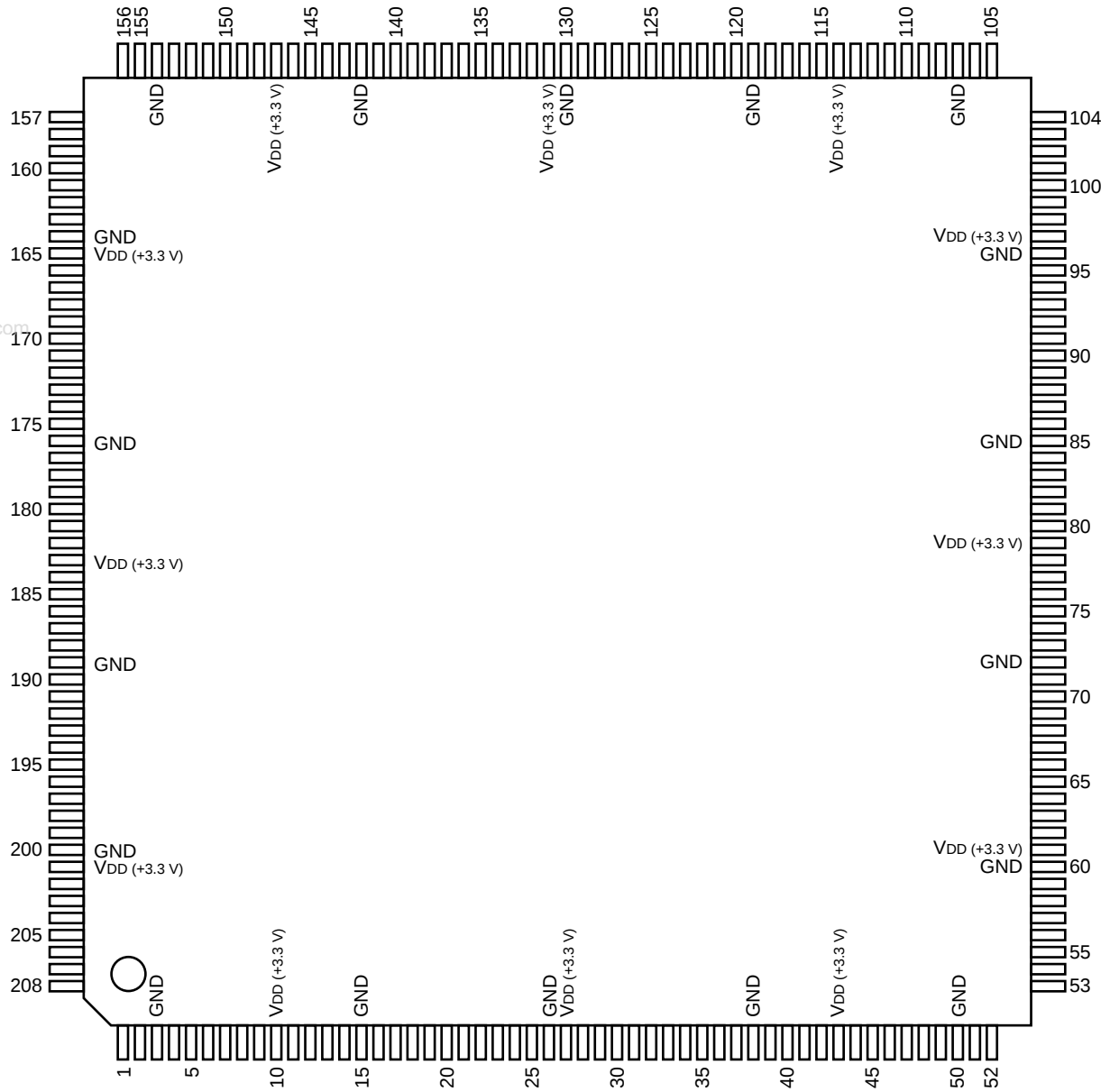

C-MOS SDDI VIDEO DEPACKING (GATE ARRAY)

- TOP VIEW -



(V_{DD} = +3.3 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	DIN9	43	—	V _{DD}	85	—	GND	127	O	REB13	169	O	OUTFRM
2	I	DIN8	44	O	INT	86	O	WEA22	128	O	REB12	170	O	DEC17
3	—	GND	45	O	ATWRST	87	O	WEA21	129	O	REB11	171	O	DEC16
4	I	DIN7	46	O	SYSWRST	88	O	WEA20	130	—	GND	172	O	DEC15
5	I	DIN6	47	O	ATWE	89	O	WEB23	131	—	V _{DD}	173	O	DEC14
6	I	DIN5	48	O	SYSWE	90	O	WEB22	132	O	REB10	174	O	DEC13
7	I	DIN4	49	O	VEXIST	91	O	WEB21	133	O	RSTR1B	175	O	DEC12
8	I	DIN3	50	—	GND	92	O	WEB20	134	I	MD27	176	—	GND
9	I	DIN2	51	O	AEXIST	93	O	BSELH2	135	I	MD26	177	O	DEC11
10	—	V _{DD}	52	O	CPUCF	94	O	OBANK1	136	I	MD25	178	O	DEC10
11	I	DIN1	53	O	D1SEL	95	I	BANK1	137	I	MD24	179	O	DEC1SYNC
12	I	DIN0	54	I	INCLK	96	—	GND	138	I	MD23	180	O	DEC1PTY
13	I	INF	55	O	MDOUT7	97	—	V _{DD}	139	I	MD22	181	O	DEC1ERR
14	I	INV	56	O	MDOUT6	98	O	OBANK2	140	I	MD21	182	O	ASELH2
15	—	GND	57	O	MDOUT5	99	I	BANK2	141	I	MD20	183	—	V _{DD}
16	I	INH	58	O	MDOUT4	100	I	MD17	142	—	GND	184	I	XACK
17	I	INPTY	59	O	MDOUT3	101	I	MD16	143	I	MSYNC2	185	I	BCK
18	I	VINT	60	—	GND	102	I	MD15	144	I	MERR2	186	I	XTCK
19	I	VEN	61	—	V _{DD}	103	I	MD14	145	I	MPTY2	187	O	DEC27
20	I	AIN	62	O	MDOUT2	104	I	MD13	146	O	OEA23	188	O	DEC26
21	I	AEN	63	O	MDOUT1	105	I	MD12	147	—	V _{DD}	189	—	GND
22	I	PCERD	64	O	MDOUT0	106	I	MD11	148	O	OEA22	190	O	DEC25
23	I	SWDET	65	O	MDOSYNC	107	—	GND	149	O	OEA21	191	O	DEC24
24	I	LNEC	66	O	MDOERR	108	I	MD10	150	O	OEA20	192	O	DEC23
25	O	ASELH1	67	O	MDOPTY	109	I	MSYNC1	151	O	REA23	193	O	DEC22
26	—	GND	68	O	WRA	110	I	MERR1	152	O	REA22	194	O	DEC21
27	—	V _{DD}	69	O	WRB	111	I	MPTY1	153	O	REA21	195	O	DEC20
28	I	RST	70	O	WEA13	112	O	OEA13	154	—	GND	196	O	DEC2SYNC
29	I/O	SYSI07	71	O	WEA12	113	O	OEA12	155	O	REA20	197	O	DEC2PTY
30	I/O	SYSI06	72	—	GND	114	—	V _{DD}	156	O	RSTR2A	198	O	DEC2ERR
31	I/O	SYSI05	73	O	WEA11	115	O	OEA11	157	O	OEB23	199	O	BSELH1
32	I/O	SYSI04	74	O	WEA10	116	O	OEA10	158	O	OEB22	200	—	GND
33	I/O	SYSI03	75	O	WEB13	117	O	REA13	159	O	OEB21	201	—	V _{DD}
34	I/O	SYSI02	76	O	WEB12	118	O	REA12	160	O	OEB20	202	I	OUTCLK
35	I/O	SYSI01	77	O	WEB11	119	—	GND	161	O	REB23	203	I	TEST0
36	I/O	SYSI00	78	O	WEB10	120	O	REA11	162	O	REB22	204	I	TEST1
37	I	STATE1	79	—	V _{DD}	121	O	REA10	163	O	REB21	205	I	TEST2
38	—	GND	80	I	XSM	122	O	RSTR1A	164	—	GND	206	I	REFHD
39	I	STATE0	81	I	XTST	123	O	OEB13	165	—	V _{DD}	207	I	REFVD
40	I	STRB	82	I	SDI0	124	O	OEB12	166	O	REB20	208	I	REFCFI
41	I	CS	83	O	SDO0	125	O	OEB11	167	O	RSTR2B			
42	O	HRST	84	O	WEA23	126	O	OEB10	168	I	OSDRW			

INPUT

$\overline{\text{AEN}}$	; ATTRIBUTE DATA ENABLE
$\overline{\text{AINT}}$	; ATTRIBUTE DATA INTERRUPT
BANK1, BANK2	; FIFO MEMORY BANK SELECT1, 2
BCK	; TEST
$\overline{\text{CS}}$	; CPU I/F (CHIP SELECT)
DIN0 - DIN9	; SDDI DATA
INCLK	; INPUT CLOCK
INF	; INPUT FRAME PULSE
$\overline{\text{INH}}$	; INPUT H PULSE
INPTY	; INPUT PARITY
INV	; INPUT V PULSE
$\overline{\text{LNEC}}$	; FIFO MEMORY SELECT
MD10 - MD17	; FIFO MEMORY INPUT DATA1
MD20 - MD27	; FIFO MEMORY INPUT DATA2
MERR1, MERR2	; FIFO MEMORY INPUT ERROR1, 2
MPTY1, MPTY2	; FIFO MEMORY INPUT PARITY1, 2
$\overline{\text{MSYNC1}}, \overline{\text{MSYNC2}}$	; FIFO MEMORY INPUT SYNC1, 2
OSDRW	; EXTERNAL LOCK
OUTCLK	; OUTPUT CLOCK
PCERD	; SDDI ERROR
REFCFI	; REFERENCE CF INFORMATION
$\overline{\text{REFHD}}$	; REFERENCE HD
$\overline{\text{REFVD}}$	; REFERENCE VD
$\overline{\text{RST}}$	; RESET
SDIO	; TEST
STATE0, STATE1	; CPU I/F (MODE SELECT)
$\overline{\text{STRB}}$	; CPU I/F (STROBE)
$\overline{\text{SWDET}}$	; SDDI SWITCHING DETECT
TEST0 - TEST2	; TEST
$\overline{\text{VEN}}$	; VIDEO DATA ENABLE
$\overline{\text{VINT}}$	; VIDEO DATA INTERRUPT
XACK	; TEST
XSM	; TEST
XTCK	; TEST
XTST	; TEST

OUTPUT

<u>AEXIST</u>	; ATTRIBUTE EXIST
<u>ASELH1, ASELH2</u>	; FIFO MEMORY READ SELECT (A)
<u>ATWE</u>	; FIFO MEMORY WRITE ENABLE (ATTRIBUTE)
<u>ATWRST</u>	; FIFO MEMORY WRITE RESET (ATTRIBUTE)
<u>BSELH1, BSELH2</u>	; FIFO MEMORY READ SELECT (B)
<u>CPUCF</u>	; INPUT CF PULSE
<u>D1SEL</u>	; DECODER SELECT
<u>DEC0 - DEC17</u>	; VIDEO STREAM DATA1
<u>DEC1ERR</u>	; STREAM ERROR1
<u>DEC1PTY</u>	; STREAM PARITY1
<u>DEC1SYNC</u>	; STREAM SYNC1
<u>DEC0 - DEC27</u>	; VIDEO STREAM DATA2
<u>DEC2ERR</u>	; STREAM ERROR2
<u>DEC2PTY</u>	; STREAM PARITY2
<u>DEC2SYNC</u>	; STREAM SYNC2
<u>HRST</u>	; FIFO MEMORY WRITE RESET (1H DELAY)
<u>INT</u>	; CPU INTERRUPT
<u>MDOERR</u>	; FIFO MEMORY OUTPUT ERROR
<u>MDOPTY</u>	; FIFO MEMORY OUTPUT PARITY
<u>MDOSYNC</u>	; FIFO MEMORY OUTPUT SYNC
<u>MDOUT0 - MDOUT7</u>	; FIFO MEMORY OUTPUT DATA
<u>OBANK1, OBANK2</u>	; FIFO MEMORY BANK SELECT1, 2
<u>OEA10 - OEA13</u>	; FIFO MEMORY OUTPUT ENABLE (1A)
<u>OEA20 - OEA23</u>	; FIFO MEMORY OUTPUT ENABLE (2A)
<u>OEB10 - OEB13</u>	; FIFO MEMORY OUTPUT ENABLE (1B)
<u>OEB20 - OEB23</u>	; FIFO MEMORY OUTPUT ENABLE (2B)
<u>OUTFRM</u>	; OUTPUT FRAME PULSE
<u>REA10 - REA13</u>	; FIFO MEMORY READ ENABLE (1A)
<u>REA20 - REA23</u>	; FIFO MEMORY READ ENABLE (2A)
<u>REB10 - REB13</u>	; FIFO MEMORY READ ENABLE (1B)
<u>REB20 - REB23</u>	; FIFO MEMORY READ ENABLE (2B)
<u>RSTR1A</u>	; FIFO MEMORY READ RESET (1A)
<u>RSTR1B</u>	; FIFO MEMORY READ RESET (1B)
<u>RSTR2A</u>	; FIFO MEMORY READ RESET (2A)
<u>RSTR2B</u>	; FIFO MEMORY READ RESET (2B)
<u>SDO0</u>	; TEST
<u>SYSWE</u>	; FIFO MEMORY WRITE ENABLE (SYS)
<u>SYSWRST</u>	; FIFO MEMORY WRITE RESET (SYS)
<u>VEXIST</u>	; VIDEO DATA EXIST
<u>WEA10 - WEA13</u>	; FIFO MEMORY WRITE ENABLE (1A)
<u>WEA20 - WEA23</u>	; FIFO MEMORY WRITE ENABLE (2A)
<u>WEB10 - WEB13</u>	; FIFO MEMORY WRITE ENABLE (1B)
<u>WEB20 - WEB23</u>	; FIFO MEMORY WRITE ENABLE (2B)
<u>WRA</u>	; FIFO MEMORY WRITE RESET (A)
<u>WRB</u>	; FIFO MEMORY WRITE RESET (B)

INPUT/OUTPUT

SYSIO0 - SYSIO7 ; CPU I/F (ADDRESS & DATA)