ANALOG DEVICES

# High Performance Analog to Digital Converter

# ADC1133

**FEATURES**
**12 Bit Resolution**
**Very Small Module Package**
**No Missing Codes: 0 to +70°C**
**25μs Conversion Time**
**Programmable Input Ranges**




## GENERAL DESCRIPTION

The ADC1133 is a high performance, 12-bit A/D converter packaged in an exceptionally compact 2" x 2" x 0.4" (51 x 51 x 10mm) module. Using the successive approximations technique, it performs complete conversions in less than 25μs. Performance specifications include ±7.5ppm/°C gain temperature coefficient, ±½LSB linearity error and no missing codes from 0 to +70°C.

The ADC1133 combines the AD562 integrated circuit D/A with a precision reference source, a high speed comparator, and successive approximations logic to form a complete converter package. The laser trimmed AD562, which consists of precision current switches and a very stable thin film resistor network, provides the ADC1133 with very good performance over temperature and makes possible its small module size.

## TIMING

As shown in Figure 1, the "0" to "1" transition of the CONVERT COMMAND input sets the MSB output to logic "0" and the CLOCK, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to logic "1". Nothing further happens until the CONVERT COMMAND returns to logic "0", at which time the conversion proceeds.

With the MSB in the logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to logic "1". If the D/A output is greater than the analog input, the MSB remains at logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to logic "0" and another comparison is made. This process continues through each successive bit until the BIT 12 (LSB) comparison is completed. At this time the STATUS output returns to logic "0" and the conversion cycle ends.

The SERIAL DATA output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, 40ns after each of the twelve "0" to "1" clock transitions.

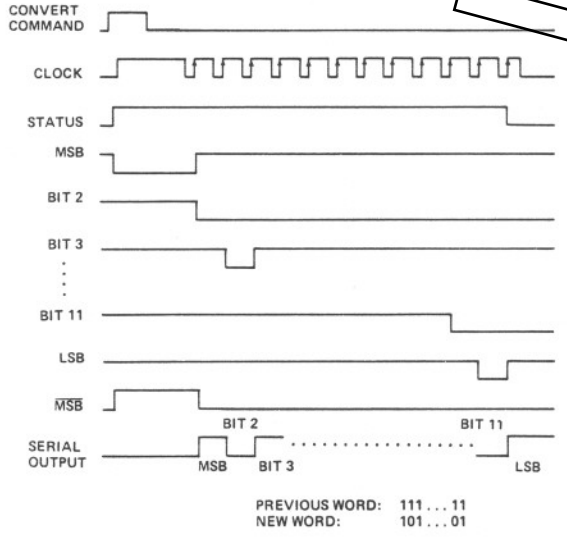


*Figure 1. Timing Diagram*



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Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783 Mid-West 312/894-3300 Texas 214/231-5094

# SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

| | |
|---|---|
| RESOLUTION | 12 Bits |
| CONVERSION TIME[1] | 25μs max |
| ACCURACY[2] | |
| Error Relative to Full Scale | ±½LSB max |
| Quantization Error | ±½LSB max |
| Differential Nonlinearity Error | ±½LSB (±1LSB max) |
| TEMPERATURE COEFFICIENTS | |
| Gain | ±7.5ppm/°C (±15ppm/°C max) |
| Offset (Unipolar Inputs) | ±25μV/°C (±40μV/°C max) |
| Offset (Bipolar Inputs) | ±25μV/°C (±40μV/°C max) |
| Differential Nonlinearity | ±2.8ppm/°C (±3ppm/°C max) |
| Missing Codes | No Missing Codes 0 to +70°C |
| INPUT VOLTAGE RANGES | ±5V, ±10V, 0 to +10V |
| INPUT IMPEDANCE | |
| ±5V, 0 to +10V Range | 5kΩ |
| ±10V Range | 10kΩ |
| CONVERT COMMAND | Positive Pulse, TTL Compatible<br>100ns min width |
| PARALLEL DATA OUTPUT | |
| Unipolar Inputs | Positive True Binary |
| Bipolar Inputs | Positive True Offset Binary or<br>Two's Complement |
| SERIAL DATA OUTPUT | |
| Unipolar Inputs | Positive True Binary |
| Bipolar Inputs | Positive True Offset Binary, TTL Compatible, NRZ Format, MSB First |
| STATUS OUTPUT | Logic "1" During Conversion<br>TTL Compatible |
| CLOCK OUTPUT | 480kHz, TTL Compatible |
| LOGIC FANOUTS AND LOADING | |
| Convert Command | 1TTL Load |
| Parallel Data Outputs | 6TTL Loads/Bit |
| Status Output | 4TTL Loads |
| $\overline{\text{Status}}$ Output | 10TTL Loads |
| Serial Data Output | 6TTL Loads |
| Clock Output | 9TTL Loads |
| ADJUSTMENT RANGES | |
| Gain | ±5LSB min |
| Offset | ±10LSB min |
| POWER REQUIREMENTS | +5VDC ±5% @ 120mA (160mA max)<br>+15VDC ±3% @ 15mA (20mA max)<br>-15VDC ±3% @ 25mA (30mA max) |
| POWER SUPPLY SENSITIVITY[3] | |
| Gain | ±1.5mV/V |
| Offset | ±1.5mV/V |
| Reference | ±0.5mV/V |
| TEMPERATURE RANGE | |
| Operating | 0 to +70°C |
| Storage | -55°C to +85°C |
| PRICE (1-9) | $159 |

[1] Conversion time is measured from the trailing edge of the convert command to the "1" to "0" transition of the status output.

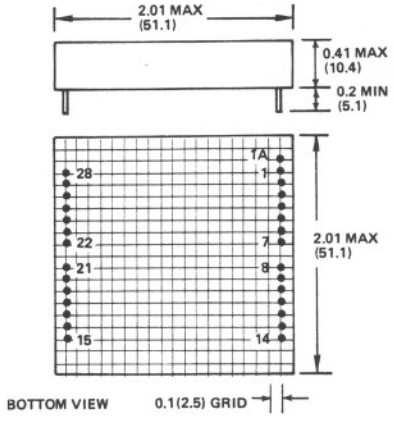
[2] Warmup time to rated accuracy is 5 minutes.

[3] Specification applies only when tracking +15V and -15V supplies are used, and for slowly occuring variations in power supply voltages.

Specifications subject to change without notice.

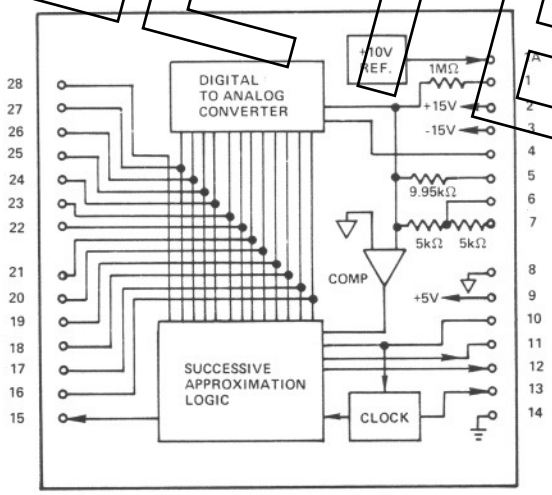
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).




Pins are half hard brass, gold plated per MIL–G–45204B, Class I, Type II. Pin Diameter is 0.019" (0.483mm) ±0.001" (0.025mm).
For plug-in mounting card, order Board No. AC1505 @ $30.

## BLOCK DIAGRAM AND PIN DESIGNATIONS




| | | | |
|---|---|---|---|
| 1A | REF. OUT | 15 | SERIAL OUT |
| 1 | OFFSET ADJUST | 16 | BIT 12 (LSB) |
| 2 | +15V | 17 | BIT 11 |
| 3 | -15V | 18 | BIT 10 |
| 4 | GAIN ADJ. | 19 | BIT 9 |
| 5 | BIP. OFFSET | 20 | BIT 8 |
| 6 | 10V INPUT | 21 | BIT 7 |
| 7 | 20V INPUT | 22 | BIT 6 |
| 8 | ANALOG GND. | 23 | BIT 5 |
| 9 | +5V | 24 | BIT 4 |
| 10 | CONV. COMM. | 25 | BIT 3 |
| 11 | STATUS | 26 | BIT 2 |
| 12 | $\overline{\text{STATUS}}$ | 27 | BIT 1 (MSB) |
| 13 | CLOCK OUT | 28 | $\overline{\text{MSB}}$ |
| 14 | DIGITAL GND. | | |

## MODULE CONNECTIONS

Figure 2 shows the connections required to operate the ADC1133 with a ±10V input range (except for connections to the bit and STATUS digital outputs, which are obvious). This figure also shows the power supply bypass capacitors that are recommended on page 4.

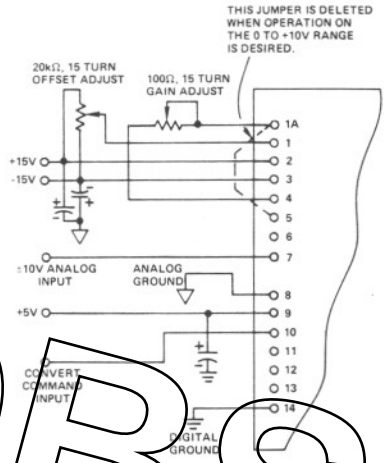



*Figure 2. Module Connections*

The ADC1133 can be operated with an input range of ±5V by connecting the analog input to pin 6 instead of pin 7. Operation on the 0 to +10V range is achieved by deleting the jumper between pins 1A and 5, and connecting the analog input to pin 6.

If an input impedance of greater than 5kΩ on the ±5V or 0 to +10V ranges, or 10kΩ on the ±10V range is desired, an operational amplifier input buffer will be required. The Analog Devices AD509 fast settling integrated circuit differential amplifier would be an ideal choice.

## PARALLEL DATA OUTPUT

The ADC1133 produces natural Binary coded outputs when configured as a unipolar device; as a bipolar device it can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by pin 27 (the MSB output) for Binary and Offset Binary codes and by the pin 28 (the $\overline{\text{MSB}}$ output) for the Two's Complement code. Tables I and II below illustrate the relationship between the analog input and digital output for all three codes.

| ANALOG INPUT | DIGITAL OUTPUT |
|---|---|
| | BINARY CODE |
| +9.9976V | 111111111111 |
| +5.0000V | 100000000000 |
| +1.2500V | 001000000000 |
| +0.0024V | 000000000001 |
| +0.0000V | 000000000000 |

*Table I. Nominal Unipolar Input-Output Relationships*

The user should note that under worst case conditions, the LSB output will not be valid until 28ns after the "1" to "0" transition of the STATUS output. If this is not properly accounted for in the design of the external digital circuitry, the LSB might always appear as a "0" to the system.

| ANALOG INPUT | | DIGITAL OUTPUT | |
|---|---|---|---|
| ±5V RANGE | ±10V RANGE | OFFSET BINARY CODE | TWO'S COMPLEMENT CODE |
| +4.9976V | +9.9951V | 111111111111 | 011111111111 |
| +2.5000V | +5.0000V | 110000000000 | 010000000000 |
| +0.0024V | +0.0049V | 100000000001 | 000000000001 |
| +0.0000V | +0.0000V | 100000000000 | 000000000000 |
| -5.0000V | -10.0000V | 000000000000 | 100000000000 |

*Table II. Nominal Bipolar Input-Output Relationships*

## GAIN AND OFFSET ADJUSTMENTS

The ADC1133 is calibrated with external gain and offset adjustment potentiometers connected as shown in Figure 2. The offset adjustment potentiometer has an adjustment range of at least ±10LSB's, and the gain range adjustment potentiometer has an adjustment range of at least ±5LSB's.

Offset calibration is not affected by changes in gain calibration, and should therefore be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within ±1/10LSB of the desired value at any point within its range.

These adjustments are not made with zero and full scale input signals, and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the converter to be on the verge of switching between two adjacent digital outputs, the unit can be calibrated so that it does switch at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' Conversion Handbook gives more detailed information on testing and calibrating A/D converters.

## OFFSET CALIBRATION

For unipolar units set the input voltage precisely to +0.0012V and adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V bipolar units set the input voltage precisely to -4.9988V; for ±10V units set it to -9.9976V. Adjust the offset potentiometer until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching 100000000000 to 100000000001.

## GAIN CALIBRATION

Set the input voltage precisely to +9.9963V for unipolar units, +4.9963V for ±5V units, or +9.9926V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the 100Ω variable gain resistor until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.

## POWER SUPPLY AND GROUNDING CONNECTIONS

The ADC1133 requires power supplies of +15V, -15V, and +5V which are connected to pins 2, 3, and 9 respectively. The +5V power supply return and digital return are connected to DIGITAL GROUND (pin 14) while the ±15V supply return and analog signal return are connected to ANALOG GROUND (pin 8). The analog and digital grounds are not connected within the module but it is recommended that they be tied together externally with a short jumper between the two pins. If this is done, care must be taken to assure that no digital signals are present on the analog ground return.

The +5V and ±15V supplies are internally bypassed, but it is recommended that additional bypass capacitors be added externally. The capacitors should be located as near to the module pins as possible. The +5V bypass capacitor should be connected between the +5V input (pin 9) and DIGITAL GROUND (pin 14). The ±15V bypass capacitors should be connected between pin 2 and ANALOG GROUND (pin 8), and between pin 3 and ANALOG GROUND. The capacitors would typically be 10μF (or greater) tantalum types.

## SERIAL DATA OUTPUT

The serial data output, available on pin 15, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the ADC1133.

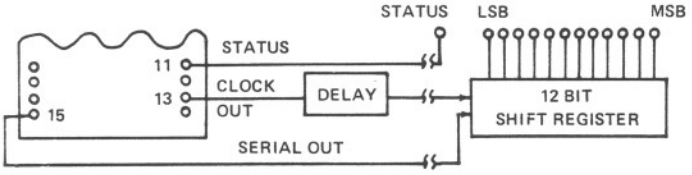



*Figure 3. Serial Data Transmission*

The timing diagram presented in Figure 4 shows that the converter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 40ns maximum CLOCK OUTPUT to SERIAL OUTPUT delay.

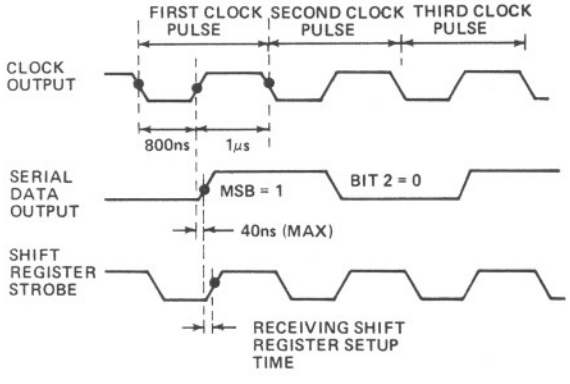



*Figure 4. Serial Data Timing Diagram*

The data appearing in the shift register will be valid a period of time equal to the shift register propagation delay, after the "0" to "1" transition of the last shift register strobe pulse.

## REPETITIVE CONVERSIONS

When making repetitive conversions in the parallel output mode, at least 100ns must be allowed between the completion of one conversion and the beginning of the next. This results in a throughput rate of 39.7kHz. When operating in the serial output mode, an additional period of time may be necessary to assure that the data from one conversion has been completely entered in the receiving shift register before the next conversion is initiated.

## THE AC1505 MOUNTING CARD

The AC1505 mounting card is available to assist in the application of the ADC1133. This 4.5" x 3.0" printed circuit card, shown below in Figure 5, has sockets which allow an ADC1133 to be plugged directly onto it. It includes the necessary gain and offset adjustment potentiometers and power supply bypass capacitors. It mates with a Cinch 251-22-30-160 (or equivalent) edge connector which is supplied with every card. Jumpers can be installed on the printed circuit card to program the analog input range.

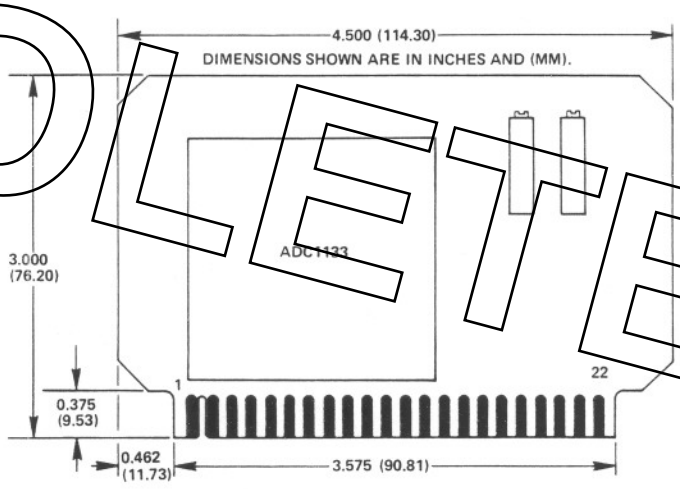



*Figure 5. AC1505 Outline Drawing*



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