262,144 WORD × 4 BIT BiCMOS STATIC RAM **PRELIMINARY**

DESCRIPTION

The TC55B4256P/J is a 1,048,576 bits high speed static random access memory organized as 262,144 words by 4 bits using BiCMOS technology, and operated from a single 5-volt supply. Toshiba's BiCMOS technology and advanced circuit form provide high speed feature.

The TC55B4256P/J has low power feature with device control using Chip Enable ($\overline{CE}$).

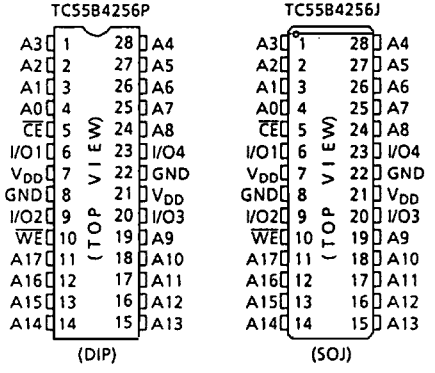
The TC55B4256P/J is suitable for use in various application systems where high speed is required as cache memory, high speed storage, main memory, and so on. All Inputs and Outputs are directly TTL compatible.

The TC55B4256P/J is packaged in a 28 pin standard DIP and SOJ with 400 mil width for high density surface assembly.

FEATURES

- Fast access time :
  - TC55B4256P/J-12 12ns (MAX.)
  - TC55B4256P/J-15 15ns (MAX.)
  - TC55B4256P/J-20 20ns (MAX.)
- Low power dissipation
  - Operation : TC55B4256P/J-12 130mA (MAX.)
  - TC55B4256P/J-15 130mA (MAX.)
  - TC55B4256P/J-20 130mA (MAX.)
  - Standby : 10mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Package
  - TC55B4256P : DIP28-P-400A
  - TC55B4256J : SOJ28-P-400

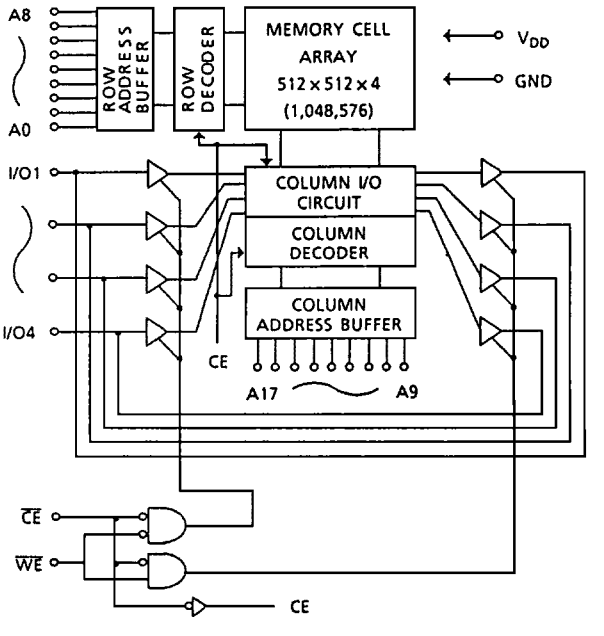
PIN CONNECTION



PIN NAMES

A0~A17	Address Inputs
I/O1~I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Terminal Voltage	-2.0* ~7.0	V
$V_{I/O}$	I/O Terminal Voltage	-0.5* ~V_{DD}+0.5	V
P_D	Power Dissipation	900	mW
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

* : −3V with a pulse width of 10ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* : −3V with a pulse width of 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	-	-	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}	-	-	±10	μA
I_{DDO}	Operating Current	tcycle = Min cycle, $\overline{CE}$ = V_{IL}, Iout = 0mA Other Inputs = V_{IH}/V_{IL}	-	-	130	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Inputs = V_{IH}/V_{IL}	-	-	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Inputs = V_{DD} - 0.2V or 0.2V	-	-	10	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O}$ = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I/O	POWER
Read	L	H	Dout	I_{DDO}
Write	L	L	Din	I_{DDO}
Standby	H	*	High - Z	I_{DDS}

* High or Low

AC CHARACTERISTICS (Ta = 0~70°C [4], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B4256P/J-12		TC55B4256P/J-15		TC55B4256P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	12	-	15	-	20	-	ns
t_{ACC}	Address Access Time	-	12	-	15	-	20	
t_{CO}	Chip Enable Access Time	-	12	-	15	-	20	
t_{COE}	Output Enable Time from $\overline{CE}$	4	-	4	-	4	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	6	-	7	-	8	
t_{OH}	Output Data Hold Time from Address Change	4	-	4	-	4	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	12	-	15	-	20	

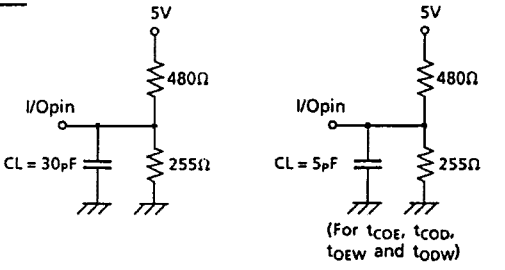
WRITE CYCLE

SYMBOL	PARAMETER	TC55B4256P/J-12		TC55B4256P/J-15		TC55B4256P/J-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	12	-	15	-	20	-	ns
t_{WP}	Write Pulse Width	8	-	9	-	10	-	
t_{AW}	Address Valid to End of Write	9	-	10	-	11	-	
t_{CW}	Chip Enable to End of Write	8	-	9	-	10	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	1	-	1	-	1	-	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	-	1	-	1	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	6	-	7	-	8	
t_{DS}	Data Set Up Time	7	-	8	-	9	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITIONS

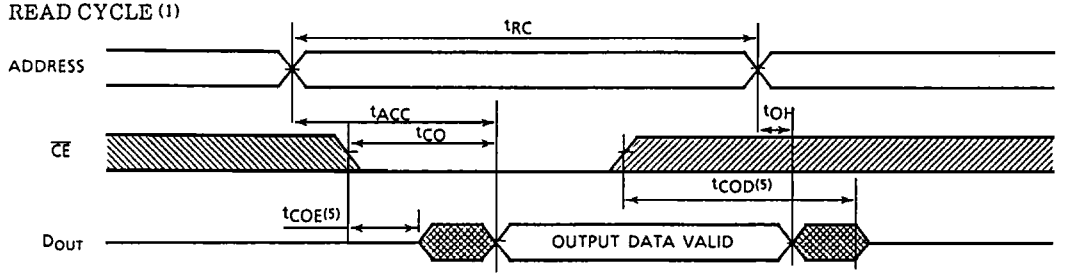
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

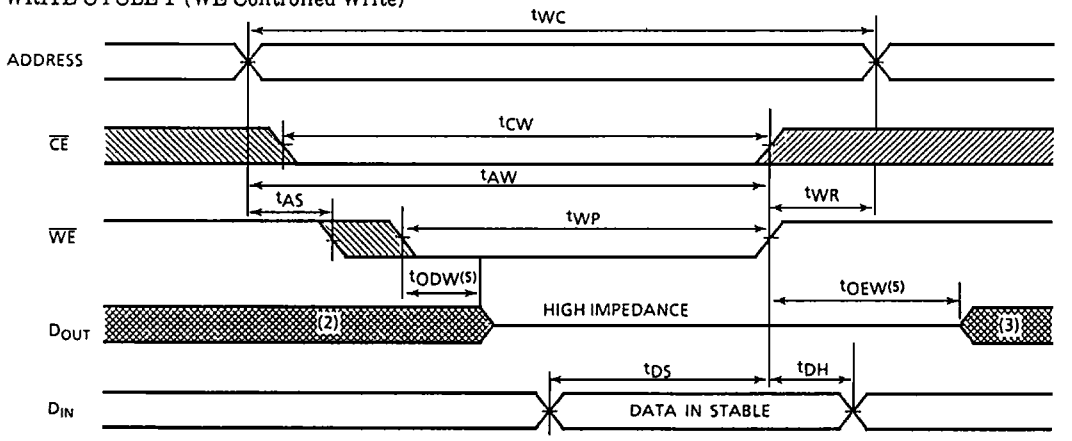


TIMING WAVEFORMS

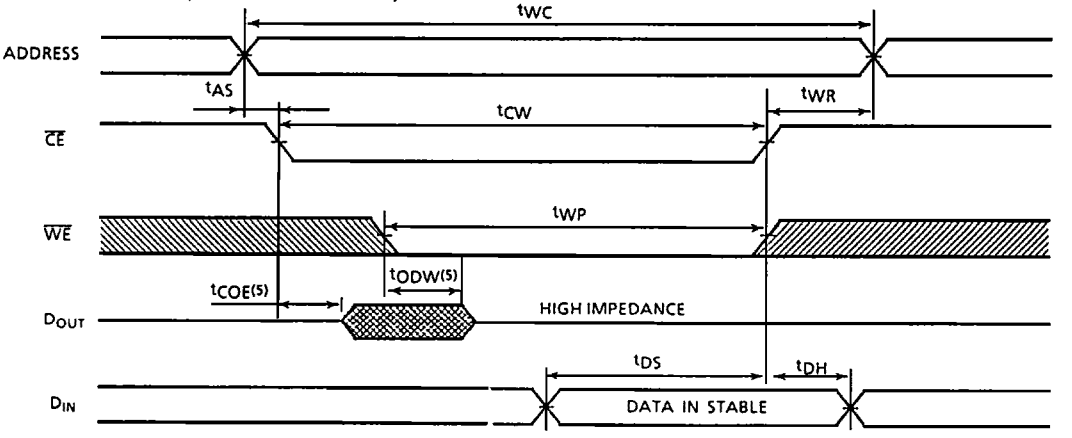
READ CYCLE (1)



WRITE CYCLE 1 ($\overline{WE}$ Controled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controled Write)



Note :

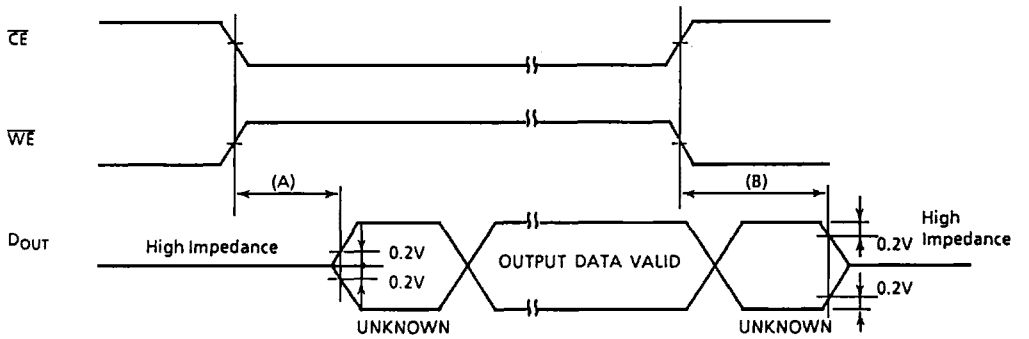
1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

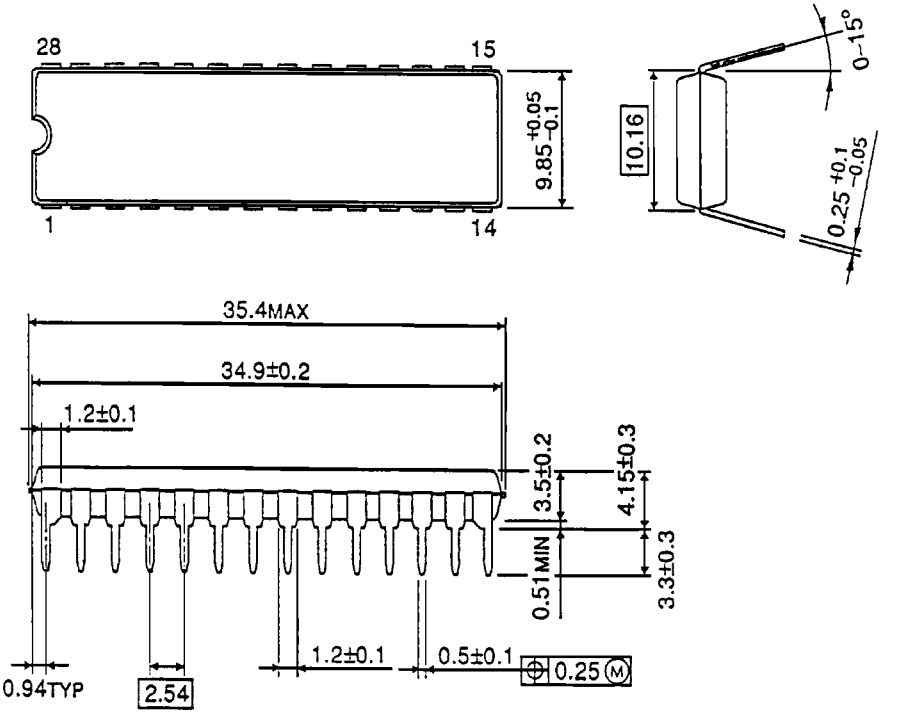
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{COE}, t_{OEW} ..... Output Enable Time
   (B) t_{COD}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28−P−400A)

Unit in mm



OUTLINE DRAWINGS

Plastic SOJ (SOJ28−P−400)

Unit in mm