Zytrex

ZX54AHCT ZX74AHCT **161** ZX54AHCT ZX74AHCT **163**

February 1985

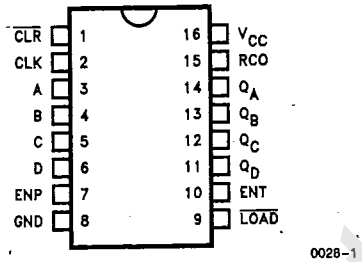
OBJECTIVE SPECIFICATIONS

Synchronous 4-Bit Binary Counters

Features

- **Function, pin-out, speed and drive compatibility with 54/74ALS logic family**
- **Low power consumption characteristic of CMOS**
- **High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  74AHCT: −40°C to +85°C
  54AHCT: −55°C to +125°C

Pin Configuration



0028-1

Function Tables

'161

CLK	CLR	ENP	ENT	LOAD	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disable
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

'163

CLK	CLR	ENP	ENT	LOAD	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

Description

These are synchronous, presettable 4-bit binary counters featuring internal carry-look-ahead for high-speed counting. The buffered clock input triggers all flip-flops simultaneously on the rising edge of the input waveform. This eliminates the output counting spikes normally associated with asynchronous counters.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs.

The clear function for the '163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter.

Two enable inputs and a ripple carry output allow easy cascading of the counters. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or LOAD) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

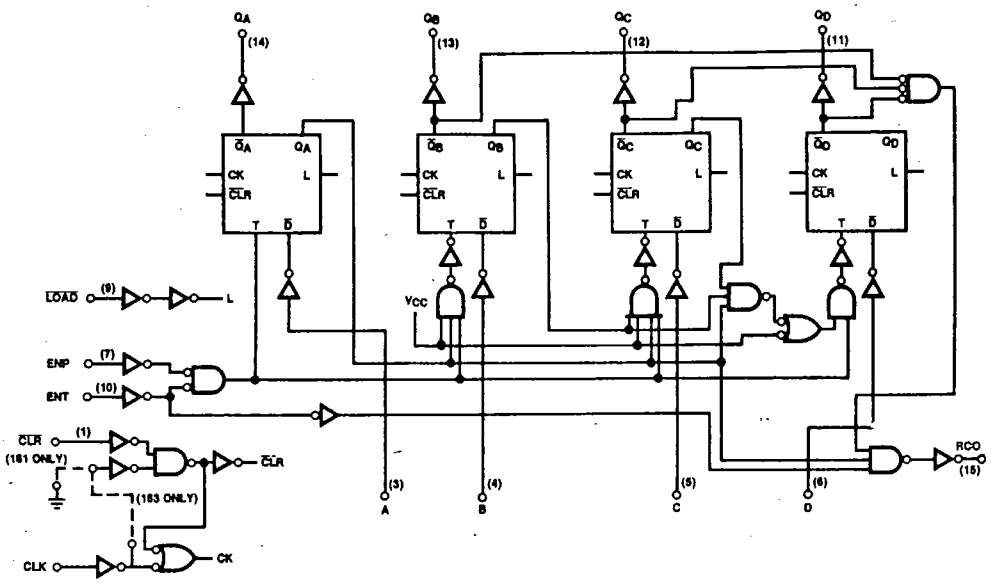
Fabricated using Zytrex's proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Zytrex ZX54AHCT ZX74AHCT **161** ZX54AHCT ZX74AHCT **163**

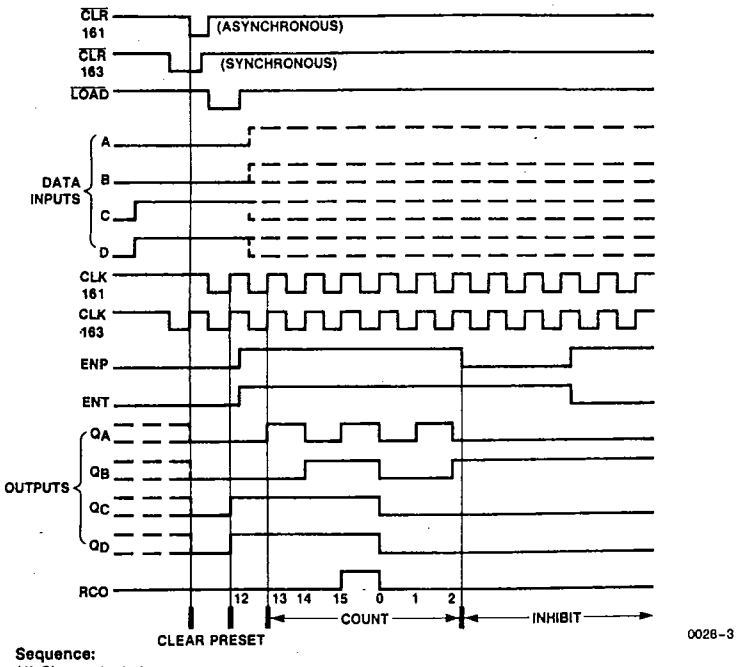
T-45-23-05

Logic Diagram



0028-2

Typical Clear, Preset, Count and Inhibit Sequences



0028-3

Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

Zytrex

ZX54AHCT ZX74AHCT 161 ZX54AHCT ZX74AHCT 163

T-45-23-05

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} ..... −0.5V to 7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} + 0.5V) ..... ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} + 0.5V) ..... ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} + 0.5V) ..... ±35 mA
Continuous Current Through
V_{CC} or GND pins ..... ±125 mA
Storage Temperature Range, T_{STG} .. −65°C to +150°C
Power Dissipation Per Package, P_D† ..... 500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12 mW/°C from 65°C to 85°C
Ceramic Package (J): −12 mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range ZX74AHCT: −40°C to +85°C
ZX54AHCT: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics (V_{CC} = 5V ± 10% Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	T_A = 25°C	74AHCT T_A = −40°C to +85°C	54AHCT T_A = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = −20 μA I_O = −4 mA	V_{CC} 4.2	V_{CC} − 0.1 3.98	V_{CC} − 0.1 3.84	V_{CC} − 0.1 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = 20 μA I_O = 4 mA I_O = 8 mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80.0	160.0	μA

4

Zytrex

ZX54AHCT ZX74AHCT **161** ZX54AHCT ZX74AHCT **163**

T-45-23-05

AC Electrical Characteristics (Input t_r, $t_f \leq 2$ ns), AHCT161

Symbol	Parameter		Conditions†	$T_A = 25°C$ $V_{CC} = 5.0V$	74AHCT $T_A = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	54AHCT $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits		
f_{max}	Maximum Operating Frequency		$C_L = 50$ pF	50	30	25	MHz
t_{PLH}	Maximum Propagation Delay, CLK to RCO			15	25	29	ns
t_{PHL}				15	25	29	
t_{PLH}	Maximum Propagation Delay, CLK to any Q			10	16	19	ns
t_{PHL}				10	16	19	
t_{PLH}	Maximum Propagation Delay, ENT to RCO			8	13	16	ns
t_{PHL}				8	13	16	
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to any Q			15	24	29	ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to RCO			17	28	33	ns
t_w	Minimum Pulse Width	CLK High or Low		10	15	20	ns
		$\overline{CLR}$ Low		10	15	20	
t_{su}	Minimum Setup Time before CLK ↑	A, B, C, D		10	15	20	ns
		$\overline{LOAD}$		10	15	20	
		ENP, ENT		10	15	20	
		$\overline{CLR}$ Inactive		6	10	10	
t_h	Minimum Hold Time, All Synchronous Inputs after CLK ↑			0	0	0	ns
C_{IN}	Maximum Input Capacitance			5			pF
C_{PD}	Power Dissipation Capacitance*			80			pF

*C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
†For AC switching test circuits and timing waveforms see section 2.

Zytrex

ZX54AHCT ZX74AHCT 161 ZX54AHCT ZX74AHCT 163

T-45-23-05

AC Electrical Characteristics (Input t_r, $t_f \leq 2$ ns), AHCT163

Symbol	Parameter		Conditions†	$T_A = 25°C$ $V_{CC} = 5.0V$	74AHCT $T_A = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$	54AHCT $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits		
f_{max}	Maximum Operating Frequency		$C_L = 50$ pF	50	30	25	MHz
t_{PLH}	Maximum Propagation Delay, CLK to RCO			15	25	30	ns
t_{PHL}				15	25	30	
t_{PLH}	Maximum Propagation Delay, CLK to any Q			10	16	20	ns
t_{PHL}				10	16	20	
t_{PLH}	Maximum Propagation Delay, ENT to RCO			9	15	18	ns
t_{PHL}				9	15	18	
t_w	Minimum Pulse Width, CLK High or Low			10	17	20	ns
t_{su}	Minimum Setup Time before CLK ↑	A, B, C, D		10	15	20	ns
		$\overline{LOAD}$		10	15	20	
		ENP, ENT		15	25	30	
		$\overline{CLR}$ Inactive (High)		10	15	20	
		$\overline{CLR}$ Low		6	10	10	
t_h	Minimum Hold Time, All Synchronous Inputs after CLK ↑			0	0	0	ns
C_{IN}	Maximum Input Capacitance			5			pF
C_{PD}	Power Dissipation Capacitance*			80			pF

*C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
†For AC switching test circuits and timing waveforms see section 2.

4