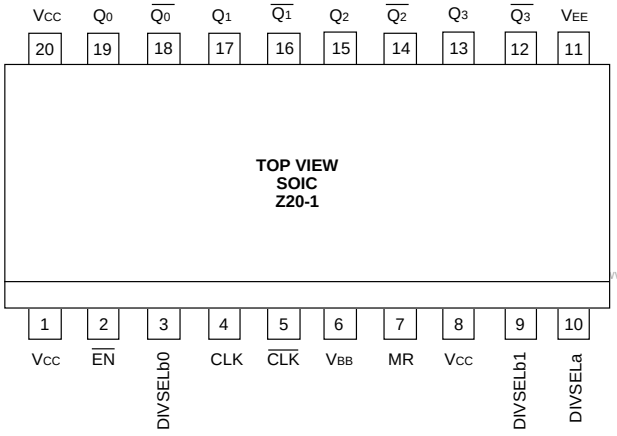
÷2/4, ÷4/5/6 CLOCK GENERATION CHIP

ClockWorks™
SY100S839V
FINAL

FEATURES

- **3.3V and 5V power supply option**
- **50ps output-to-output skew**
- **50% duty cycle outputs**
- **Synchronous enable/disable**
- **Master Reset for synchronization**
- **Internal 75KΩ input pull-down resistors**
- **Available in 20-pin SOIC package**

PIN CONFIGURATION/BLOCK DIAGRAM



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TRUTH TABLE

CLK	/EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

NOTE:
Z = LOW-to-HIGH transition
ZZ = HIGH-to-LOW transition

DIVSELa	Q_0, Q_1 OUTPUTS
0	Divide by 2
1	Divide by 4

DIVSELb1	DIVSELb0	Q_2, Q_3 OUTPUTS
0	0	Divide by 4
0	1	Divide by 6
1	0	Divide by 5
1	1	Divide by 5

DESCRIPTION

The SY100S839V is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL/LVECL or, if positive power supplies are used, PECL/LVPECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the /CLK input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the S839V under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The common enable (/EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one S839V, the MR pin need not be exercised as the internal divider designs ensures synchronization between the ÷2/4, and the ÷4/5/6 outputs of a single device.

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
/EN	Synchronous Enable
MR	Master Reset
V_{BB}	Reference Output
Q_0, Q_1	Differential ÷2/4 Outputs
Q_2, Q_3	Differential ÷4/5/6 Outputs
DIVSEL	Frequency Select Input

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DC ELECTRICAL CHARACTERISTICS[1]

V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	—	50	95	—	50	95	—	50	95	—	54	95	mA
V_{BB}	Output Reference Voltage	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	V
I_{IH}	Input High Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
V_{OH}	Output HIGH Voltage[2]	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage[2]	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{OHA}	Output HIGH Voltage[3]	–1095	—	—	–1035	—	—	–1035	—	—	–1035	—	—	mV
V_{OLA}	Output LOW Voltage[3]	—	—	–1555	—	—	–1610	—	—	–1610	—	—	–1610	mV
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	–1165	—	–880	–1165	—	–880	mV
V_{IL}	Input LOW Voltage	–1810	—	–1475	–1810	—	–1475	–1810	—	–1475	–1810	—	–1475	mV
I_{IL}	Input LOW Current[4]	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	—	µA

NOTE:

1. Parametric values specified at: -3.0V to -3.8V or -4.2V to -5.5V.
2. V_{IN} = V_{IH}(Max) or V_{IL}(Min): Loading with 50Ω to –2.0V.
3. V_{IN} = V_{IH}(Min) or V_{IL}(Max): Loading with 50Ω to –2.0V.
4. V_{IN} = V_{IL}(Min).

AC ELECTRICAL CHARACTERISTICS[1]

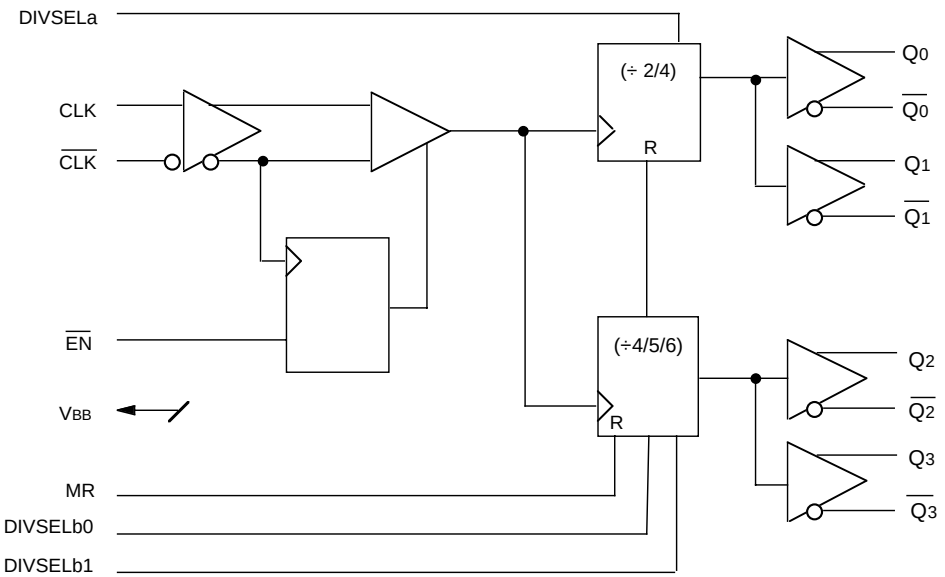
V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = GND

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Maximum Toggle Frequency	1000	—	—	1000	—	—	1000	—	—	1000	—	—	MHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK → Output (Diff.) CLK → Output (S.E.) MR → Output	 725 675 600	 — — —	 925 975 900	 725 675 600	 — — —	 925 975 900	 725 675 610	 — — —	 925 975 910	 725 675 630	 — — —	 925 975 930	ps
t_{skew}	Within-Device Skew[2] Q_0 — Q_3 Part-to-Part Q_0 — Q_3 (Diff.)	— —	— —	50 200	— —	— —	50 200	— —	— —	50 200	— —	— —	50 200	ps
t_S	Set-up Time /EN → /CLK DIVSEL → CLK	250 400	— —	— —	250 400	— —	— —	250 400	— —	— —	250 400	— —	— —	ps
t_H	Hold Time /CLK → /EN CLK → DIVSEL	100 150	— —	— —	100 150	— —	— —	100 150	— —	— —	100 150	— —	— —	ps
V_{PP}	Minimum Input Swing[3] CLK	250	—	—	250	—	—	250	—	—	250	—	—	mV
V_{CMR}	Common Mode Range[4], [5]	-1.6	—	-0.4	-1.7	—	-0.4	-1.7	—	-0.4	-1.7	—	-0.4	V
t_{RR}	Reset Recovery Time	—	—	100	—	—	100	—	—	100	—	—	100	ps
t_{PW}	Minimum Pulse Width CLK MR	500 700	— —	— —	500 700	— —	— —	500 700	— —	— —	500 700	— —	— —	ps
tr tf	Output Rise/Fall Times Q (20% —80%)	280	—	550	280	—	550	280	—	550	280	—	550	ps

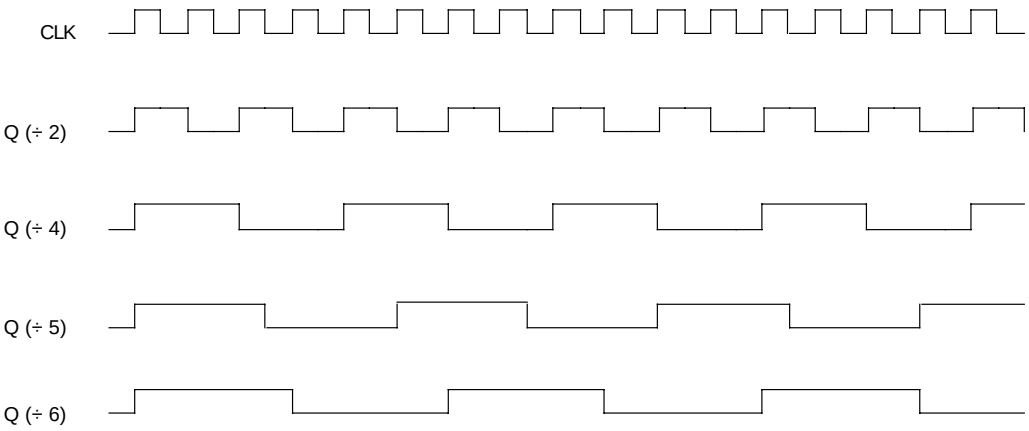
NOTES:

1. Parametric values specified at: -3.0V to -3.8V or -4.2V to -5.5V.
2. Skew is measured between outputs under identical transitions.
3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V – IV_{CMR} (min)I.
5. Duty Cycle: (Min. 48%; Max. 52%) } over temp.

LOGIC DIAGRAM



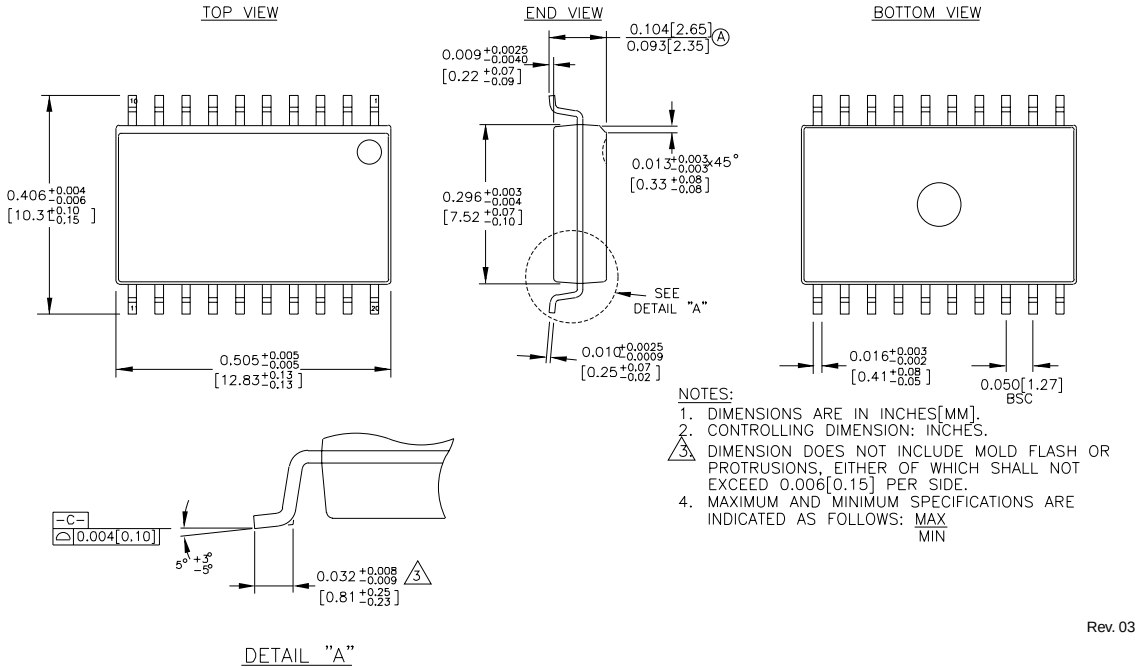
TIMING DIAGRAMS



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S839VZC	Z20-1	Commercial
SY100S839VZCTR	Z20-1	Commercial

20 LEAD SOIC .300" WIDE (Z20-1)



Rev. 03

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