M5M27C101K,-12,-15,-2/ M5M27C101JK -12,-15,-2

1048576-BIT(131072-WORD BY 8-BIT)
CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27C101K, JK is a high-speed 1048576-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C101K, JK is fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and is available in DIP/CLCC with a transparent lid.

FEATURES

- 131072 word x 8 bit organization
- Access time M5M27C101K-12, JK-12 . . 120ns (max.)
  - M5M27C101K-15, JK-15 . . 150ns (max.)
  - M5M27C101K-2, JK-2 . . . . 200ns (max.)
  - M5M27C101K . . . . 250ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active . . . . . 50mA (max.)
  - Stand by . . . . . 1mA (max.)
- Single 5V power supply
- Programming voltage 12.5V
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 32 pin DIP
- Byte programming algorithm
- Page programming algorithm

APPLICATION

Microcomputer systems and peripheral equipment

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{16}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.
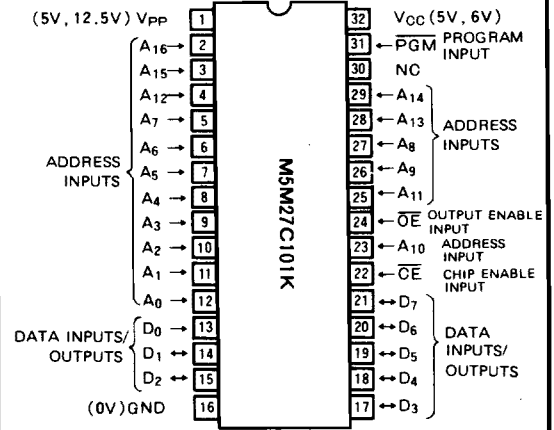
Programming
(Byte programming algorithm)

The M5M27C101K, JK enters the byte programming mode when 12.5V is supplied to the V_{PP} power supply input, $\overline{CE}$ is at low level and $\overline{OE}$ is at high level. A location is designated by address signals ($A_0 \sim A_{16}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). In this state, byte programming is completed when $\overline{PGM}$ is at low level.
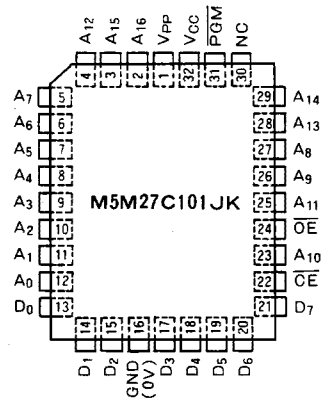
(Page programming algorithm)

Page programming feature of the M5M27C101K, JK allows 4 bytes of data to be simultaneously programmed. The destination addresses for a page programming operation must reside on the same page; that is, A_2 through A_{16} must not change. At first, the M5M27C101K, JK enters the page data latch mode when $V_{PP} = 12.5V$, $\overline{CE} = $ "H", $\overline{OE} = $ "L" and $\overline{PGM} = $ "H". The four locations in same page are designated by address signals (A_0, A_1 change) and the data to be programmed must be applied to each location at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). In this state, the data (4-bytes) latch is completed. Then the M5M27C101K, JK enters the page programming mode when $\overline{OE} = $ "H". In this state, page (4-bytes) programming is completed when PGM = "L".

PIN CONFIGURATION (TOP VIEW)

Outline 32K4 (DIP: K)

Outline 32K0 (CLCC: JK)

NC: NO CONNECTION

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Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately 15WS/cm^2. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

BLOCK DIAGRAM
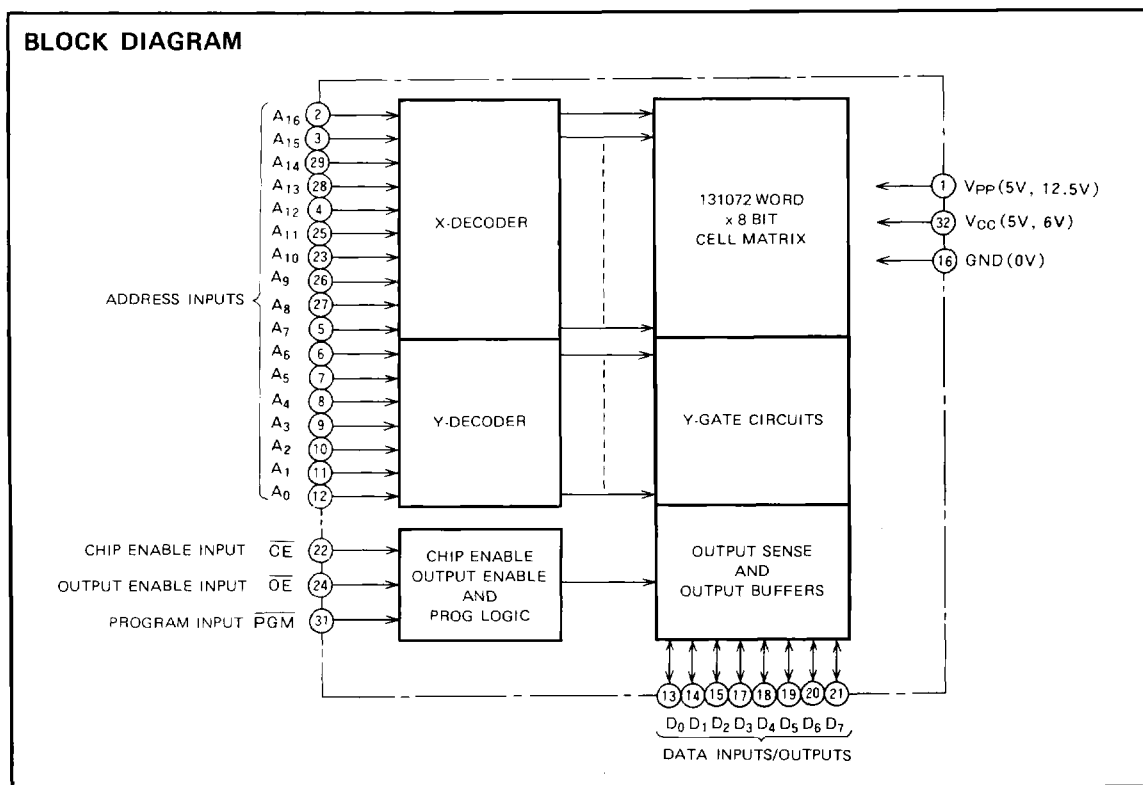
MODE SELECTION

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Data I/O (13~15, 17~21)
Read	V_{IL}	V_{IL}	X*	5 V	5 V	Data out
Output disable	V_{IL}	V_{IH}	X*	5 V	5 V	Floating
Standby (Power down)	V_{IH}	X*	X*	5 V	5 V	Floating
Byte program	V_{IL}	V_{IH}	V_{IL}	12.5 V	6 V	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6 V	Data out
Page data latch	V_{IH}	V_{IL}	V_{IH}	12.5 V	6 V	Data in
Page program	V_{IH}	V_{IH}	V_{IL}	12.5 V	6 V	Floating
Program inhibit	V_{IL}	V_{IL}	V_{IL}	12.5 V	6 V	Floating
	V_{IL}	V_{IH}	V_{IH}	12.5 V	6 V	
	V_{IH}	V_{IL}	V_{IL}	12.5 V	6 V	
	V_{IH}	V_{IH}	V_{IH}	12.5 V	6 V	

** X can be either V_{IL} or V_{IH}

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Conditions	Ratings	Unit
V_{I1}	All input or output voltage except $V_{PP} \cdot A_9$		$-0.6 \sim 7$	V
V_{I2}	V_{PP} supply voltage	With respect to Ground	$-0.6 \sim 14.0$	V
V_{I3}	A_9 supply voltage		$-0.6 \sim 13.5$	V
T_{opr}	Operating temperature		$-10 \sim 80$	°C
T_{stg}	Storage temperature		$-65 \sim 125$	°C

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of
the device at those or at any other conditions above those indicated in the operational sections of this specification is not
implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

READ OPERATION
DC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

| Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
I_{Li}	Input load current	$V_{IN} = 0 \sim V_{CC}$			10	μA
I_{LO}	Output leakage current	$V_{OUT} = 0 \sim V_{CC}$			10	μA
I_{PP1}	V_{PP} current read	$V_{PP} = 5.5V$		1	100	μA
I_{SB1}	V_{CC} current standby	$\overline{CE} = V_{IH}$			1	mA
I_{SB2}		$\overline{CE} = V_{CC}$		1	100	μA
I_{CC1}	V_{CC} current Active	$\overline{CE} = \overline{OE} = V_{IL}$			50	mA
I_{CC2}		$f = 6.7MHz$, $I_{OUT} = 0mA$			50	mA
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V

Note 2: Typical values are at $T_a = 25°C$ and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	M5M27C101K-12 M5M27C101JK-12 Min	Max	M5M27C101K-15 M5M27C101JK-15 Min	Max	M5M27C101K-2 M5M27C101JK-2 Min	Max	M5M27C101K Min	Max	Unit
$t_{a(AD)}$	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
$t_{a(CE)}$	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
$t_{a(OE)}$	Output enable to output delay	$\overline{CE} = V_{IL}$		60		60		75		100	ns
t_{DF}	Output enable high to output float	$\overline{CE} = V_{IL}$	0	50	0	50	0	60	0	60	ns
t_{OH}	Output hold from $\overline{CE}$, $\overline{OE}$ or Addresses		0		0		0		0		ns

Note 3: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.
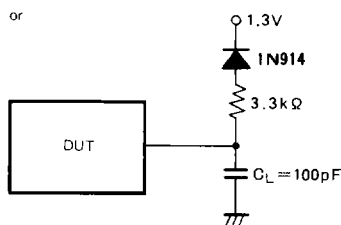
AC WAVEFORMS
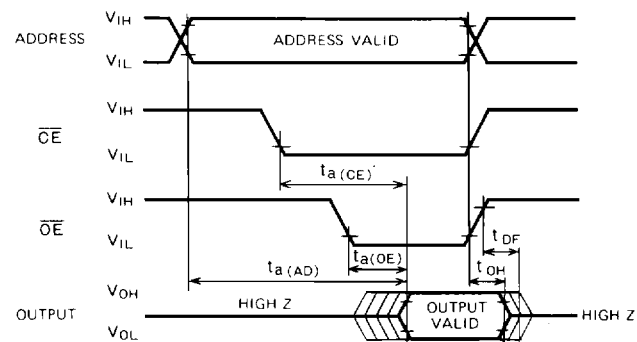
Test conditions for A.C. characteristics
Input voltage: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall times $\leq 20ns$
Reference voltage at timing measurement: Input, Output
"L" = 0.8V, "H" = 2V.

Output load: 1TTL gate + C_L (100pF)

or

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CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	$Ta=25°C$, $f=1MHz$, $V_I=V_O=0V$			10	pF
C_{OUT}	Output capacitance				15	pF

PROGRAM OPERATION

BYTE PROGRAMMING ALGORITHM

First set $V_{CC} = 6V$, $V_{PP} = 12.5V$ and then set an address to first address to be programmed. After applying 0.2 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.2 ms program pulse. The programmer continues 0.2 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 0.2 ms pulse applied to that address in register X. And then applied a program pulse X times of 0.2 ms width as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

DC ELECTRICAL CHARACTERISTICS ($Ta=25±5°C$, $V_{CC}=6V±0.25V$, $V_{PP}=12.5V±0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=0 \sim V_{CC}$			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC}	V_{CC} supply current				50	mA
I_{PP}	V_{PP} supply current	$\overline{CE}=\overline{PGM}=V_{IL}$			50	mA

## AC ELECTRICAL CHARACTERISTICS ($Ta=25±5°C$, $V_{CC}=6V±0.25V$, $V_{PP}=12.5V±0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

Note 4 V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

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AC WAVEFORMS
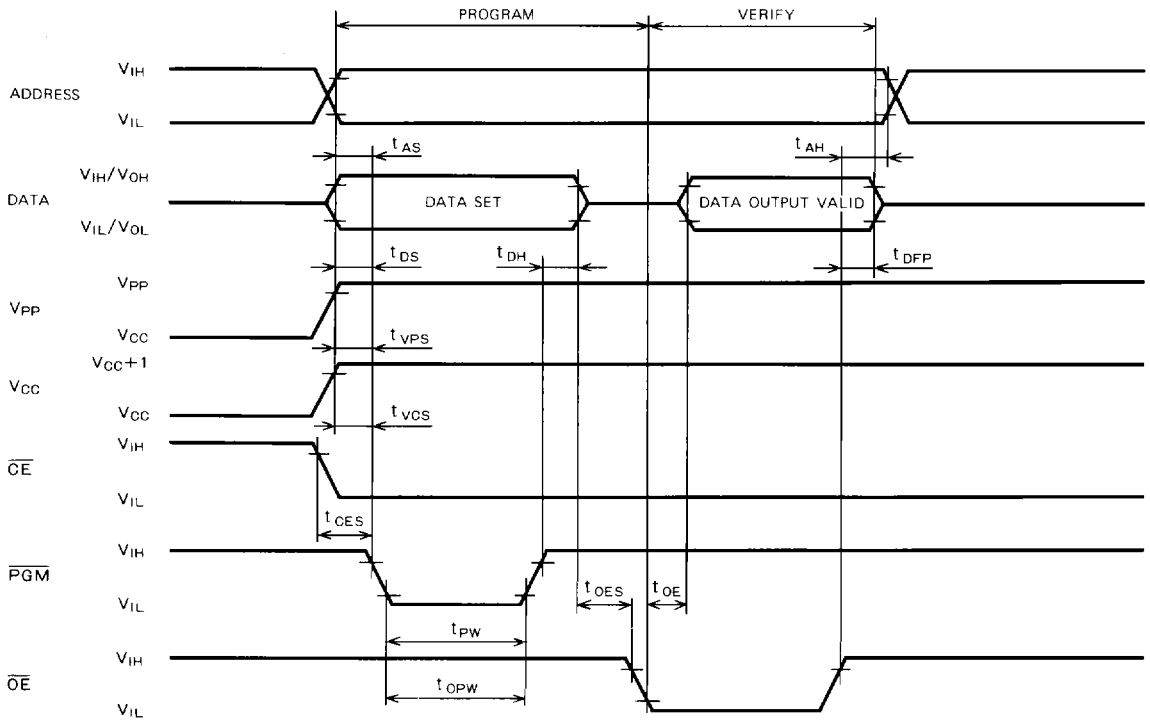
BYTE PROGRAMMING ALGORITHM FLOW CHART

Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: $\leq$ 20ns
Reference voltage at timing measurement: Input, Output
"L" = 0.8V, "H" = 2V.

START

ADDR = FIRST LOCATION

V_{CC} = 6.0V
V_{PP} = 12.5V

X = 0

PROGRAM ONE PULSE OF 0.2ms

X = X + 1

X = 25 ? — YES

NO

VERIFY BYTE — FAIL

VERIFY BYTE — FAIL → DEVICE FAILED

PASS

PROGRAM PULSE OF 0.2Xms DURATION

INCREMENT ADDR ← NO — LAST ADDR?

YES

V_{CC} = V_{PP} = *5.0V

VERIFY ALL BYTE — FAIL → DEVICE FAILED

PASS

DEVICE PASSED
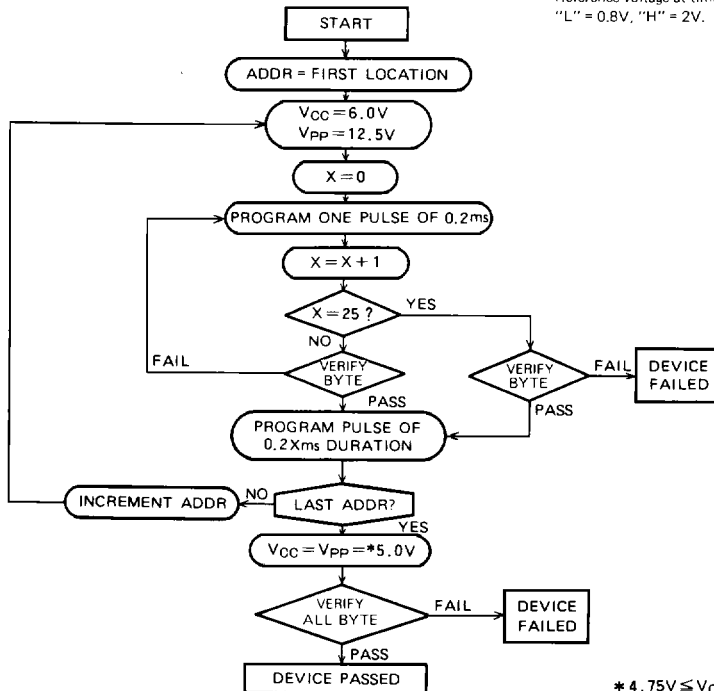
*4.75V $\leq V_{CC}$ = $V_{PP} \leq$ 5.25V

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PAGE PROGRAMMING ALGORITHM

First set $V_{CC} = 6V$, $V_{PP} = 12.5V$ and then set an address to first page address to be programmed. After data of 4 bytes are latched, these latch data are programmed simultaneously by applying 0.2 ms program pulse. Then a verify is performed. If each output data is not verified correctly, apply one more 0.2 ms program pulse. The programmer continues 0.2 ms pulse-then-verify routines until each output data is verified correctly or twenty five of these pulse-then-verify routines have been completed.

The programmer also maintains its total number of 0.2 ms pulse applied to that page addresses in register X. And then applied a program pulse X times of 0.2 ms width as an overprogram pulse. When the programming procedure above is finished, step to the next page address and repeat this procedure till last page address to be programmed. When the entire page addresses have been programmed completely, all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

DC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	$V_{IN}=0\sim V_{CC}$			10	μA
V_{OL}	Output low voltage	$I_{OL}=2.1mA$			0.45	V
V_{OH}	Output high voltage	$I_{OH}=-400\mu A$	2.4			V
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC}	V_{CC} supply current				50	mA
I_{PP}	V_{PP} supply current	$\overline{PGM}=V_{IL}$			100	mA

AC ELECTRICAL CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.3V$, unless otherwise noted)

| Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{AHL}			2			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	$\overline{OE}$ to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns
t_{LW}	Data latch time		1			μs
t_{PGMS}	$\overline{PGM}$ setup time		2			μs
t_{CEH}	$\overline{CE}$ hold time		2			μs
t_{OEH}	$\overline{OE}$ hold time		2			μs

Note 5: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

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AC WAVEFORMS
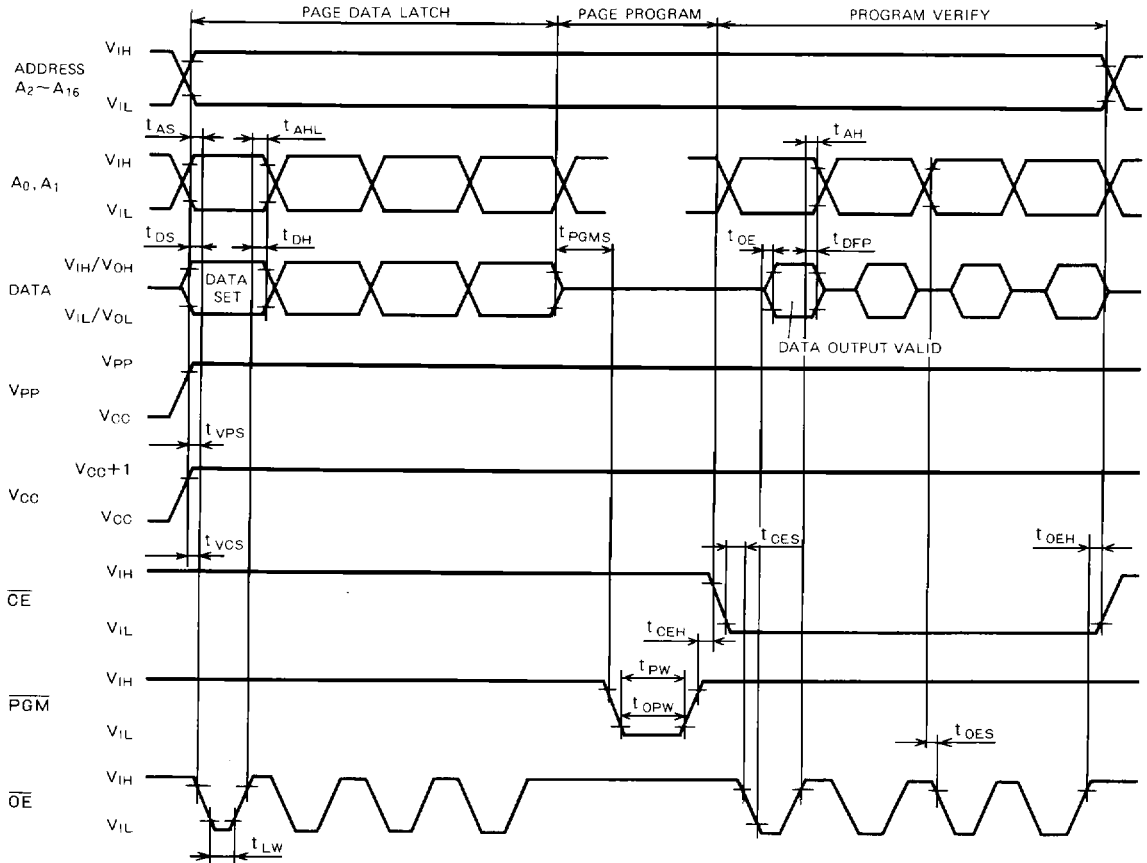
Test condition for A.C characteristics
Input voltage: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall time: (10% ~ 90%): ≤ 20ns
Reference voltage at timing measurement: Input, Output "L" = 0.8V, "H" = 2V.

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PAGE PROGRAMMING ALGORITHM
FLOW CHART
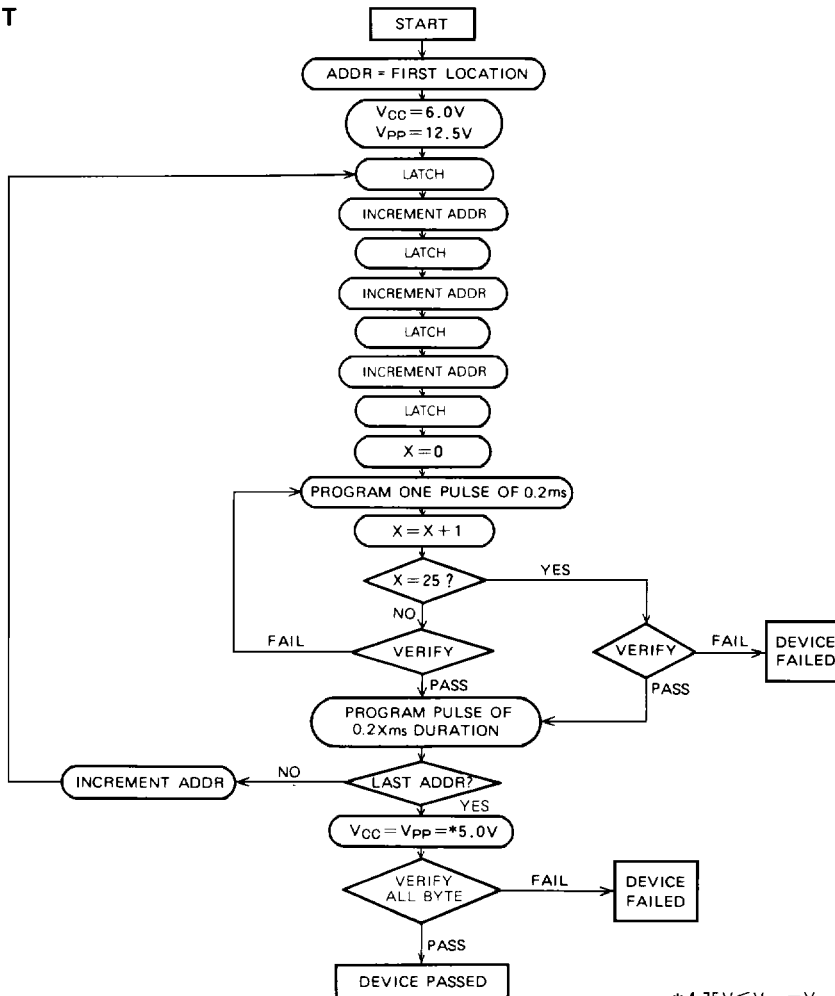
* $4.75V \leq V_{CC} = V_{PP} \leq 5.25V$

DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5M27C101K, JK DEVICE IDENTIFIER CODE

Code \ Pins	A_0 (12)	D_7 (21)	D_6 (20)	D_5 (19)	D_4 (18)	D_3 (17)	D_2 (15)	D_1 (14)	D_0 (13)	Hex Data
Manufacturer code	V_{IL}	0	0	0	1	1	1	0	0	1C
Device code	V_{IH}	1	0	0	0	0	0	1	1	83

Note 6: $A_9 = 12.0 \pm 0.5V$
$A_1 \sim A_8$, $A_{10} \sim A_{16}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$
$V_{CC} = V_{PP} = 5V \pm 5\%$

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