



V2267

LINEAR INTEGRATED CIRCUIT

DUAL VIDEO 6dB AMPLIFIER WITH 75Ω DRIVER

DESCRIPTION

The UTC V2267 is a dual video 6dB amplifier with 75Ω drivers for SVHS VCRs, HI-BAND VCRs, etc. Its operating supply voltage is 4.85 to 9V and bandwidth is 7MHz. Each channel has clamp function that fixes DC level of video signal and 75Ω drivers to be connected to TV monitors directly. Further more it has SAG corrective circuits that prevent the generation of SAG with a small capacitance.

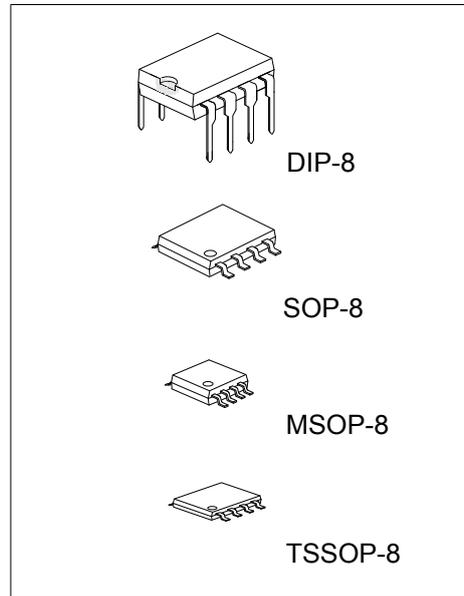
It is for VCR, Video Camera, TV, Video Disc Player.

FEATURES

- * Dual Channel
- * Wide Operating Voltage (4.85V ~ 9.0V)
- * Low Operating Current 14.0mA (Dual)
- * Wide Frequency Range (7MHz)
- * Internal Clamp Function
- * Internal Driver Circuit For 75Ω Load
- * SAG Corrective Function
- * Bipolar Technology

ORDERING INFORMATION

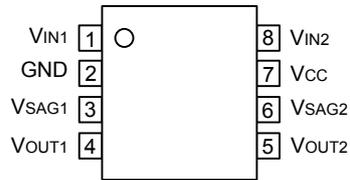
Ordering Number			Package	Packing
Normal	Lead Free Plating	Halogen Free		
V2267-D08-T	V2267L-D08-T	V2267G-D08-T	DIP-8	Tube
V2267-S08-R	V2267L-S08-R	V2267G-S08-R	SOP-8	Tape Reel
V2267-SM1-R	V2267L-SM1-R	V2267G-SM1-R	MSOP-8	Tape Reel
V2267-P08-R	V2267L-P08-R	V2267G-P08-R	TSSOP-8	Tape Reel



Lead-free: V2267L
Halogen-free: V2267G

<p>V2267L-D08-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) D08: DIP-8, SM1: MSOP-8, S08: SOP-8, P08: TSSOP-8 (3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn</p>
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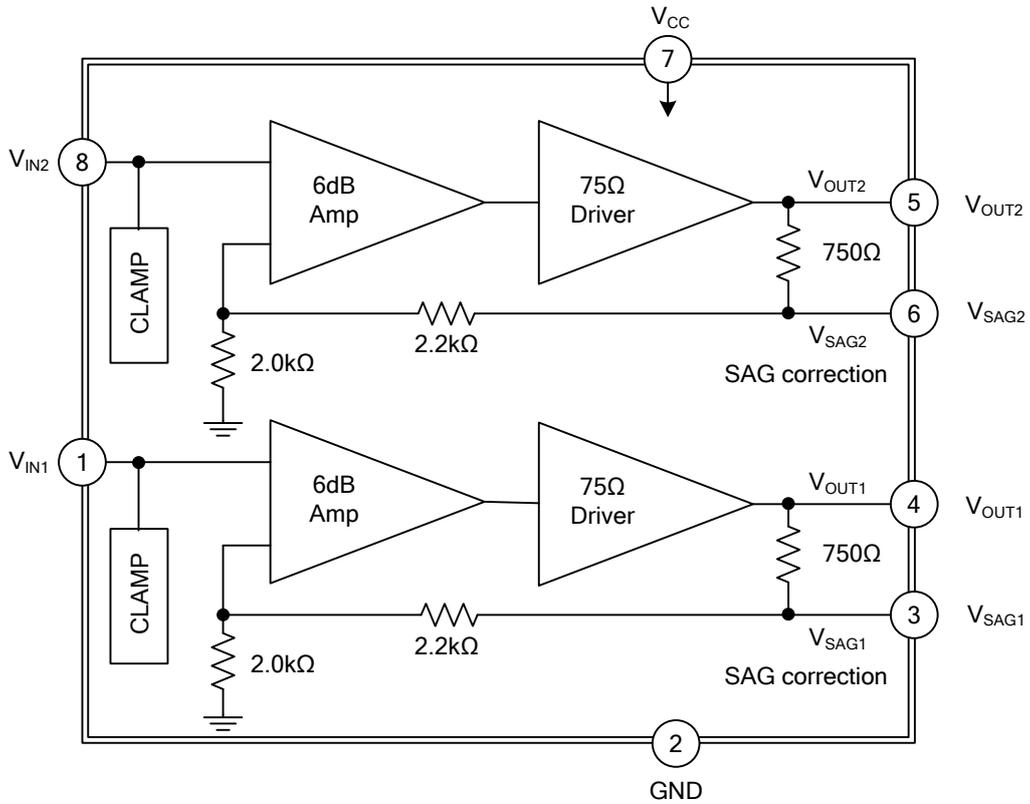
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	PIN DESCRIPTION
1	V _{IN1}	I	Input terminal of 1Vp-p composite signal or Y signal. Clamp level is 1.9V
2	GND		Ground
3	V _{SAG1}	O	Channel 1 SAG correction output
4	V _{OUT1}	O	Output terminal that can drive 75Ω line. Channel 1 output
5	V _{OUT2}	O	Output terminal that can drive 75Ω line. Channel 2 output
6	V _{SAG2}	O	Channel 2 SAG correction output
7	V _{CC}		Supply voltage
8	V _{IN2}	I	Input terminal of 1Vp-p composite signal or Y signal. Clamp level is 1.9V

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	10	V
Power Dissipation	DIP-8	P_D	500	mW
	SOP-8		350	mW
	MSOP-8		300	mW
	TSSOP-8		250	mW
Operating Temperature		T_{OPR}	-40 ~ +85	°C
Storage Temperature		T_{STG}	-40 ~ +125	°C

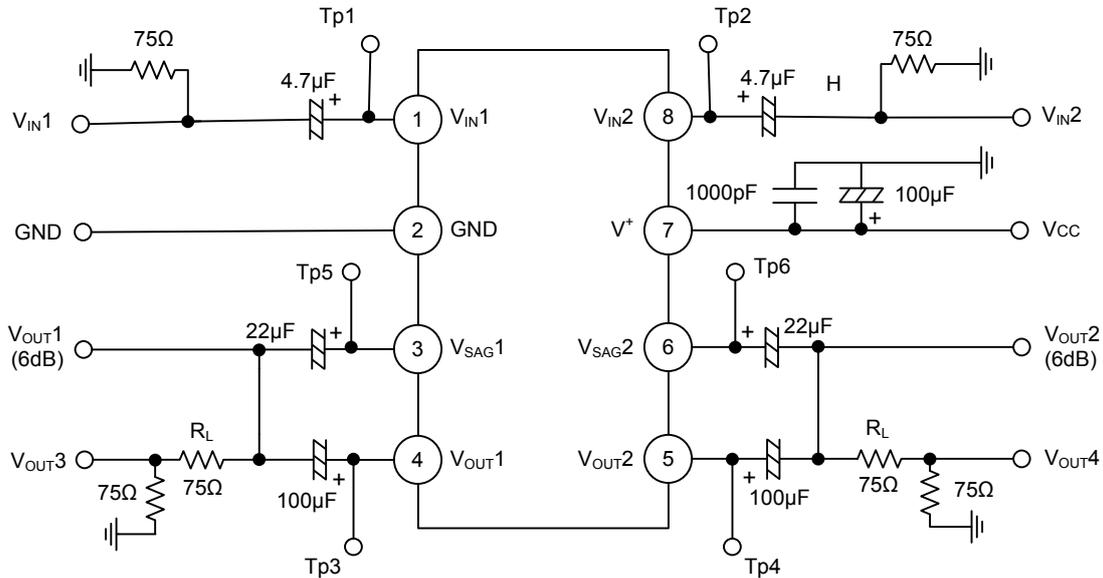
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Clamp Voltage	V_{CL}	Measuring at TP1(TP2) No signal	1.79	1.91	2.03	V
Operating Current	I_{CC}	No signal		14.0	18.2	mA
Voltage Gain	G_V	V_{OUT1}/V_{IN1} , V_{OUT2}/V_{IN2} at $V_{IN1}(V_{IN2})=1MHz$, 1Vp-p, Sinewave	5.7	6.2	6.7	dB
Frequency Characteristic	G_F	$V_{IN}=1Vp-p$, Sinewave, 7MHz/1MHz			± 1.0	dB
Crosstalk	CT	V_{OUT2}/V_{OUT1} at $V_{IN1}=4.43MHz$, 1Vp-p, $V_{IN2}=gnd$, Sinewave V_{OUT1}/V_{OUT2} at $V_{IN2}=4.43MHz$, 1Vp-p, $V_{IN1}=gnd$, Sinewave		-70		dB
Gain Offset	G_{CH}	$V_{IN}=1MHz$, 1Vp-p, $G_{V1} = V_{OUT1}/V_{IN1}$, $G_{V2} = V_{OUT2}/V_{IN2}$, $G_{CH} = G_{V1}-G_{V2}$			± 0.5	dB
SAG Terminal Gain	G_{SAG}		35	45		dB
Differential Gain	G_{DIFF}	$V_{IN1}=1Vp-p$, Staircase Measuring V_{OUT3} at V_{IN1} = Staircase Signal		1.0	3.0	%
Differential Phase	DP	$V_{IN1}=1Vp-p$, Staircase Measuring V_{OUT3} at V_{IN1} = Staircase Signal		1.0	3.0	deg

■ TEST CIRCUIT



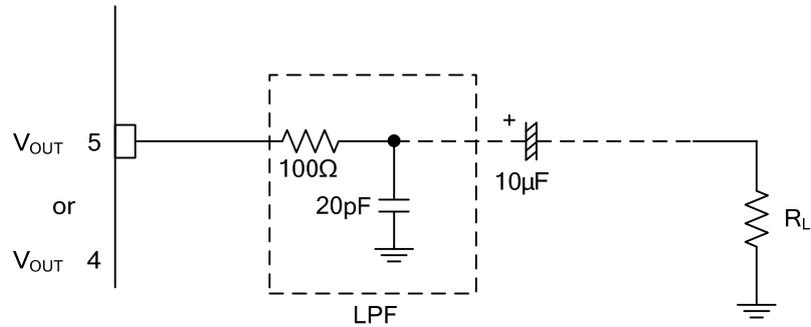
■ TEST METHODES

PARAMETER	SYMBOL	TEST METHODES
Input Clamp Voltage	V_{CL}	No signal Measuring at TP1(TP2)
Operating Current	I_{CC}	No signal 7PIN Sink Current
Voltage Gain	G_V	V_{OUT1}/V_{IN1} , V_{OUT2}/V_{IN2} at $V_{IN1}(V_{IN2}) = 1\text{MHz}$, 1Vp-p, Sinewave
Frequency Characteristic	G_F	G_{V1M} ; Voltage Gain at $V_{IN1}(V_{IN2}) = 1\text{MHz}$, 1Vp-p G_{V10M} ; Voltage Gain at $V_{IN1}(V_{IN2}) = 10\text{MHz}$, 1Vp-p $G_F = G_{V10M} - G_{V1M}$
Crosstalk	CT	V_{OUT2}/V_{IN1} at $V_{IN1} = 4.43\text{MHz}$, 1Vp-p, Sinewave, $V_{IN2} = \text{gnd}$ V_{OUT1}/V_{IN2} at $V_{IN2} = 4.43\text{MHz}$, 1Vp-p, Sinewave, $V_{IN1} = \text{gnd}$
Gain Offset	G_{CH}	$V_{IN} = 1\text{MHz}$, 1Vp-p, $G_{V1} = V_{OUT1}/V_{IN1}$, $G_{V2} = V_{OUT2}/V_{IN2}$ $G_{CH} = G_{V1} - G_{V2}$
Differential Gain	G_{DIFF}	$V_{IN1} = 1\text{Vp-p}$, Staircase Measuring V_{OUT3} at $V_{IN1} = \text{Staircase Signal}$
Differential Phase	DP	$V_{IN1} = 1\text{Vp-p}$, Staircase Measuring V_{OUT3} at $V_{IN1} = \text{Staircase Signal}$

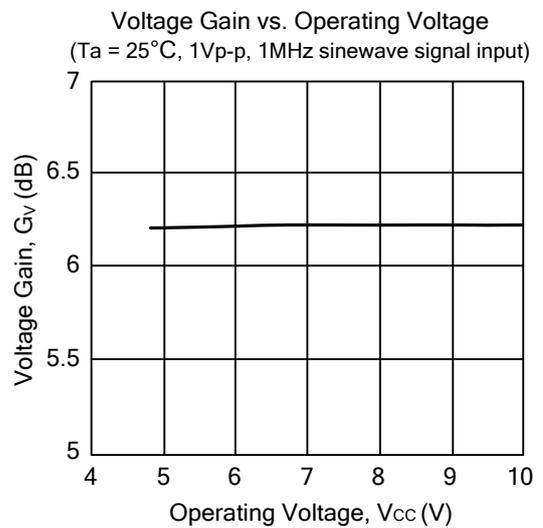
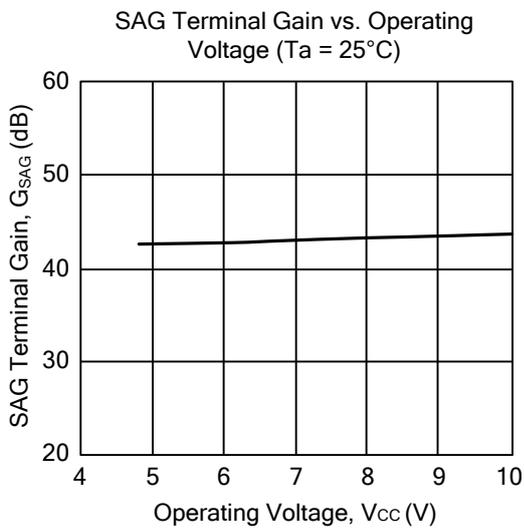
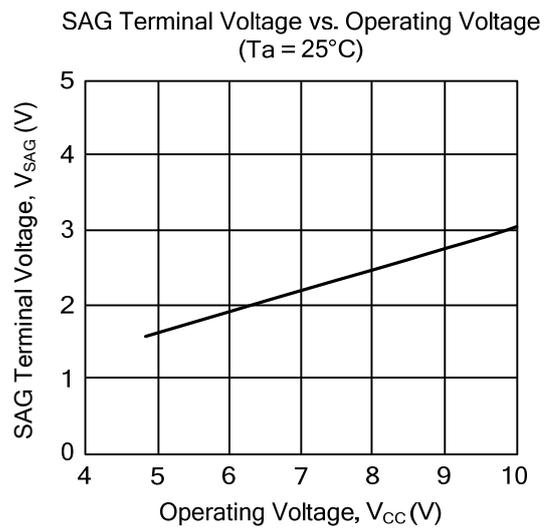
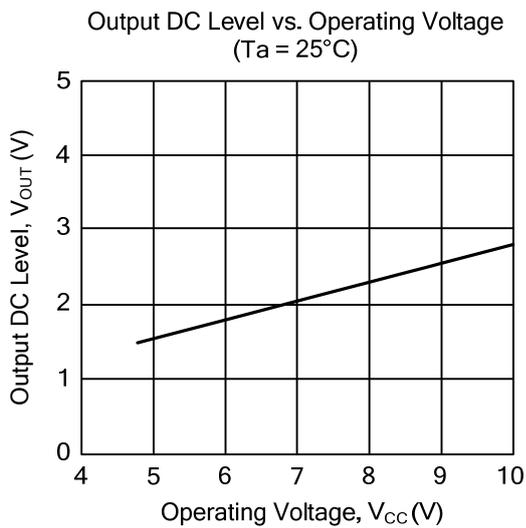
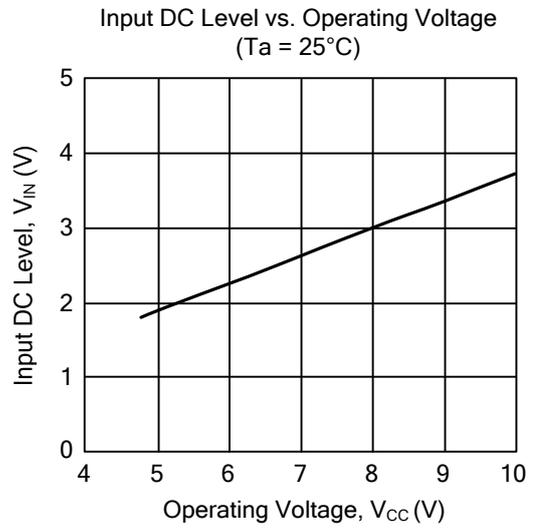
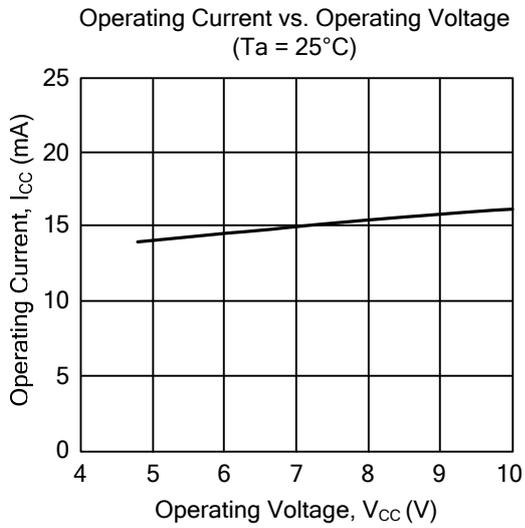
■ APPLICATION**Oscillation Prevention**

It is much effective to insert LPF (Cutoff Frequency 70MHz) under light loading conditions ($R_L \gg 1k\Omega$)

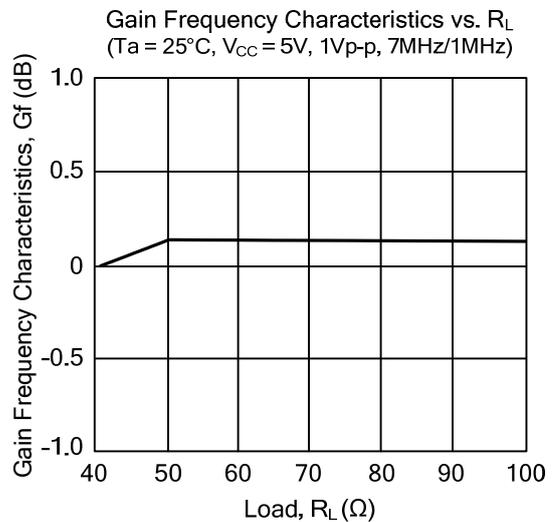
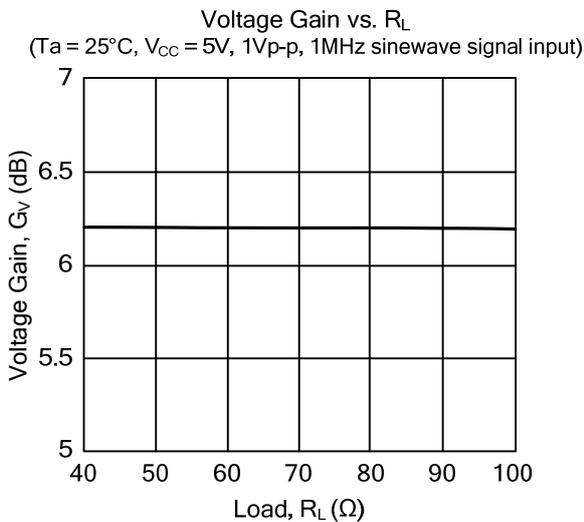
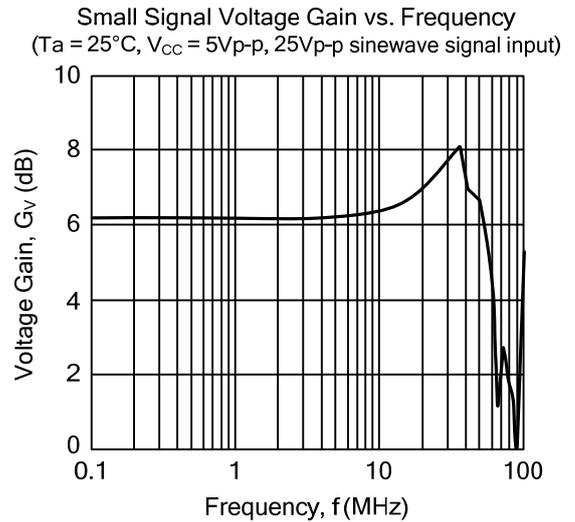
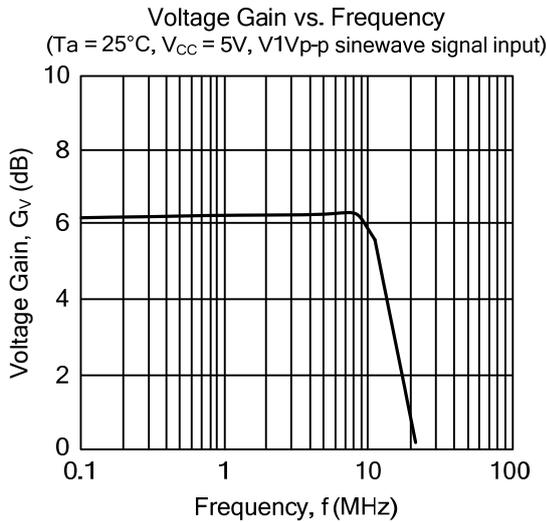
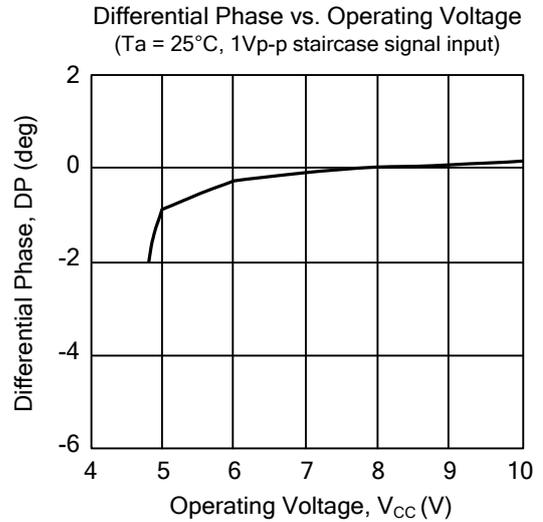
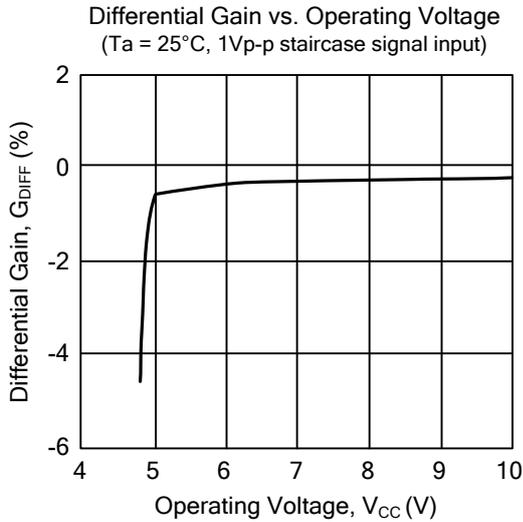
This IC requires $1M\Omega$ resistance between INPUT and GND pin for clamp type input since the minute current causes an unstable pin voltage.



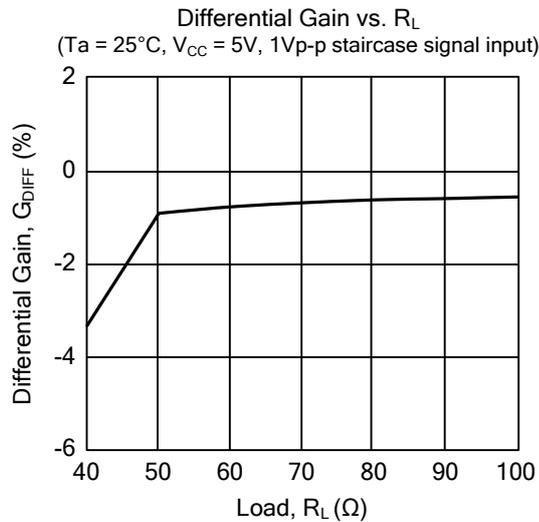
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



■ TYPICAL CHARACTERISTICS(Cont.)



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