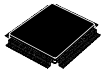
STM32F103xF
STM32F103xG

XL-density performance line ARM-based 32-bit MCU with 768 KB to 1 MB Flash, USB, CAN, 17 timers, 3 ADCs, 13 communication interfaces

Data brief

Features

- Core: ARM 32-bit Cortex™-M3 CPU with MPU
  - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 768 Kbytes to 1 Mbyte of Flash memory
  - 96 Kbytes of SRAM
  - Flexible static memory controller with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC with calibration
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- 3 × 12-bit, 1 µs A/D converters (up to 21 channels)
  - Conversion range: 0 to 3.6 V
  - Triple-sample and hold capability
  - Temperature sensor
- 2 × 12-bit D/A converters
- DMA: 12-channel DMA controller
  - Supported peripherals: timers, ADCs, DAC, SDIO, I^2Ss, SPIs, I^2Cs and USARTs
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M3 Embedded Trace Macrocell™



LQFP64 10 × 10 mm,
LQFP100 14 × 14 mm,
LQFP144 20 × 20 mm

LFBGA144 10 × 10 mm

- Up to 112 fast I/O ports
  - 51/80/112 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant
- Up to 17 timers
  - Up to ten 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 × 16-bit motor control PWM timers with dead-time generation and emergency stop
  - 2 × watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
  - 2 × 16-bit basic timers to drive the DAC
- Up to 13 communication interfaces
  - Up to 2 × I^2C interfaces (SMBus/PMBus)
  - Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 3 SPIs (18 Mbit/s), 2 with I^2S interface multiplexed
  - CAN interface (2.0B Active)
  - USB 2.0 full speed interface
  - SDIO interface
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

Table 1. Device summary

Reference	Part number
STM32F103xF	STM32F103RF STM32F103VF STM32F103ZF
STM32F103xG	STM32F103RG STM32F103VG STM32F103ZG

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xF and STM32F103xG XL-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The XL-density STM32F103xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the *www.arm.com* website at the following address: *http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/*.

2 Description

The STM32F103xF and STM32F103xG performance line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 1 Mbyte and SRAM up to 96 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer three 12-bit ADCs, ten general-purpose 16-bit timers plus two PWM timers, as well as standard and advanced communication interfaces: up to two I^2Cs, three SPIs, two I2Ss, one SDIO, five USARTs, an USB and a CAN.

The STM32F103xx XL-density performance line family operates in the –40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx XL-density performance line family offers devices in four different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx high-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications, PLC, inverters, printers, and scanners
- Alarm systems, power meters and video intercom

Figure 1 shows the general block diagram of the device family.

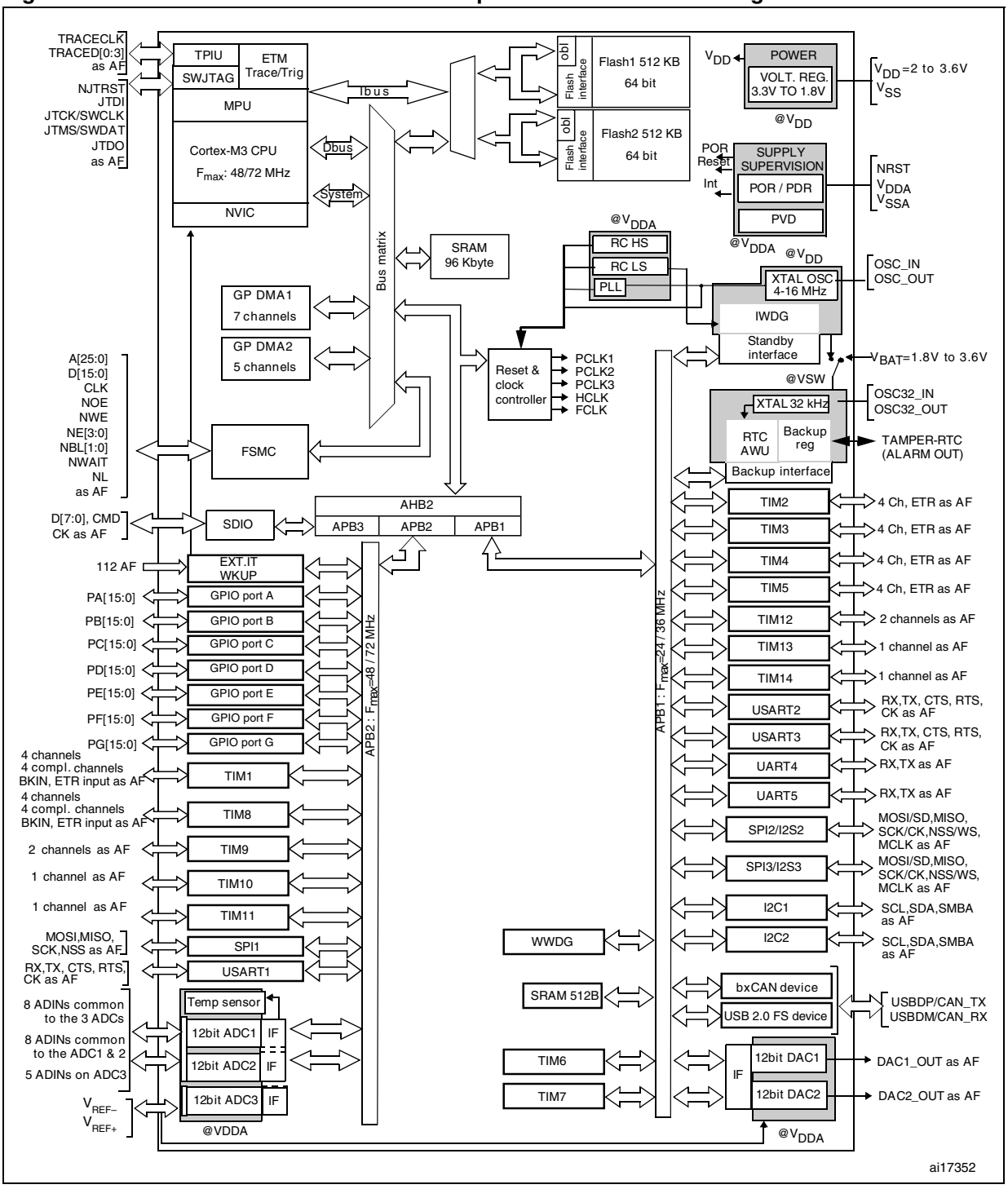
2.1 Device overview

Table 2. STM32F103xF and STM32F103xG features and peripheral counts

Peripherals		STM32F103Rx		STM32F103Vx		STM32F103Zx	
Flash memory		768 KB	1 MB	768 KB	1 MB	768 KB	1 MB
SRAM in Kbytes		96		96		96	
FSMC		No		Yes(1)		Yes	
Timers	General-purpose	10					
	Advanced-control	2					
	Basic	2					
Comm	SPI(I^2S)(2)	3(2)					
	I^2C	2					
	USART	5					
	USB	1					
	CAN	1					
	SDIO	1					
GPIOs		51		80		112	
12-bit ADC Number of channels		3 16		3 16		3 21	
12-bit DAC Number of channels		2 2					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C Junction temperature: –40 to + 125 °C					
Package		LQFP64		LQFP100		LQFP144, BGA144	

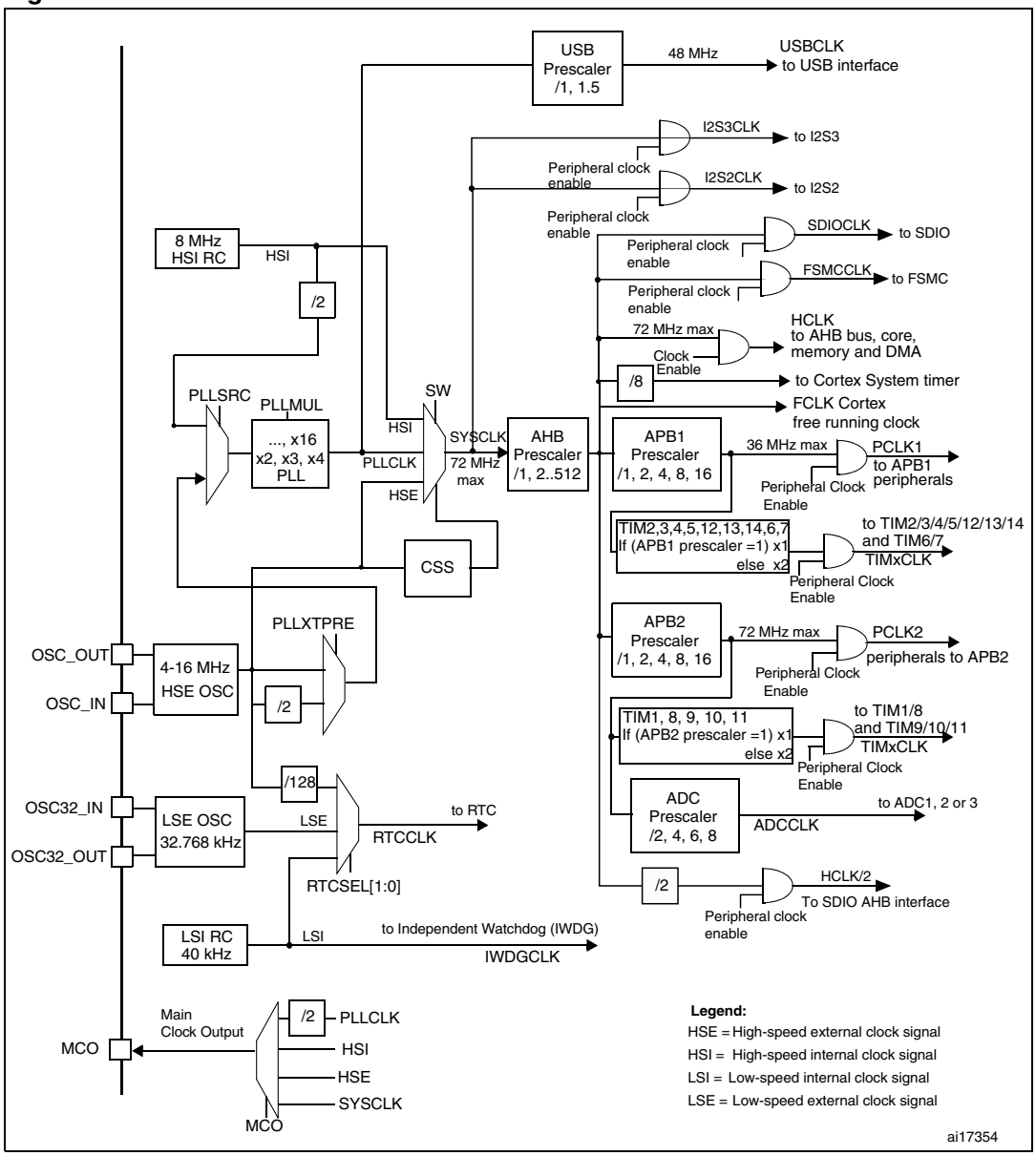
1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I^2S audio mode.

Figure 1. STM32F103xF and STM32F103xG performance line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 12*) or –40 °C to +105 °C (suffix 7, see *Table 12*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 48 MHz or 72 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

2.2 Full compatibility throughout the family

The STM32F103xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x4 and STM32F103x6 are identified as low-density devices, the STM32F103x8 and STM32F103xB are referred to as medium-density devices, the STM32F103xF, and STM32F103xG are referred to as high-density devices and the STM32F103xF and STM32F103xG are called XL-density devices.

Low-density, high-density and XL-density devices are an extension of the STM32F103x8/B medium-density devices, they are specified in the STM32F103x4/6, STM32F103xC/D/E and STM32F103xF/G datasheets, respectively. Low-density devices feature lower Flash memory and RAM capacities, less timers and peripherals. High-density devices have higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I^2S and DAC. XL-density devices bring even more Flash and RAM memory, and extra features, namely an MPU, a greater number of timers and a dual bank Flash structure while remaining fully compatible with the other members of the family.

The STM32F103x4, STM32F103x6, STM32F103xF, , STM32F103xG, STM32F103xF and STM32F103xG are a drop-in replacement for the STM32F103x8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Moreover, the STM32F103xx performance line family is fully compatible with all existing STM32F101xx access line and STM32F102xx USB access line devices.

Table 3. STM32F103xx family

<table>
<tr><th rowspan="3">Pinout</th><th colspan="2">Low-density devices</th><th colspan="2">Medium-density devices</th><th colspan="3">High-density devices</th><th colspan="2">XL-density devices</th></tr>
<tr><th>16 KB Flash</th><th>32 KB Flash(1)</th><th>64 KB Flash</th><th>128 KB Flash</th><th>256 KB Flash</th><th>384 KB Flash</th><th>512 KB Flash</th><th>768 KB Flash</th><th>1 MB Flash</th></tr>
<tr><th>6 KB RAM</th><th>10 KB RAM</th><th>20 KB RAM</th><th>20 KB RAM</th><th>48 or 64 KB(2) RAM</th><th>64 KB RAM</th><th>64 KB RAM</th><th>96 KB RAM</th><th>96 KB RAM</th></tr>
<tr><td>144</td><td colspan="4" rowspan="2"></td><td colspan="3" rowspan="3">5 × USARTs
4 × 16-bit timers,
2 × basic timers
3 × SPIs, 2 × I2Ss, 2 × I2Cs
USB, CAN, 2 × PWM timers
3 × ADCs, 2 × DACs,
1 × SDIO
FSMC (100- and 144-pin packages(3))</td><td colspan="2" rowspan="3">5 × USARTs
10 × 16-bit timers,
2 × basic timers
3 × SPIs, 2 × I2Ss, 2 × I2Cs
USB, CAN, 2 × PWM timers
3 × ADCs, 2 × DACs, 1 × SDIO,
Cortex-M3 with MPU
FSMC (100- and 144-pin packages(4)), dual bank Flash memory</td></tr>
<tr><td>100</td></tr>
<tr><td>64</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I2C,
USB, CAN,
1 × PWM timer
2 × ADCs</td><td colspan="2" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs, 2 × I2Cs,
USB, CAN,
1 × PWM timer
2 × ADCs</td></tr>
<tr><td>48</td><td colspan="3"></td></tr>
<tr><td>36</td><td colspan="5"></td></tr>
</table>

1. For orderable part numbers that do not show the A internal code after the temperature range code (6 or 7), the reference datasheet for electrical characteristics is that of the STM32F103x8/B medium-density devices.
2. 64 KB RAM for 256 KB Flash are available on devices delivered in CSP packages only.
3. Ports F and G are not available in devices delivered in 100-pin packages.
4. Ports F and G are not available in devices delivered in 100-pin packages.

2.3 Overview

2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xF and STM32F103xG performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3.3 Embedded Flash memory

768 Kbytes to 1 Mbyte of embedded Flash are available for storing programs and data. The Flash memory is organized as two banks. The first bank has a size of 512 Kbytes. The second bank is either 256 or 512 Kbytes depending on the device. This gives the device the capability of writing to one bank while executing code from the other bank (read-while-write capability).

2.3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.5 Embedded SRAM

96 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.6 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xF and STM32F103xG performance line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK}, is HCLK/2, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz

2.3.7 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.8 Nested vectored interrupt controller (NVIC)

The STM32F103xF and STM32F103xG performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.9 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.12 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.3.14 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.15 Low-power modes

The STM32F103xF and STM32F103xG performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.16 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I^2S, SDIO and ADC.

2.3.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.18 Timers and watchdogs

The XL-density STM32F103xx performance line devices include up to two advanced-control timers, up to ten general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. STM32F103xF and STM32F103xG timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9, TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10, TIM11 TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with

programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are10 synchronizable general-purpose timers embedded in the STM32F103xF and STM32F103xG performance line devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xF and STM32F103xG access line devices.

  These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

  Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

  These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- **TIM10, TIM11 and TIM9**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

- **TIM13, TIM14 and TIM12**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.20 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F103xF and STM32F103xG performance line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.22 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.3.23 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.
The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.25 Universal serial bus (USB)

The STM32F103xF and STM32F103xG performance line embed a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.3.26 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.3.27 ADC (analog to digital converter)

Three 12-bit analog-to-digital converters are embedded into STM32F103xF and STM32F103xG performance line devices and each ADC shares up to 21 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.3.28 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F103xF and STM32F103xG performance line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.3.29 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally

connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.30 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.31 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

3 Pinouts and pin descriptions

Figure 3. STM32F103xF and STM32F103xG XL-density performance line BGA144 ballout

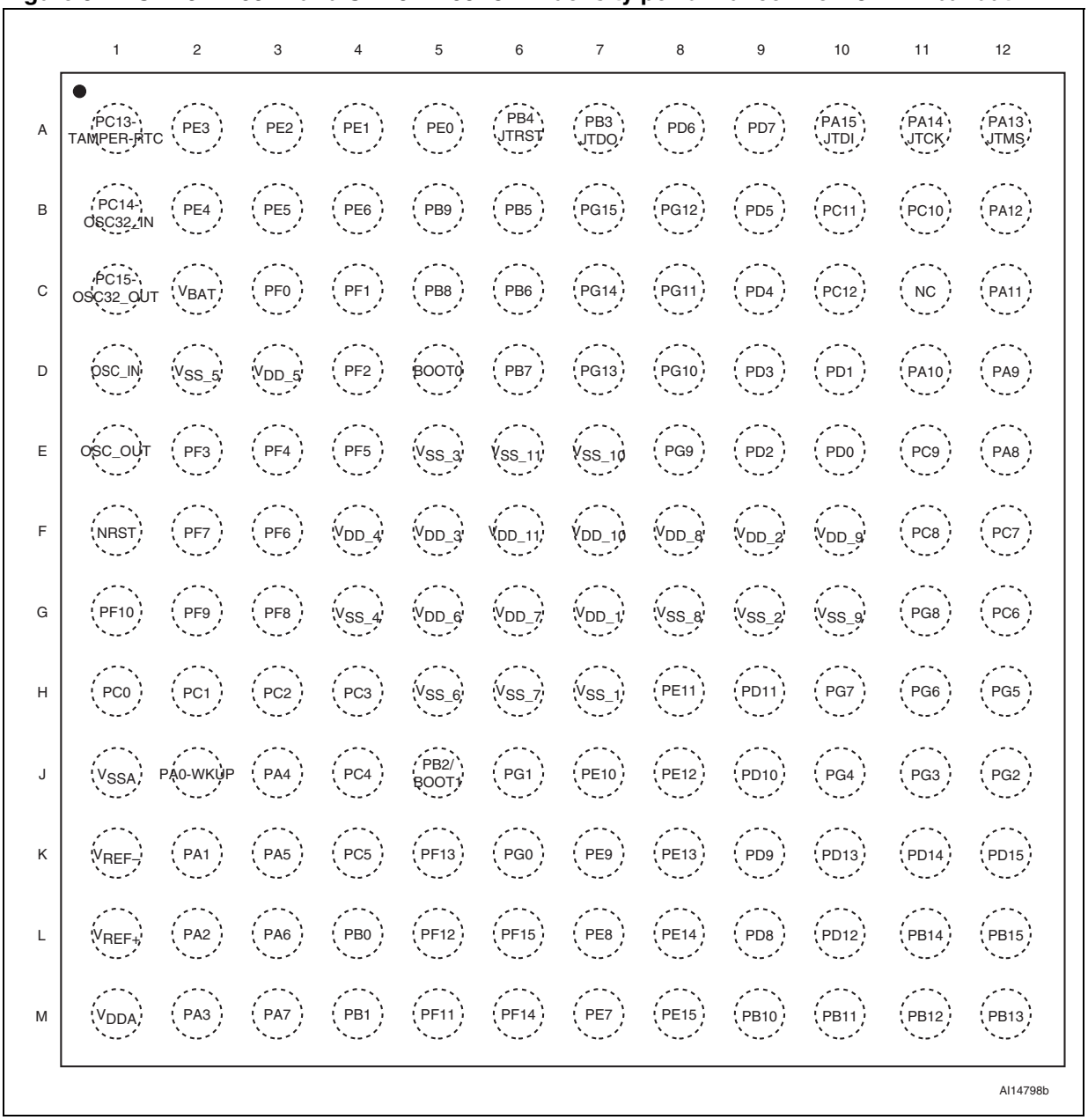


Figure 4. STM32F103xF and STM32F103xG XL-density performance line LQFP144 pinout

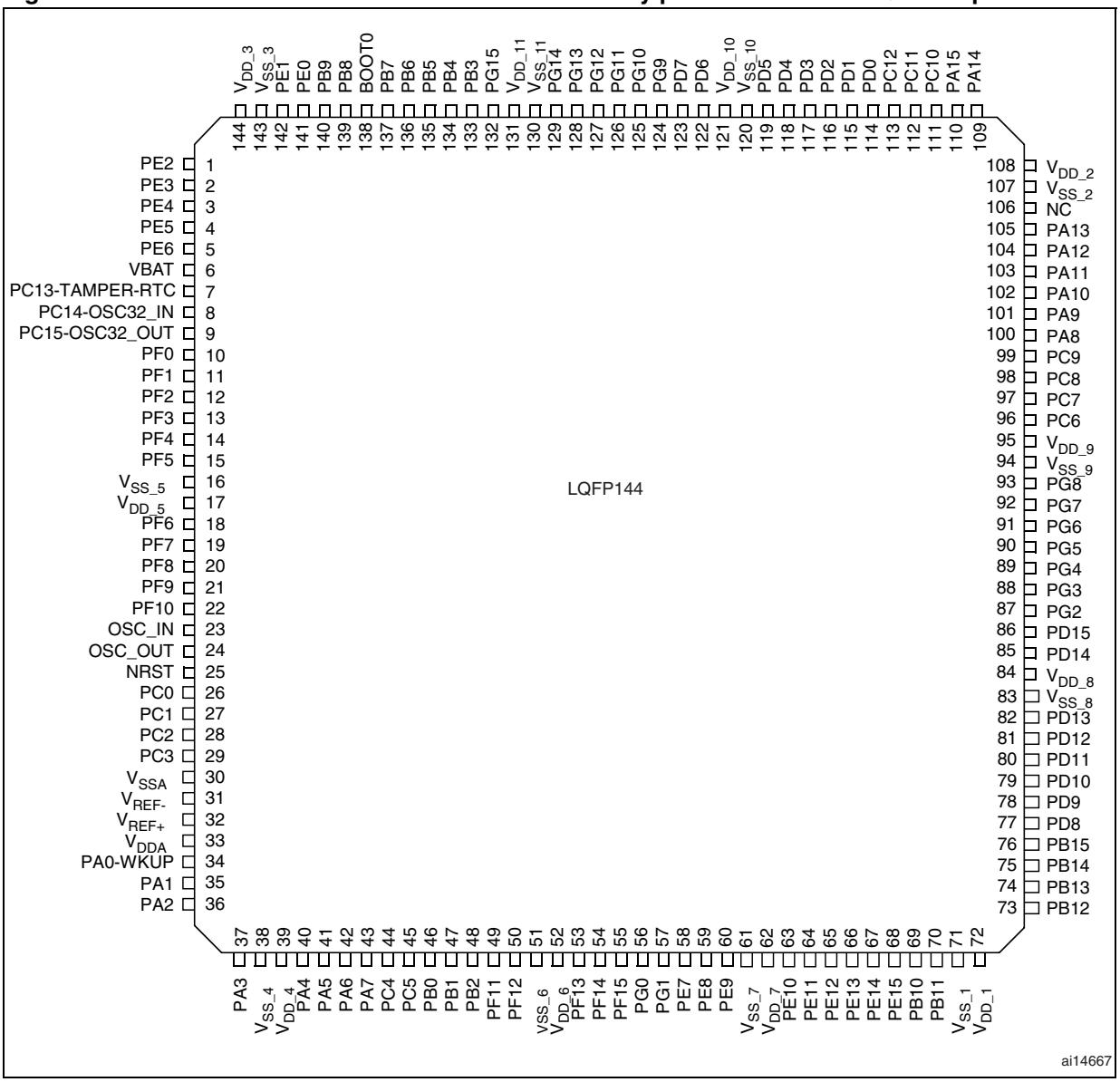


Figure 5. STM32F103xF and STM32F103xG XL-density performance line LQFP100 pinout

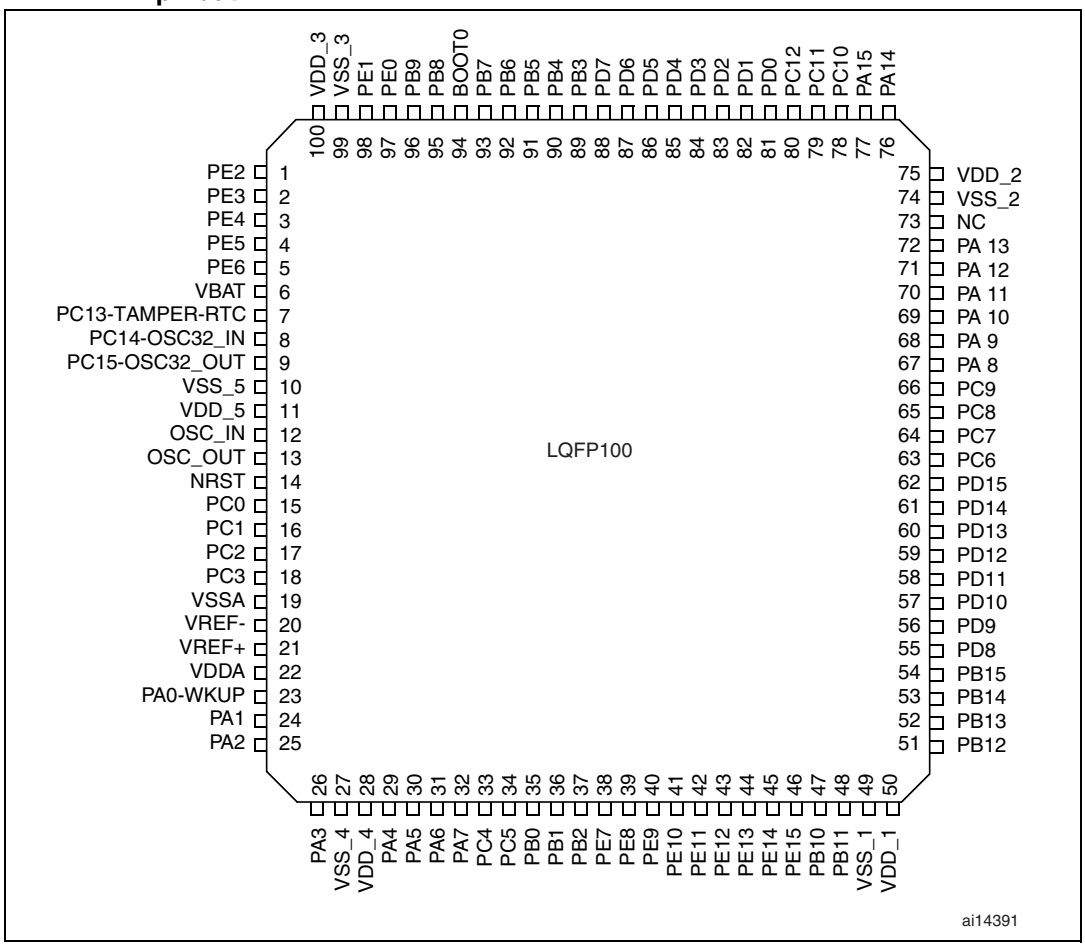


Figure 6. STM32F103xF and STM32F103xG XL-density performance line LQFP64 pinout

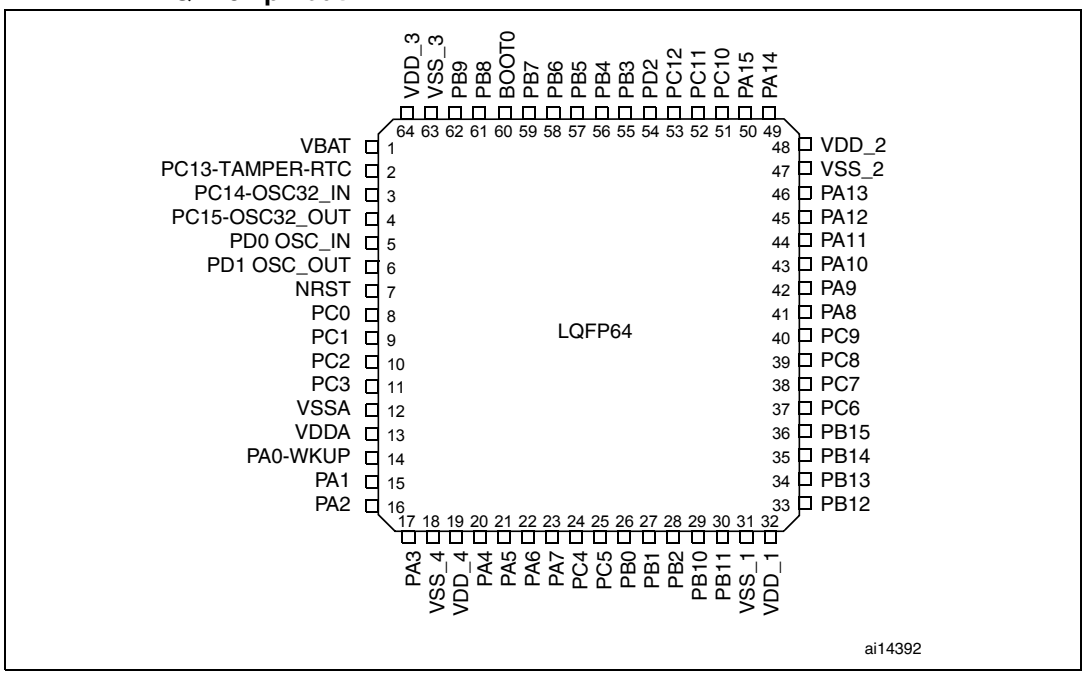


Table 5. STM32F103xF and STM32F103xG pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
A3	-	1	1	PE2	I/O	FT	PE2	TRACECK / FSMC_A23	
A2	-	2	2	PE3	I/O	FT	PE3	TRACED0 / FSMC_A19	
B2	-	3	3	PE4	I/O	FT	PE4	TRACED1/ FSMC_A20	
B3	-	4	4	PE5	I/O	FT	PE5	TRACED2/ FSMC_A21	TIM9_CH1
B4	-	5	5	PE6	I/O	FT	PE6	TRACED3 / FSMC_A22	TIM9_CH2
C2	1	6	6	V_{BAT}	S		V_{BAT}		
A1	2	7	7	PC13-TAMPER-RTC(5)	I/O		PC13(6)	TAMPER-RTC	
B1	3	8	8	PC14-OSC32_IN(5)	I/O		PC14(6)	OSC32_IN	
C1	4	9	9	PC15-OSC32_OUT(5)	I/O		PC15(6)	OSC32_OUT	
C3	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	
C4	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	
D4	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	
E2	-	-	13	PF3	I/O	FT	PF3	FSMC_A3	
E3	-	-	14	PF4	I/O	FT	PF4	FSMC_A4	
E4	-	-	15	PF5	I/O	FT	PF5	FSMC_A5	
D2	-	10	16	V_{SS_5}	S		V_{SS_5}		
D3	-	11	17	V_{DD_5}	S		V_{DD_5}		
F3	-	-	18	PF6	I/O		PF6	ADC3_IN4 / FSMC_NIORD	TIM10_CH1
F2	-	-	19	PF7	I/O		PF7	ADC3_IN5 / FSMC_NREG	TIM11_CH1
G3	-	-	20	PF8	I/O		PF8	ADC3_IN6 / FSMC_NIOWR	TIM3_CH1
G2	-	-	21	PF9	I/O		PF9	ADC3_IN7 / FSMC_CD	TIM14_CH1
G1	-	-	22	PF10	I/O		PF10	ADC3_IN8 / FSMC_INTR	
D1	5	12	23	OSC_IN	I		OSC_IN		
E1	6	13	24	OSC_OUT	O		OSC_OUT		
F1	7	14	25	NRST	I/O		NRST		
H1	8	15	26	PC0	I/O		PC0	ADC123_IN10	
H2	9	16	27	PC1	I/O		PC1	ADC123_IN11	
H3	10	17	28	PC2	I/O		PC2	ADC123_IN12	
H4	11	18	29	PC3	I/O		PC3	ADC123_IN13	
J1	12	19	30	V_{SSA}	S		V_{SSA}		
K1	-	20	31	V_{REF-}	S		V_{REF-}		

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
L1	-	21	32	V_{REF+}	S		V_{REF+}		
M1	13	22	33	V_{DDA}	S		V_{DDA}		
J2	14	23	34	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS[7] / ADC123_IN0 / TIM2_CH1_ETR / TIM5_CH1 / TIM8_ETR	
K2	15	24	35	PA1	I/O		PA1	USART2_RTS[8] / ADC123_IN1 / TIM5_CH2 / TIM2_CH2[8]	
L2	16	25	36	PA2	I/O		PA2	USART2_TX[8] / TIM5_CH3 / ADC123_IN2 / TIM9_CH1 / TIM2_CH3 [8]	
M2	17	26	37	PA3	I/O		PA3	USART2_RX[8] / TIM5_CH4 / ADC123_IN3 / TIM2_CH4[8]/ TIM9_CH2	
G4	18	27	38	V_{SS_4}	S		V_{SS_4}		
F4	19	28	39	V_{DD_4}	S		V_{DD_4}		
J3	20	29	40	PA4	I/O		PA4	SPI1_NSS[8] / USART2_CK[8] / DAC_OUT1 / ADC12_IN4	
K3	21	30	41	PA5	I/O		PA5	SPI1_SCK[8] / DAC_OUT2 / ADC12_IN5	
L3	22	31	42	PA6	I/O		PA6	SPI1_MISO[8] / TIM8_BKIN / ADC12_IN6 / TIM3_CH1[8]/ TIM13_CH1	TIM1_BKIN
M3	23	32	43	PA7	I/O		PA7	SPI1_MOSI[8]/ TIM8_CH1N / ADC12_IN7 / TIM3_CH2[8] / TIM14_CH1	TIM1_CH1N
J4	24	33	44	PC4	I/O		PC4	ADC12_IN14	
K4	25	34	45	PC5	I/O		PC5	ADC12_IN15	
L4	26	35	46	PB0	I/O		PB0	ADC12_IN8 / TIM3_CH3 / TIM8_CH2N	TIM1_CH2N
M4	27	36	47	PB1	I/O		PB1	ADC12_IN9 / TIM3_CH4[8] / TIM8_CH3N	TIM1_CH3N
J5	28	37	48	PB2	I/O	FT	PB2/BOOT1		
M5	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	
L5	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	
H5	-	-	51	V_{SS_6}	S		V_{SS_6}		
G5	-	-	52	V_{DD_6}	S		V_{DD_6}		
K5	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
M6	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	
L6	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	
K6	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	
J6	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	
M7	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	61	V_{SS_7}	S		V_{SS_7}		
G6	-	-	62	V_{DD_7}	S		V_{DD_7}		
J7	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL / USART3_TX[8]	TIM2_CH3
M10	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA / USART3_RX[8]	TIM2_CH4
H7	31	49	71	V_{SS_1}	S		V_{SS_1}		
G7	32	50	72	V_{DD_1}	S		V_{DD_1}		
M11	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS / I2S2_WS / I2C2_SMBA / USART3_CK[8] / TIM1_BKIN[8]	
M12	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK / I2S2_CK / USART3_CTS[8] / TIM1_CH1N	
L11	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO / TIM1_CH2N / USART3_RTS[8]/ TIM12_CH1	
L12	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI / I2S2_SD / TIM1_CH3N[8] / TIM12_CH2	
L9	-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
H9	-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
K10	-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	83	V_{SS_8}	S		V_{SS_8}		
F8	-	-	84	V_{DD_8}	S		V_{DD_8}		
K11	-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	-	-	87	PG2	I/O	FT	PG2	FSMC_A12	
J11	-	-	88	PG3	I/O	FT	PG3	FSMC_A13	
J10	-	-	89	PG4	I/O	FT	PG4	FSMC_A14	
H12	-	-	90	PG5	I/O	FT	PG5	FSMC_A15	
H11	-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	
H10	-	-	92	PG7	I/O	FT	PG7	FSMC_INT3	
G11	-	-	93	PG8	I/O	FT	PG8		
G10	-	-	94	V_{SS_9}	S		V_{SS_9}		
F10	-	-	95	V_{DD_9}	S		V_{DD_9}		
G12	37	63	96	PC6	I/O	FT	PC6	I2S2_MCK / TIM8_CH1 / SDIO_D6	TIM3_CH1
F12	38	64	97	PC7	I/O	FT	PC7	I2S3_MCK / TIM8_CH2 / SDIO_D7	TIM3_CH2
F11	39	65	98	PC8	I/O	FT	PC8	TIM8_CH3 / SDIO_D0	TIM3_CH3
E11	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4 / SDIO_D1	TIM3_CH4
E12	41	67	100	PA8	I/O	FT	PA8	USART1_CK / TIM1_CH1[8] / MCO	
D12	42	68	101	PA9	I/O	FT	PA9	USART1_TX[8] / TIM1_CH2[8]	
D11	43	69	102	PA10	I/O	FT	PA10	USART1_RX[8] / TIM1_CH3[8]	
C12	44	70	103	PA11	I/O	FT	PA11	USART1_CTS / USBDM / CAN_RX[8] / TIM1_CH4[8]	
B12	45	71	104	PA12	I/O	FT	PA12	USART1_RTS / USBDP / CAN_TX[8] / TIM1_ETR[8]	
A12	46	72	105	PA13	I/O	FT	JTMS-SWDIO		PA13
C11	-	73	106	Not connected					
G9	47	74	107	V_{SS_2}	S		V_{SS_2}		
F9	48	75	108	V_{DD_2}	S		V_{DD_2}		
A11	49	76	109	PA14	I/O	FT	JTCK-SWCLK		PA14

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
A10	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS / I2S3_WS	TIM2_CH1_ETR PA15 / SPI1_NSS
B11	51	78	111	PC10	I/O	FT	PC10	UART4_TX / SDIO_D2	USART3_TX
B10	52	79	112	PC11	I/O	FT	PC11	UART4_RX / SDIO_D3	USART3_RX
C10	53	80	113	PC12	I/O	FT	PC12	UART5_TX / SDIO_CK	USART3_CK
E10	5	81	114	PD0	I/O	FT	OSC_IN[8]	FSMC_D2[9]	CAN_RX
D10	6	82	115	PD1	I/O	FT	OSC_OUT[9]	FSMC_D3[9]	CAN_TX
E9	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR / UART5_RX / SDIO_CMD	
D9	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
C9	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	120	V_{SS_10}	S		V_{SS_10}		
F7	-	-	121	V_{DD_10}	S		V_{DD_10}		
A8	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
A9	-	88	123	PD7	I/O	FT	PD7	FSMC_NE1 / FSMC_NCE2	USART2_CK
E8	-	-	124	PG9	I/O	FT	PG9	FSMC_NE2 / FSMC_NCE3	
D8	-	-	125	PG10	I/O	FT	PG10	FSMC_NCE4_1 / FSMC_NE3	
C8	-	-	126	PG11	I/O	FT	PG11	FSMC_NCE4_2	
B8	-	-	127	PG12	I/O	FT	PG12	FSMC_NE4	
D7	-	-	128	PG13	I/O	FT	PG13	FSMC_A24	
C7	-	-	129	PG14	I/O	FT	PG14	FSMC_A25	
E6	-	-	130	V_{SS_11}	S		V_{SS_11}		
F6	-	-	131	V_{DD_11}	S		V_{DD_11}		
B7	-	-	132	PG15	I/O	FT	PG15		
A7	55	89	133	PB3/	I/O	FT	JTDO	SPI3_SCK / I2S3_CK/	PB3/TRACESWO TIM2_CH2 / SPI1_SCK
A6	56	90	134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1 SPI1_MISO
B6	57	91	135	PB5	I/O		PB5	I2C1_SMBA / SPI3_MOSI / I2S3_SD	TIM3_CH2 / SPI1_MOSI
C6	58	92	136	PB6	I/O	FT	PB6	I2C1_SCL[7]/ TIM4_CH1[7]	USART1_TX
D6	59	93	137	PB7	I/O	FT	PB7	I2C1_SDA[7] / FSMC_NADV / TIM4_CH2[7]	USART1_RX

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type[1]	I / O level[2]	Main function[3] (after reset)	Alternate functions[4]	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
D5	60	94	138	BOOT0	I		BOOT0		
C5	61	95	139	PB8	I/O	FT	PB8	TIM4_CH3[7] / SDIO_D4	I2C1_SCL/ CAN_RX
B5	62	96	140	PB9	I/O	FT	PB9	TIM4_CH4[7] / SDIO_D5	I2C1_SDA / CAN_TX
A5	-	97	141	PE0	I/O	FT	PE0	TIM4_ETR / FSMC_NBL0	
A4	-	98	142	PE1	I/O	FT	PE1	FSMC_NBL1	
E5	63	99	143	V_{SS_3}	S		V_{SS_3}		
F5	64	100	144	V_{DD_3}	S		V_{DD_3}		

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
8. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 6. FSMC pin definition

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2			A23	A23		Yes
PE3			A19	A19		Yes
PE4			A20	A20		Yes
PE5			A21	A21		Yes
PE6			A22	A22		Yes
PF0	A0	A0	A0			-
PF1	A1	A1	A1			-
PF2	A2	A2	A2			-
PF3	A3		A3			-
PF4	A4		A4			-
PF5	A5		A5			-
PF6	NIORD	NIORD				-
PF7	NREG	NREG				-
PF8	NIOWR	NIOWR				-
PF9	CD	CD				-
PF10	INTR	INTR				-
PF11	NIOS16	NIOS16				-
PF12	A6		A6			-
PF13	A7		A7			-
PF14	A8		A8			-
PF15	A9		A9			-
PG0	A10		A10			-
PG1			A11			-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

Table 6. FSMC pin definition (continued)

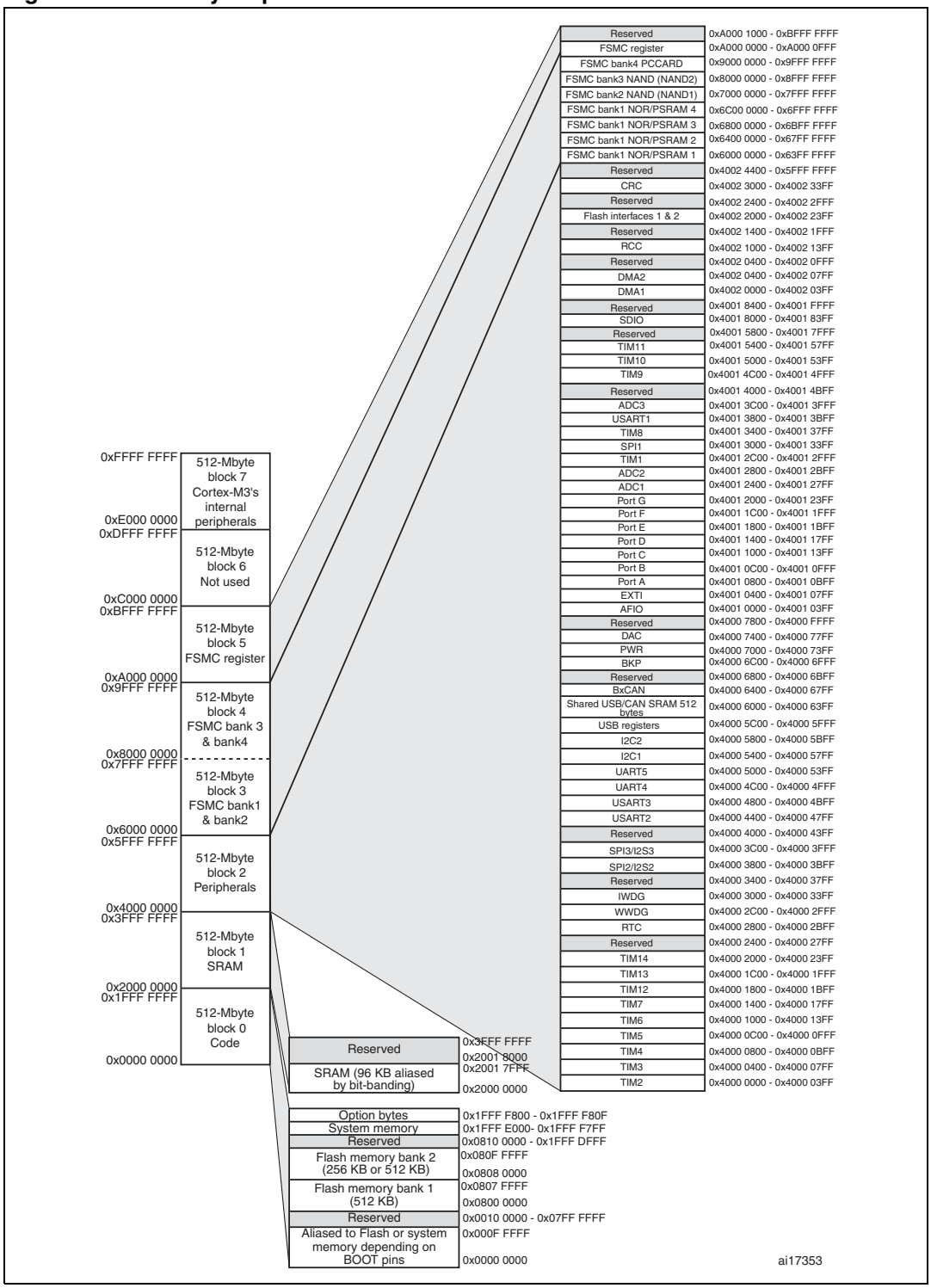
Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11			A16	A16	CLE	Yes
PD12			A17	A17	ALE	Yes
PD13			A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2			A12			-
PG3			A13			-
PG4			A14			-
PG5			A15			-
PG6					INT2	-
PG7					INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3			CLK	CLK		Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7			NE1	NE1	NCE2	Yes
PG9			NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3		-
PG11	NCE4_2	NCE4_2				-
PG12			NE4	NE4		-
PG13			A24	A24		-
PG14			A25	A25		-
PB7			NADV	NADV		Yes
PE0			NBL0	NBL0		Yes
PE1			NBL1	NBL1		Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

4 Memory mapping

The memory map is shown in *Figure 7*.

Figure 7. Memory map

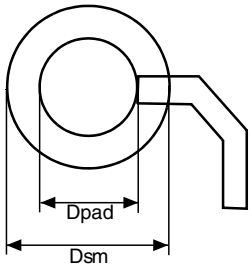


5 Package characteristics

5.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

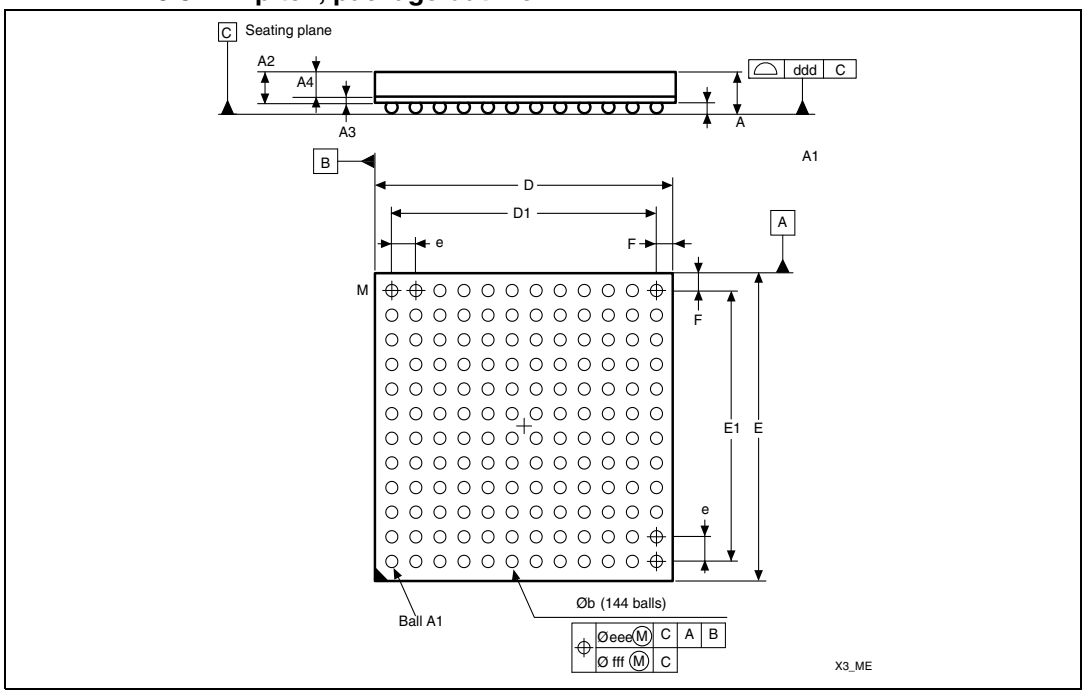
Figure 8. Recommended PCB design rules (0.80/0.75 mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

ai15469

Figure 9. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 7. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A			1.70			0.0669
A1	0.21			0.0083		
A2		1.07			0.0421	
A3		0.27			0.0106	
A4			0.85			0.0335
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	9.85	10.00	10.15	0.3878	0.3937	0.3996
D1		8.80			0.3465	
E	9.85	10.00	10.15	0.3878	0.3937	0.3996
E1		8.80			0.3465	
e		0.80			0.0315	
F		0.60			0.0236	
ddd		0.10			0.0039	
eee		0.15			0.0059	
fff		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 10. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline(1)

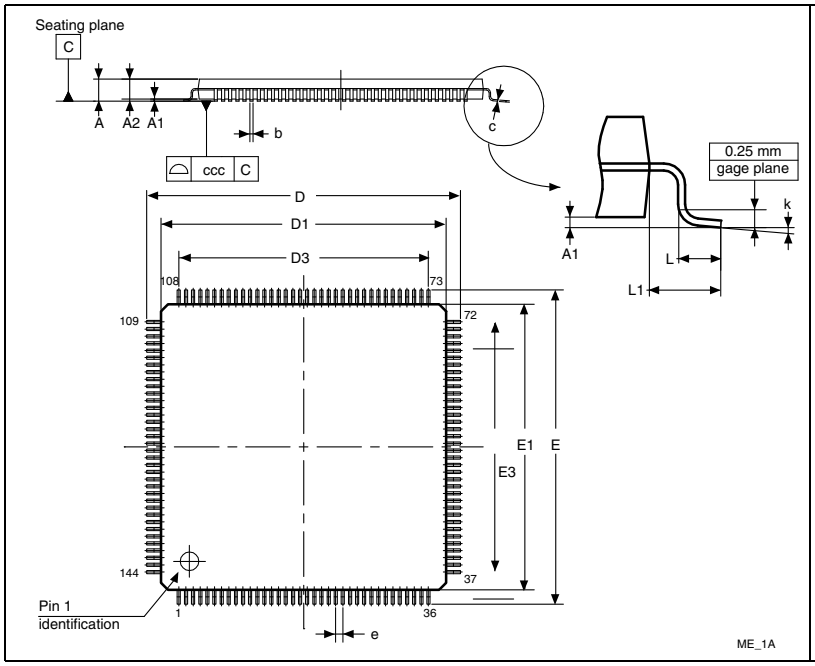
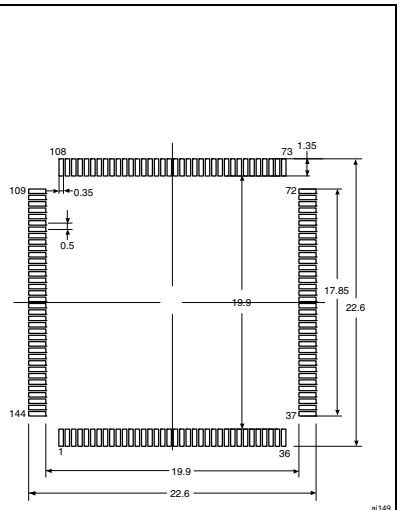


Figure 11. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 8. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	21.80	22.00	22.20	0.8583	0.8661	0.874
D1	19.80	20.00	20.20	0.7795	0.7874	0.7953
D3		17.50			0.689	
E	21.80	22.00	22.20	0.8583	0.8661	0.874
E1	19.80	20.00	20.20	0.7795	0.7874	0.7953
E3		17.50			0.689	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 12. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline(1)

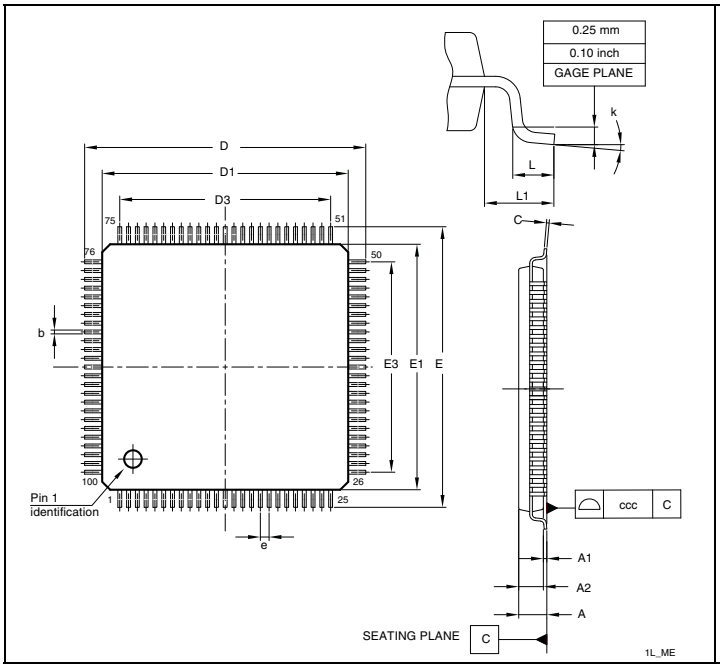
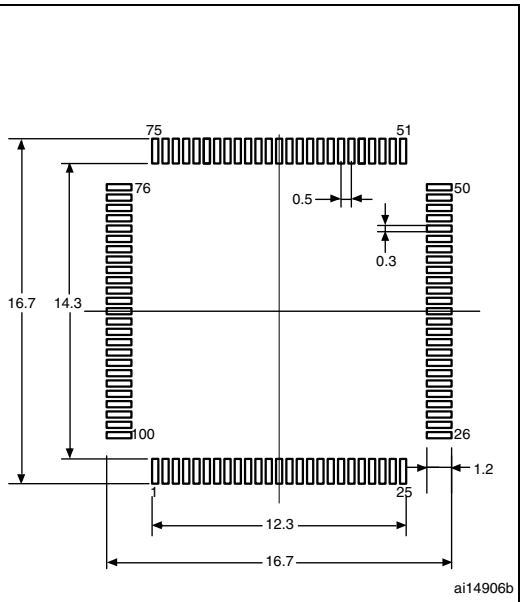


Figure 13. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 9. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D	15.80	16.00	16.20	0.622	0.6299	0.6378
D1	13.80	14.00	14.20	0.5433	0.5512	0.5591
D3		12.00			0.4724	
E	15.80	16.00	16.20	0.622	0.6299	0.6378
E1	13.80	14.00	14.20	0.5433	0.5512	0.5591
E3		12.00			0.4724	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 14. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline(1)

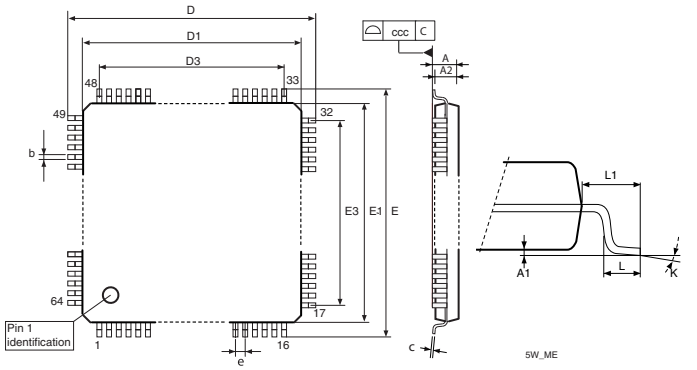
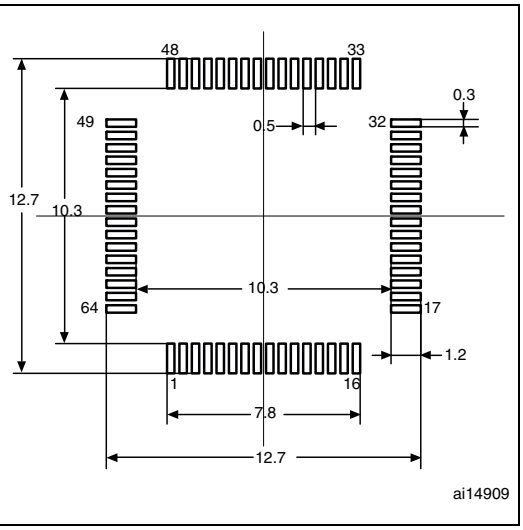


Figure 15. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 10. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D.		7.500				
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.00	10.200	0.3858	0.3937	0.4016
e		0.500			0.0197	
k	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.75	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc		0.080			0.0031	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5.2 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max x } \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 11. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LFBGA144 - 10 × 10 mm / 0.8 mm pitch	40	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	30	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	

5.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

5.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 12: STM32F103xF and STM32F103xG ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xF and STM32F103xG at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 11* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 12: STM32F103xF and STM32F103xG ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 11* T_{Jmax} is calculated as follows:

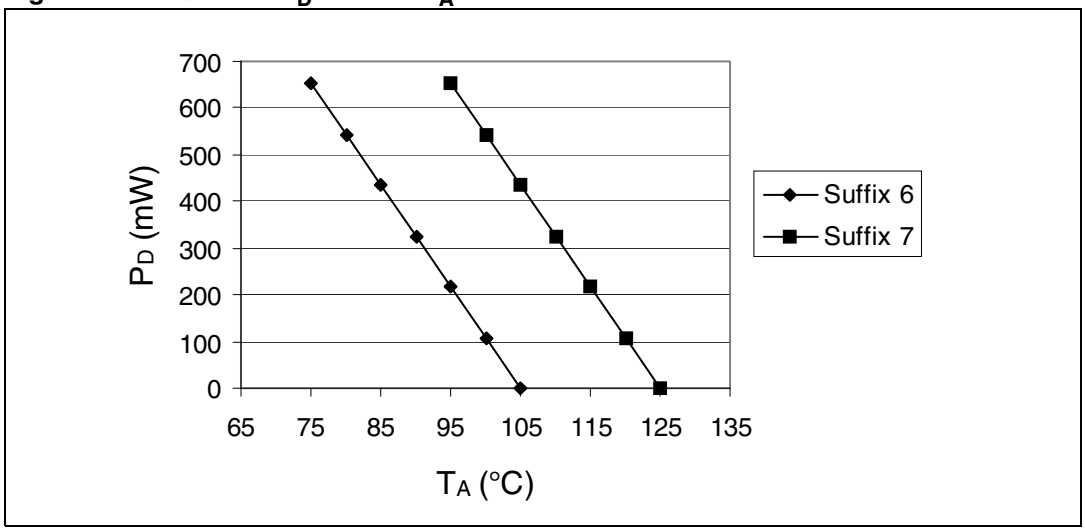
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 12: STM32F103xF and STM32F103xG ordering information scheme*).

Figure 16. LQFP100 P_D max vs. T_A



6 Part numbering

Table 12. STM32F103xF and STM32F103xG ordering information scheme

Example: STM32 F103 R F T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

103 = performance line

Pin count

R = 64 pins
V = 100 pins
Z = 144 pins

Flash memory size

F = 768 Kbytes of Flash memory
G = 1 Mbyte of Flash memory

Package

H = BGA
T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
17-Feb-2010	1	Initial release.
04-Mar-2010	2	LQFP64 package mechanical data updated: see *Figure 14: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 10: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Internal code removed from *Table 12: STM32F103xF and STM32F103xG ordering information scheme*.

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