OKI Semiconductor

MSM6652/53/54/55/56-xxx, MSM6652A/53A/ 54A/55A/56A/58A-xxx, MSM66P54-xx, MSM66P56-xx, MSM6650

Internal Mask ROM Voice Synthesis IC, Internal One-Time-Programmable (OTP) ROM Voice Synthesis IC, External ROM Drive Voice Synthesis IC

This document contains minimum specifications. For full specifications, please contact your nearest Oki office or representative.

GENERAL DESCRIPTION

The MSM6650 family is the successor to OKI's MSM6375 family. To ensure high-quality voice synthesis, the MSM6650 family members offer adaptive differential pulse-code modulation (ADPCM) playback, pulse-code modulation (PCM) playback, 12-bit D/A conversion, and on-chip –40 dB/ octave low-pass filter (LPF).

The conventional "beep" tones and 2-channel playback are now easier to use. OKI has added additional functions such as melody play, fade-out, and random playback. OKI has improved external control by adding an Edit ROM. The Edit ROM can be used to form sentences by linking phrases.

The MSM6650 family members can support a variety of applications as it can function in either Standalone Mode or Microcontroller Interface Mode. In Microcontroller Interface Mode, serial input control is available. Serial input control minimizes the number of microcontroller port pins required for voice synthesis control. The MSM6650 family includes an internal mask ROM version, internal one-time-programmable (OTP) ROM version, and external ROM version. The features of the MSM6650 family devices are as follows.

- MSM6652/53/54/55/56-xxx
  These devices are single-chip voice synthesizers with an on-chip mask ROM using the CMOS technology.
  Standalone Mode or Microcontroller Interface Mode can be selected by mask option.
- MSM6652A/53A/54A/55A/56A/58A-xxx
  The trial production period for these devices is shorter than those described above. These devices are suitable for developing prototype models and concept demonstration of new products.
- MSM66P54-xx, MSM66P56-xx
  The device is a single-chip CMOS voice synthesizer with one-time-programmable (OTP) ROM. Standalone and Microcontroller Interface Modes are selected by using a code (01-04).
  The user can easily write voice data using the development tool AR761 or AR762, or P54 adapter. Unlike the mask ROM version, the OTP version is suited to applications which requires a small lot production of different type devices or short delivery time.
- MSM6650
  The MSM6650 device can directly connect external ROM or EPROM of up to 64 Mbits, which stores voice data.
  This device is ideally suited to an evaluation IC for the MSM6650 family because its circuit configuration is identical to those of the mask ROM-based and OTP version devices.

• Option Table

	Pin Name	Microcontroller Interface Mode		Standalone Mode		
		Serial Input	**Parallel Input**	**With Standby**	**No Standby**	
MSM6652/53/54/55/56	—	Mask Option				*1
MSM6652A/53A/54A/55A/56A/58A						
MSM66P54/P56	—	−01	−02	−03	−04	*2
MSM6650	CPU	"H"	"H"	"L"	"L"	
	SERIAL	"H"	"L"	"L"	"L"	
	STBY	—	—	"L"	"H"	

*1. The options for the mask ROM-based devices are mask options. The user should send OKI an option list before starting development. A sample of option list is shown below.

*2. A code of OTP version device corresponds to one of the options. The user should specify either MSM66P54-03 or MSM66P54-04 or MSM66P56-03 or MSM66P56-04. (In this case, no option list is required.)

Oki Electric Industry Co., Ltd.

Date:

Option List

You are requested to develop MSM665X-XXX on the following conditions.

1. Options
There are four options for the MSM6650 family.
Choose and circle the desired option.

Option	Interface mode	Input	Standby conversion
Option A	Microcontroller	Serial	—
Option B	Microcontroller	Parallel	—
Option C	Standalone	—	Yes
Option D	Standalone	—	No

2. Package and quantity

Item	Package (circle the desired one)			Quantity	Note
Ceramic sample	18-pin DIP (ceramic)	24-pin SOP (ceramic)	chip	____ pcs	Up to 10 samples. Operating temp. : 10 to 30°C
Mold sample	18-pin DIP (plastic)	24-pin SOP (plastic)	chip	____ pcs	Up to 50 samples
Mass produc-tion	18-pin DIP (plastic)	24-pin SOP (plastic)	chip	____ pcs per lot monthly	

Signed by ____
Title :
Company name :

OKI Semiconductor

STANDALONE MODE

FEATURES

Device name	ROM size	Maximum playback time (sec)			
		f_{SAM}=4.0 kHz	f_{SAM}=6.4 kHz	f_{SAM}=8.0 kHz	f_{SAM}=16 kHz
MSM6652, 6652A	288 Kbits	16.9	10.5	8.4	4.2
MSM6653, 6653A	544 Kbits	31.2	19.5	15.6	7.8
MSM6654, 6654A	1 Mbit	63.8	39.9	31.9	15.9
MSM6655, 6655A	1.5 Mbits	96.5	60.3	48.2	24.1
MSM6656, 6656A	2 Mbits	129.1	80.7	64.5	32.2
MSM6658A	4 Mbits	259.7	162.9	129.8	64.9
MSM66P54	1 Mbit	63.8	39.9	31.9	15.9
MSM66P56	2 Mbit	129.1	80.7	64.5	32.2
MSM6650	64 Mbits (Max)	4194.3	2620.5	2096.4	1048.2

Note: Actual voice ROM area is smaller by 22 Kbits.

- 4-bit ADPCM or 8-bit PCM sound generation
- Melody function
- Edit ROM function
- Two-channel mixing function
- Built-in random playback function
- Fade-out function via four-step sound volume attenuation
- Built-in beep tone of 0.5 kHz, 1.0 kHz, 1.3 kHz, or 2.0 kHz selectable with a specific code
- Sampling frequency of 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, or 32.0 kHz (32 kHz sampling is not possible when using RC oscillation)
- Up to 120 phrases
- Built-in 12-bit D/A converter
- Built-in –40 dB/octave low-pass filter
- Standby function
- Selectable RC or ceramic oscillation
- Package options:
  18-pin plastic DIP (DIP18-P-300-2.54)   (Product name: MSM6652-xxxRS/MSM6653-xxxRS/ MSM6654-xxxRS/MSM6655-xxxRS/ MSM6656-xxxRS/MSM6652A-xxxRS/ MSM6653A-xxxRS/MSM6654A-xxxRS/ MSM6655A-xxxRS/MSM6656A-xxxRS/ MSM6658A-xxxRS)
  24-pin plastic SOP (SOP24-P-430-1.27-K) (Product name: MSM6652-xxxGS-K/MSM6653-xxxGS-K/ MSM6654-xxxGS-K/MSM6655-xxxGS-K/ MSM6656-xxxGS-K/MSM6652A-xxxGS-K/ MSM6653A-xxxGS-K/MSM6654A-xxxGS-K/ MSM6655A-xxxGS-K/MSM6656A-xxxGS-K/ MSM6658A-xxxGS-K/MSM66P54-03GS-K/ MSM66P54-04GS-K/MSM66P56-03GS-K/ MSM66P56-04GS-K)
  20-pin plastic DIP (DIP20-P-300-2.54-W1)   (Product name: MSM66P54-03RS/MSM66P54-04RS/ MSM66P56-03RS/MSM66P56-04RS)
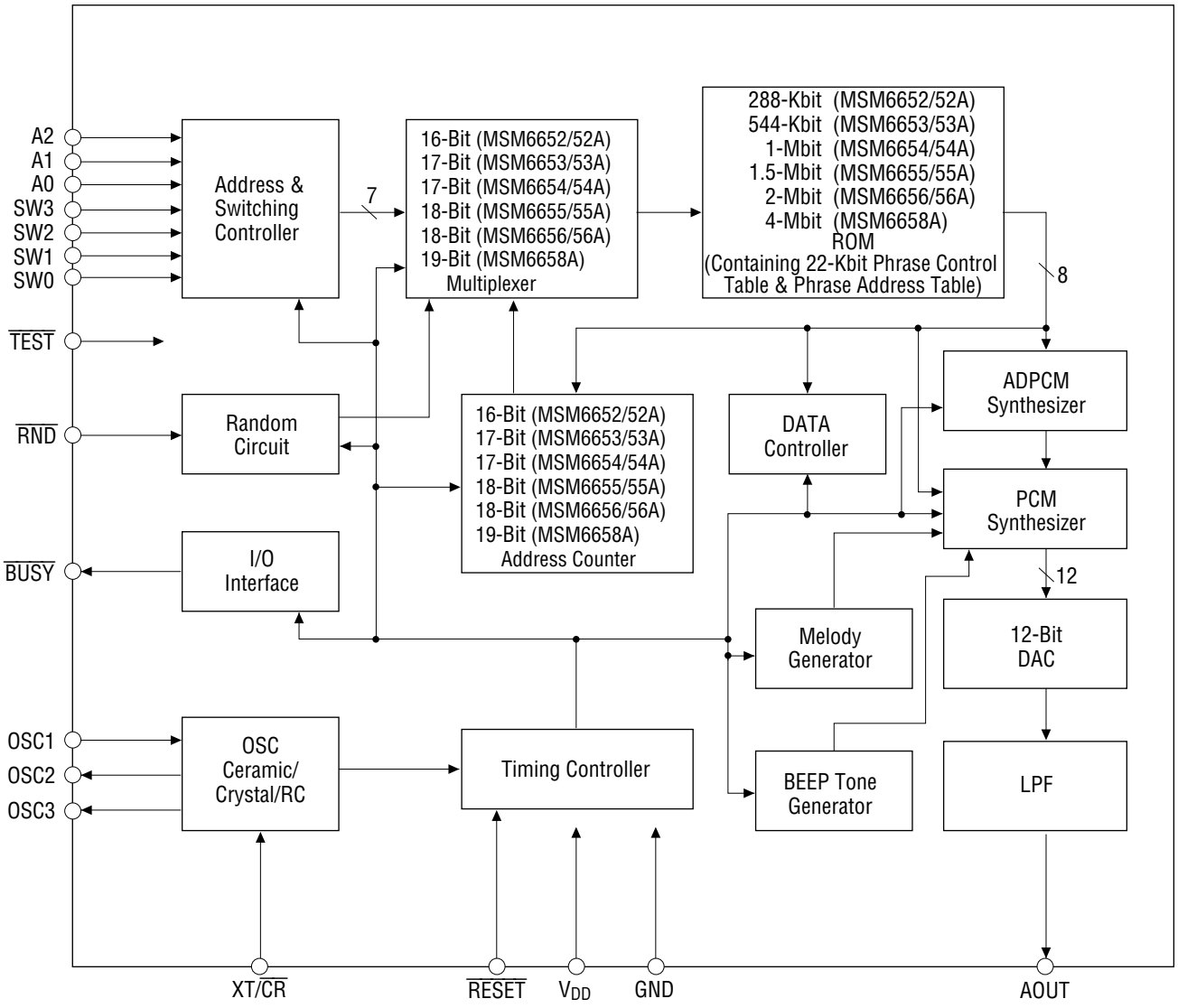 64-pin plastic QFP (QFP64-P-1420-1.00-BK) (Product name: MSM6650GS-BK)
  64-pin plastic SDIP (SDIP64-P-750-1.778)   (Product name: MSM6650SS)

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BLOCK DIAGRAMS

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RA22 ------------------------------------ RA0   D7 -------------- D0

A2
A1
A0
SW3
SW2
SW1
SW0

Address &
Switching
Controller

7

23-Bit Multiplexer

8-Bit LATCH

8

TEST1, 3

RND

Random
Circuit

23-Bit Address
Counter

DATA
Controller

ADPCM
Synthesizer

PCM
Synthesizer

12

CE
RCS
BUSY
NAR
IBUSY
STANDBY

I/O
Interface

Melody
Generator

12-Bit
DAC

XT/OSC1
XT/OSC2
OSC3

OSC
(Ceramic/
Crystal/RC)

Timing Controller

BEEP Tone
Generator

LPF

XT/CR   RESET   CPU   STBY   TEST2   DV$_{DD}$ DGND   AGND   AV$_{DD}$ AOUT

MSM6650 Family

FEDL6650-03

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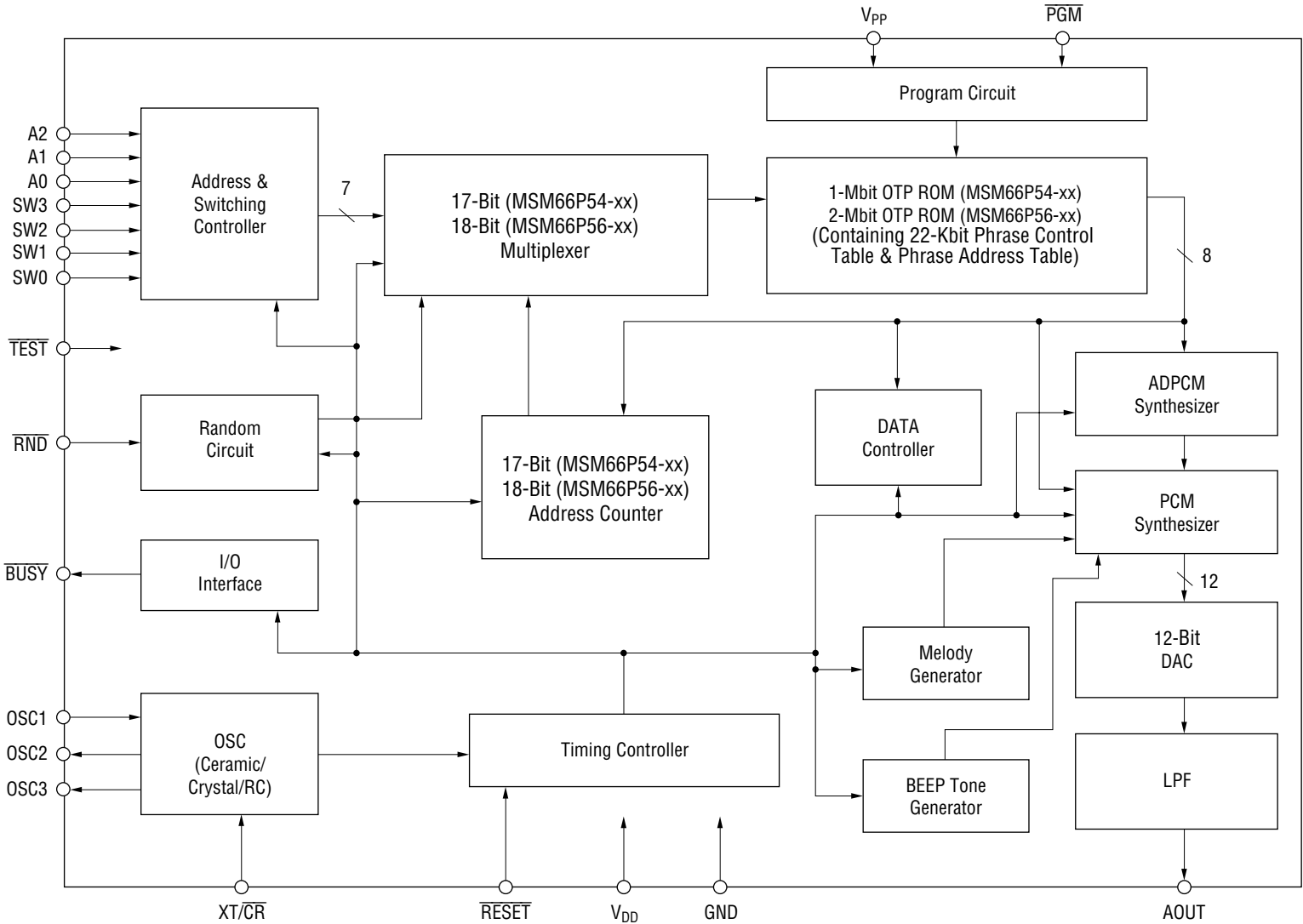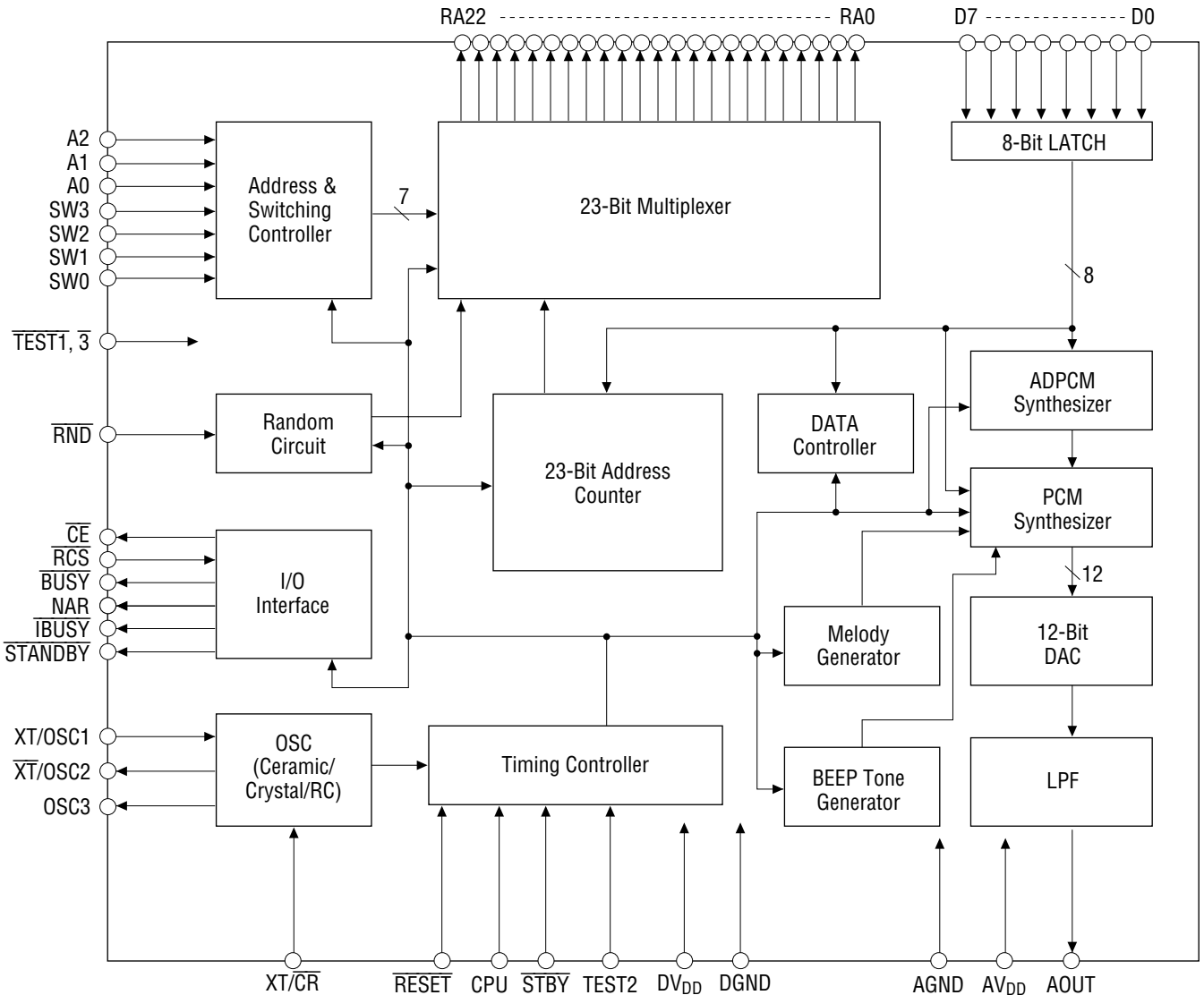
PIN CONFIGURATION (TOP VIEW)

The MSM66P54-xx and MSM66P56-xx has two more pins than the MSM6652-6658A while their pin configurations are identical.

The additional two pins (V_{PP}, $\overline{PGM}$) of the MSM66P54-xx/P56-xx may be open at playback after completion of writing.

MSM6652-6658A (Mask ROM)

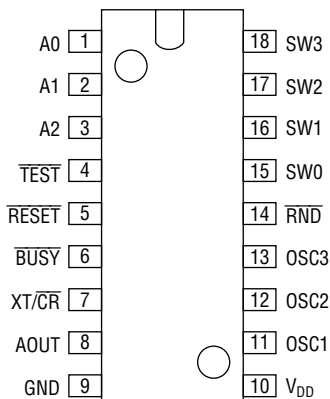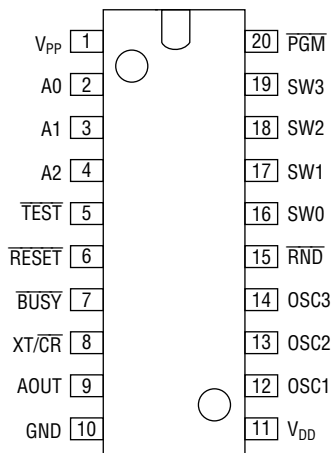|				
A0	1		18	SW3
A1	2		17	SW2
A2	3		16	SW1
$\overline{TEST}$	4		15	SW0
$\overline{RESET}$	5		14	$\overline{RND}$
$\overline{BUSY}$	6		13	OSC3
XT/$\overline{CR}$	7		12	OSC2
AOUT	8		11	OSC1
GND	9		10	V_{DD}

18-Pin Plastic DIP

MSM66P54/P56 (OTP)

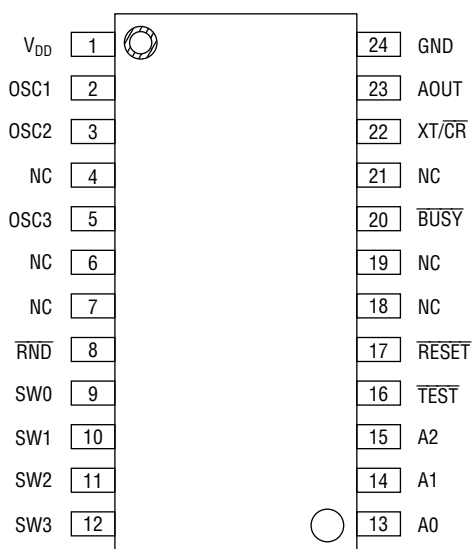|				
V_{PP}	1		20	$\overline{PGM}$
A0	2		19	SW3
A1	3		18	SW2
A2	4		17	SW1
$\overline{TEST}$	5		16	SW0
$\overline{RESET}$	6		15	$\overline{RND}$
$\overline{BUSY}$	7		14	OSC3
XT/$\overline{CR}$	8		13	OSC2
AOUT	9		12	OSC1
GND	10		11	V_{DD}

20-Pin Plastic DIP

MSM6652-xxxRS, MSM6653-xxxRS, MSM6654-xxxRS, MSM6655-xxxRS, MSM6656-xxxRS, MSM6652A-xxxRS, MSM6653A-xxxRS, MSM6654A-xxxRS, MSM6655A-xxxRS, MSM6656A-xxxRS, MSM6658A-xxxRS
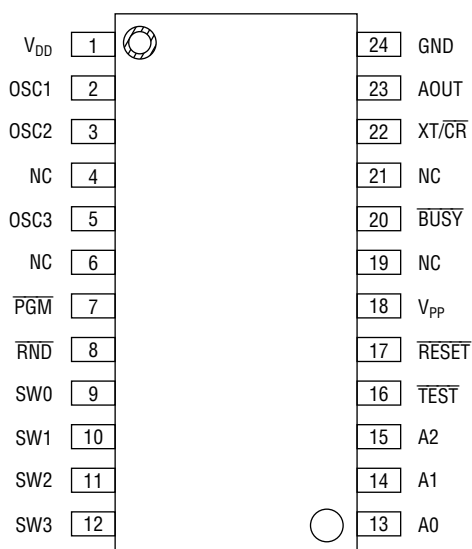
MSM66P54-03/-04RS
MSM66P56-03/-04RS

MSM6652-6658A (Mask ROM)

V_{DD}	1		24	GND
OSC1	2		23	AOUT
OSC2	3		22	XT/$\overline{CR}$
NC	4		21	NC
OSC3	5		20	$\overline{BUSY}$
NC	6		19	NC
NC	7		18	NC
$\overline{RND}$	8		17	$\overline{RESET}$
SW0	9		16	$\overline{TEST}$
SW1	10		15	A2
SW2	11		14	A1
SW3	12		13	A0

24-Pin Plastic SOP

MSM66P54/P56 (OTP)

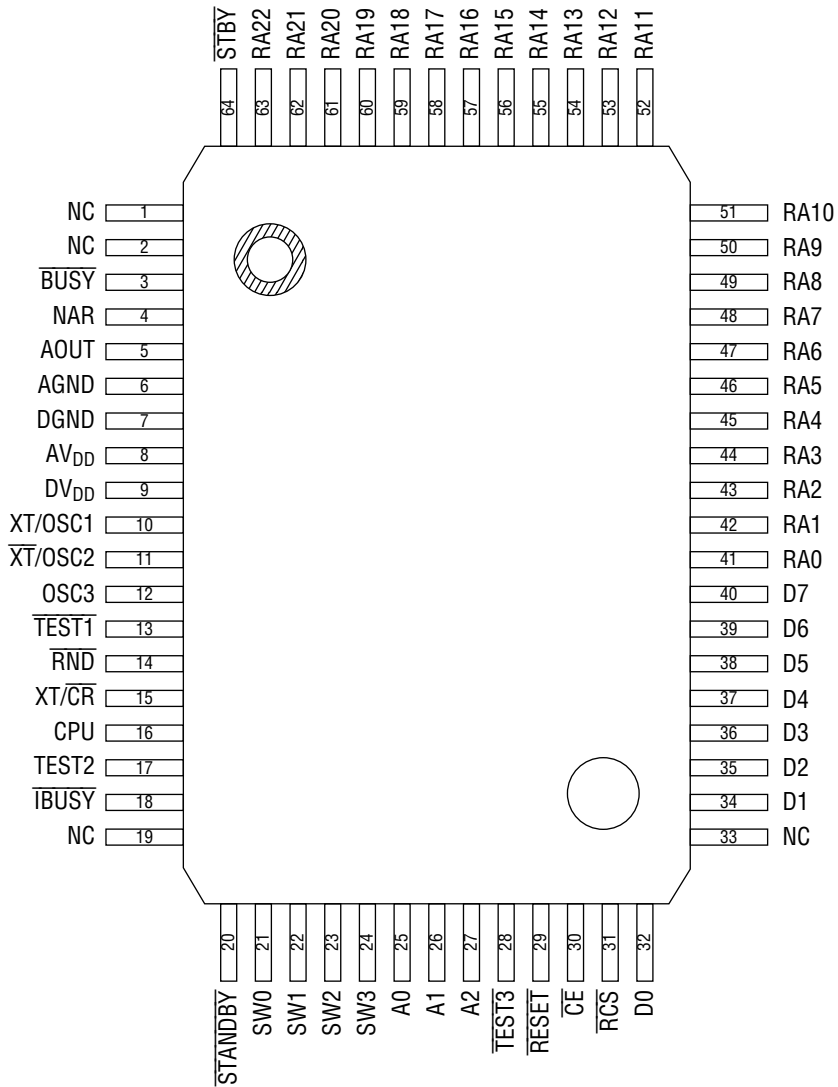|				
V_{DD}	1		24	GND
OSC1	2		23	AOUT
OSC2	3		22	XT/$\overline{CR}$
NC	4		21	NC
OSC3	5		20	$\overline{BUSY}$
NC	6		19	NC
$\overline{PGM}$	7		18	V_{PP}
$\overline{RND}$	8		17	$\overline{RESET}$
SW0	9		16	$\overline{TEST}$
SW1	10		15	A2
SW2	11		14	A1
SW3	12		13	A0

24-Pin Plastic SOP

MSM6652-xxxGS-K, MSM6653-xxxGS-K, MSM6654-xxxGS-K, MSM6655-xxxGS-K, MSM6656-xxxGS-K, MSM6652A-xxxGS-K, MSM6653A-xxxGS-K, MSM6654A-xxxGS-K, MSM6655A-xxxGS-K, MSM6656A-xxxGS-K, MSM6658A-xxxGS-K

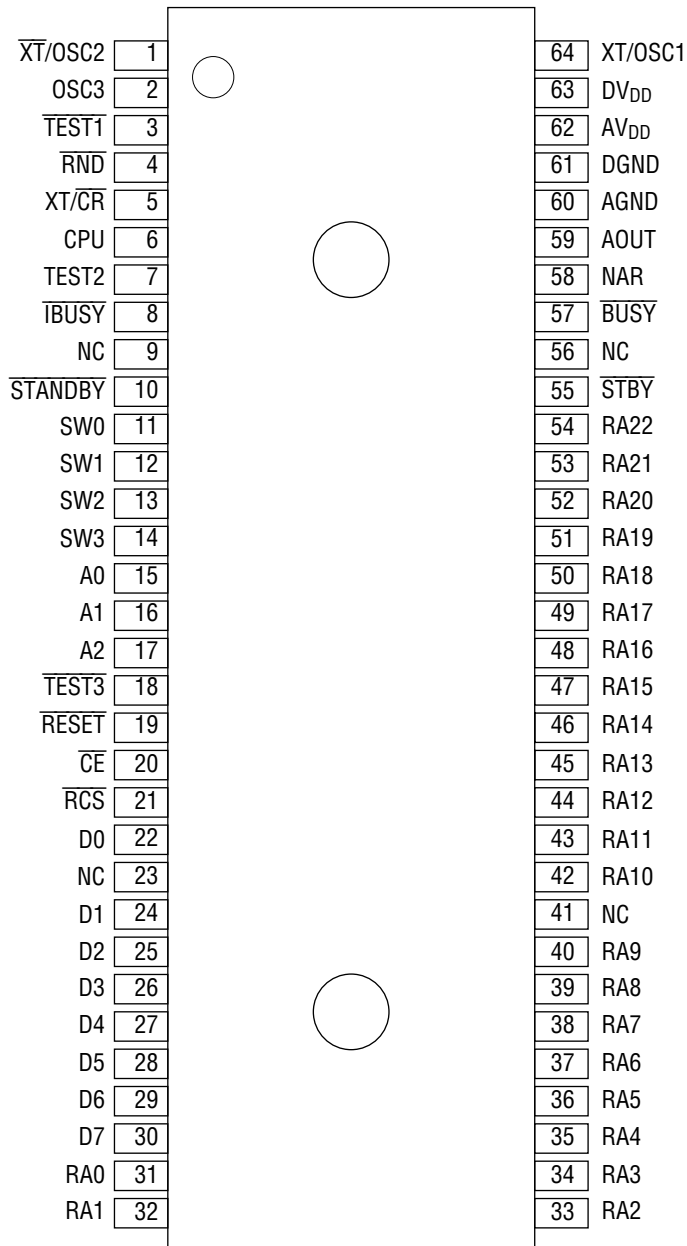MSM66P54-03/-04GS-K
MSM66P56-03/-04GS-K

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MSM6650

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Product name: MSM6650GS-BK

Pin assignments:

Top pins (left to right, 64→52): STBY, RA22, RA21, RA20, RA19, RA18, RA17, RA16, RA15, RA14, RA13, RA12, RA11

Left pins (top to bottom, 1→19):
Pin	Signal
1	NC
2	NC
3	$\overline{\text{BUSY}}$
4	NAR
5	AOUT
6	AGND
7	DGND
8	AV_{DD}
9	DV_{DD}
10	XT/OSC1
11	$\overline{\text{XT}}$/OSC2
12	OSC3
13	$\overline{\text{TEST1}}$
14	$\overline{\text{RND}}$
15	XT/$\overline{\text{CR}}$
16	CPU
17	TEST2
18	$\overline{\text{IBUSY}}$
19	NC

Right pins (top to bottom, 51→33):
Pin	Signal
51	RA10
50	RA9
49	RA8
48	RA7
47	RA6
46	RA5
45	RA4
44	RA3
43	RA2
42	RA1
41	RA0
40	D7
39	D6
38	D5
37	D4
36	D3
35	D2
34	D1
33	NC

Bottom pins (left to right, 20→32): $\overline{\text{STANDBY}}$, SW0, SW1, SW2, SW3, A0, A1, A2, $\overline{\text{TEST3}}$, $\overline{\text{RESET}}$, $\overline{\text{CE}}$, $\overline{\text{RCS}}$, D0

NC : No connection

64-Pin Plastic QFP

Product name: MSM6650SS

$\overline{XT}$/OSC2	1		64	XT/OSC1
OSC3	2		63	DV_{DD}
$\overline{TEST1}$	3		62	AV_{DD}
$\overline{RND}$	4		61	DGND
XT/$\overline{CR}$	5		60	AGND
CPU	6		59	AOUT
TEST2	7		58	NAR
$\overline{IBUSY}$	8		57	$\overline{BUSY}$
NC	9		56	NC
$\overline{STANDBY}$	10		55	$\overline{STBY}$
SW0	11		54	RA22
SW1	12		53	RA21
SW2	13		52	RA20
SW3	14		51	RA19
A0	15		50	RA18
A1	16		49	RA17
A2	17		48	RA16
$\overline{TEST3}$	18		47	RA15
$\overline{RESET}$	19		46	RA14
$\overline{CE}$	20		45	RA13
$\overline{RCS}$	21		44	RA12
D0	22		43	RA11
NC	23		42	RA10
D1	24		41	NC
D2	25		40	RA9
D3	26		39	RA8
D4	27		38	RA7
D5	28		37	RA6
D6	29		36	RA5
D7	30		35	RA4
RA0	31		34	RA3
RA1	32		33	RA2

NC : No connection

64-Pin Plastic SDIP

OKI Semiconductor

PIN DESCRIPTIONS

1. MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx
   18-Pin plastic DIP

Pin	Symbol	Type	Description
5	$\overline{\text{RESET}}$	I	**Reset.** Setting this pin to "L" puts the LSI in standby status. At this time, oscillation stops, AOUT is pulled to GND, and the deveice is initialized. This pin has an internal pull-up resistor.
6	$\overline{\text{BUSY}}$	O	**Busy.** This pin outputs a "L" level during playback. At power-on, this pin is at "H" level.
7	XT/$\overline{\text{CR}}$	I	**XT/$\overline{\text{CR}}$ selectable pin.** Set to "H" level when using ceramic oscillation. Set to "L" level when using RC oscillation.
8	AOUT	O	**Sound Output.** This is the synthesized output pin of the internal low-pass filter.
11	OSC1	I	**Oscillator 1.** This pin is a ceramic oscillator connection pin when using ceramic oscillation. This pin is an RC connection pin when using RC oscillation. When using an external clock, use this pin as the clock input.
12	OSC2	O	**Oscillator 2.** This pin is a ceramic oscillator connection pin when using a ceramic oscillator. This is an RC connection pin when using RC oscillation. Leave open if using an external clock. OSC2 outputs a "L" level in standby status.
13	OSC3	O	**Oscillator 3.** Leave open if using a ceramic oscillator. This pin is the RC connection pin when using RC oscillation. When RC oscillation is selected, OSC3 outputs a "H" level in standby status.
14	$\overline{\text{RND}}$	I	**Random Playback.** Random playback starts when the $\overline{\text{RND}}$ pin is set to a "L" level. At the fall of $\overline{\text{RND}}$, addresses from the random address playback circuit inside the IC are fetched. Set to a "H" level if random playback is not used. This pin has an internal pull-up resistor.
15-18	SW0-SW3	I	**Phrase Inputs.** These pins are phrase input pins corresponding to playback. If the input changes, SW0 to SW3 pins capture address data after 16 ms and speech playback commences. These pins have internal pull-down resistors.
1-3	A0-A2	I	**Phrase Inputs.** Phrase input pins correspoding to playback. The A0 input becomes invalid when the random playback function is used.
9	GND	—	**Ground.**
10	V$_{DD}$	—	**Power supply.** Insert a 0.1μF or more bypass capacitor between this pin and GND.
4	$\overline{\text{TEST}}$	I	**Test Mode.** Set to "H" level. This pin has an internal pull-up resistor.

2. MSM66P54-xx, MSM66P56-xx
   20-Pin plastic DIP

Pin	Symbol	Type	Description
6	$\overline{RESET}$	I	**Reset.** Setting this pin to "L" puts the LSI in standby status. At this time, oscillation stops, AOUT is pulled to GND, and the deveice is initialized. This pin has an internal pull-up resistor.
7	$\overline{BUSY}$	O	**Busy.** This pin outputs a "L" level during playback. At power-on, this pin is at "H" level.
8	XT/$\overline{CR}$	I	**XT/$\overline{CR}$ selectable pin.** Set to "H" level when using ceramic oscillation. Set to "L" level when using RC oscillation.
9	AOUT	O	**Sound Output.** This is the synthesized output pin of the internal low-pass filter.
12	OSC1	I	**Oscillator 1.** This pin is a ceramic oscillator connection pin when using ceramic oscillation. This pin is an RC connection pin when using RC oscillation. When using an external clock, use this pin as the clock input.
13	OSC2	O	**Oscillator 2.** This pin is a ceramic oscillator connection pin when using a ceramic oscillator. This is an RC connection pin when using RC oscillation. Leave open if using an external clock. OSC2 outputs a "L" level in standby status.
14	OSC3	O	**Oscillator 3.** Leave open if using a ceramic oscillator. This pin is the RC connection pin when using RC oscillation. When RC oscillation is selected, OSC3 outputs a "H" level in standby status.
15	$\overline{RND}$	I	**Random Playback.** Random playback starts when the $\overline{RND}$ pin is set to a "L" level. At the fall of $\overline{RND}$, addresses from the random address playback circuit inside the IC are fetched. Set to a "H" level if random playback is not used. This pin has an internal pull-up resistor.
16-19	SW0-SW3	I	**Phrase Inputs.** These pins are phrase input pins corresponding to playback. If the input changes, SW0 to SW3 pins capture address data after 16 ms and speech playback commences. These pins have internal pull-down resistors.
2-4	A0-A2	I	**Phrase Inputs.** Phrase input pins correspoding to playback. The A0 input becomes invalid when the random playback function is used.
10	GND	—	**Ground.**
11	V$_{DD}$	—	**Power supply.** Insert a 0.1μF or more bypass capacitor between this pin and GND.
5	$\overline{TEST}$	I	**Test Mode.** Set to "H" level. This pin has an internal pull-up resistor.
1	V$_{PP}$	—	Power supply used when writing data to internal OTP ROM. Leave open or set to "H" level during playback.
20	$\overline{PGM}$	I	Interface with voice analysis edit tool AR203 or AR204. Set to "L" level or leave open during playback.

3. MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54-xx,
   MSM66P56-xx
   24-Pin plastic SOP

Pin	Symbol	Type	Description
17	$\overline{\text{RESET}}$	I	**Reset.** Setting this pin to "L" puts the LSI in standby status. At this time, oscillation stops, AOUT is pulled to GND, and the deveice is initialized. This pin has an internal pull-up resistor.
20	$\overline{\text{BUSY}}$	O	**Busy.** This pin outputs a "L" level during playback. At power-on, this pin is at "H" level.
22	XT/$\overline{\text{CR}}$	I	**XT/$\overline{\text{CR}}$ selectable pin.** Set to "H" level when using ceramic oscillation. Set to "L" level when using RC oscillation.
23	AOUT	O	**Sound Output.** This is the synthesized output pin of the internal low-pass filter.
2	OSC1	I	**Oscillator 1.** This pin is a ceramic oscillator connection pin when using ceramic oscillation. This pin is an RC connection pin when using RC oscillation. When using an external clock, use this pin as the clock input.
3	OSC2	O	**Oscillator 2.** This pin is a ceramic oscillator connection pin when using a ceramic oscillator. This is an RC connection pin when using RC oscillation. Leave open if using an external clock. OSC2 outputs a "L" level in standby status.
5	OSC3	O	**Oscillator 3.** Leave open if using a ceramic oscillator. This pin is the RC connection pin when using RC oscillation. When RC oscillation is selected, OSC3 outputs a "H" level in standby status.
8	$\overline{\text{RND}}$	I	**Random Playback.** Random playback starts when the $\overline{\text{RND}}$ pin is set to a "L" level. At the fall of $\overline{\text{RND}}$, addresses from the random address playback circuit inside the IC are fetched. Set to a "H" level if random playback is not used. This pin has an internal pull-up resistor.
9-12	SW0-SW3	I	**Phrase Inputs.** These pins are phrase input pins corresponding to playback. If the input changes, SW0 to SW3 pins capture address data after 16 ms and speech playback commences. These pins have internal pull-down resistors.
13-15	A0-A2	I	**Phrase Inputs.** Phrase input pins correspoding to playback. The A0 input becomes invalid when the random playback function is used.
24	GND	—	**Ground.**
1	V$_{\text{DD}}$	—	**Power supply.** Insert a 0.1μF or more bypass capacitor between this pin and GND.
16	$\overline{\text{TEST}}$	I	**Test Mode.** Set to "H" level. This pin has an internal pull-up resistor.
18	V$_{\text{PP}}$*	—	Power supply used when writing data to internal OTP ROM. Leave open or set to "H" level during playback.
7	$\overline{\text{PGM}}$*	I	Interface with voice analysis edit tool AR203 or AR204. Set to "L" level or leave open during playback.

* Pins for MSM66P54/56-xx only

4. MSM6650
 64-Pin plastic QFP (64-Pin plastic SDIP)

Pin	Symbol	Type	Description
29(19)	$\overline{\text{RESET}}$	I	**Reset.** Setting this pin to "L" puts the LSI in standby status. At this time, oscillation stops, AOUT is pulled to GND, and the deveice is initialized. This pin has an internal pull-up resistor.
3(57)	$\overline{\text{BUSY}}$	O	**Busy.** This pin outputs a "L" level during playback. At power-on, this pin is at "H" level.
15(5)	XT/$\overline{\text{CR}}$	I	**XT/$\overline{\text{CR}}$ selectable pin.** Set to "H" level when using ceramic oscillation. Set to "L" level when using RC oscillation.
5 (59)	AOUT	O	**Sound Output.** This is the synthesized output pin of the internal low-pass filter.
10(64)	XT/OSC1	I	**Oscillator 1.** This pin is a ceramic oscillator connection pin when using ceramic oscillation. This pin is an RC connection pin when using RC oscillation. When using an external clock, use this pin as the clock input.
11(1)	$\overline{\text{XT}}$/OSC2	O	**Oscillator 2.** This pin is a ceramic oscillator connection pin when using a ceramic oscillator. This is an RC connection pin when using RC oscillation. Leave open if using an external clock. OSC2 outputs a "L" level in standby status.
12(2)	OSC3	O	**Oscillator 3.** Leave open if using a ceramic oscillator. This pin is the RC connection pin when using RC oscillation. When RC oscillation is selected, OSC3 outputs a "H" level in standby status.
14(4)	$\overline{\text{RND}}$	I	**Random Playback.** Random playback starts when the $\overline{\text{RND}}$ pin is set to a "L" level. At the fall of $\overline{\text{RND}}$, addresses from the random address playback circuit inside the IC are fetched. Set to a "H" level if random playback is not used. This pin has an internal pull-up resistor.
21-24 (11-14)	SW0-SW3	I	**Phrase Inputs.** These pins are phrase input pins corresponding to playback. If the input changes, SW0 to SW3 pins capture address data after 16 ms and speech playback commences. These pins have internal pull-down resistors.
25-27 (15-17)	A0-A2	I	**Phrase Inputs.** Phrase input pins correspoding to playback. The A0 input becomes invalid when the random playback function is used.

Pin	Symbol	Type	Description
6 (60)	AGND	—	Analog ground pin.
7 (61)	DGND	—	Digital ground pin.
8 (62)	AV$_{DD}$	—	Analog power pin. Insert a 0.1 μF or more bypass capacitor in between this pin and AGND.
9 (63)	DV$_{DD}$	—	Digiral power pin. Insert a 0.1 μF or more bypass capacitor in between this pin and DGND.
16 (6)	CPU	I	**CPU Mode.** Set to "L" level to select Standalone Mode. Set to "H" level to select Microcontroller Interface Mode.
13, 28 (3, 18)	$\overline{TEST1}$, $\overline{3}$	I	**Test.** Set these pins to "H" level. The $\overline{TEST1}$ and $\overline{TEST3}$ pins have internal pull-up resistor.
17 (7)	TEST2	I	**Test.** Set this pin to "L" level.
18 (8)	$\overline{IBUSY}$	O	**I Busy.** Outputs a "L" level during voice playback (except during standby conversion time), or when the AOUT pin is at half V$_{DD}$ level.
20 (10)	$\overline{STANDBY}$	O	**Standby Indicator.** This output pin remains at "L" level during oscillation.
30 (20)	$\overline{CE}$	O	**Chip Enable.** $\overline{CE}$ is a timing output pin to control read of external memory. This pin outputs when $\overline{RCS}$ is at the "L" level. This pin goes high impedance when $\overline{RCS}$ is at the "H" level.
31 (21)	$\overline{RCS}$	I	**Read Chip Select.** The data bits D0-D7 are internally pulled down when $\overline{RCS}$ is high. Addresses and $\overline{CE}$ are output when $\overline{RCS}$ is at "L" level. The RA22-RA0 address pins and $\overline{CE}$ pin become high impedance.
32, 34-40 (22, 24-30)	D0-D7	I	**External Memory Data Bus.** Data is input when $\overline{RCS}$ is low. When $\overline{RCS}$ is high, these pins become low due to internal pull-down resistors.
41-63 (31-40, 42-54)	RA0-RA22	O	**External Memory Address.** These are address pins for an external memory output when $\overline{RCS}$ is low. These pins become high impedance status if $\overline{RCS}$ is in "H" level.
64 (55)	$\overline{STBY}$	I	**Standby Contorl.** If set to "L" level, the MSM6650 enters standby mode 0.2 seconds after voice ends. If set to "H" level, the MSM6650 AOUT output maintains half V$_{DD}$ after voice ends.

ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	MSM6652-56, MSM6650, MSM6652A-56A	2.4 to 5.5			V
	V_{DD}	MSM6658A, MSM66P54/P56	3.5 to 5.5			V
Operating temperature	T_{op}	—	−40 to +85			°C
Master clock frequency 1	f_{OSC1}	When crystal selected	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Master clock frequency 2	f_{OSC2}	When RC selected (*)	200	256	300	kHz

*   If RC oscillation is selected, 32kHz sampling frequency cannot be selected.

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ELECTRICAL CHARACTERISTICS

DC Characteristics

$(V_{DD}=4.5$ to 5.5 V, GND=0 V, Ta=-40 to $+85°$C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.84 \times V_{DD}$	—	—	V
"L" input voltage	V_{IL}	—	—	—	$0.17 \times V_{DD}$	V
"H" output voltage	V_{OH}	$I_{OH}=-1$ mA	4.6	—	—	V
"L" output voltage	V_{OL}	$I_{OL}=2$ mA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH}=V_{DD}$	—	—	10	μA
"H" input current 2	I_{IH2}	Internal pull-down resistance	30	90	200	μA
"L" input current 1	I_{IL1}	$V_{IL}=$GND	-10	—	—	μA
"L" input current 2 (note)	I_{IL2}	Internal pull-up resistance	-200	-90	-30	μA
Operating power consumption	I_{DD}	$f_{OSC}=4.096$ MHz, No load	—	6	10	mA
Standby power consumption	I_{DS}	Ta=$-40°$C to $+50°$C	—	—	10	μA
		Ta=$-40°$C to $+85°$C	—	—	30	μA

DC Characteristics

$(V_{DD}=2.4$ to 3.6 V, GND=0 V, Ta=-40 to $+85°$C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.84 \times V_{DD}$	—	—	V
"L" input voltage	V_{IL}	—	—	—	$0.17 \times V_{DD}$	V
"H" output voltage	V_{OH}	$I_{OH}=-1$ mA	2.6	—	—	V
"L" output voltage	V_{OL}	$I_{OL}=2$ mA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH}=V_{DD}$	—	—	10	μA
"H" input current 2	I_{IH2}	Internal pull-down resistance	10	30	100	μA
"L" input current 1	I_{IL1}	$V_{IL}=$GND	-10	—	—	μA
"L" input current 2	I_{IL2}	Internal pull-up resistance	-100	-30	-10	μA
Operating power consumiption	I_{DD}	$f_{OSC}=4.096$ MHz, No load	—	4	7	mA
Standby power consumption	I_{DS}	Ta=$-40°$C to $+50°$C	—	—	5	μA
		Ta=$-40°$C to $+85°$C	—	—	20	μA
LPF driving resistance	R_{AOUT}	When LPF output is selected	50	—	—	kΩ
LPF output impedance	R_{LPF}	$I_F=100$ μA	—	1	3	kΩ

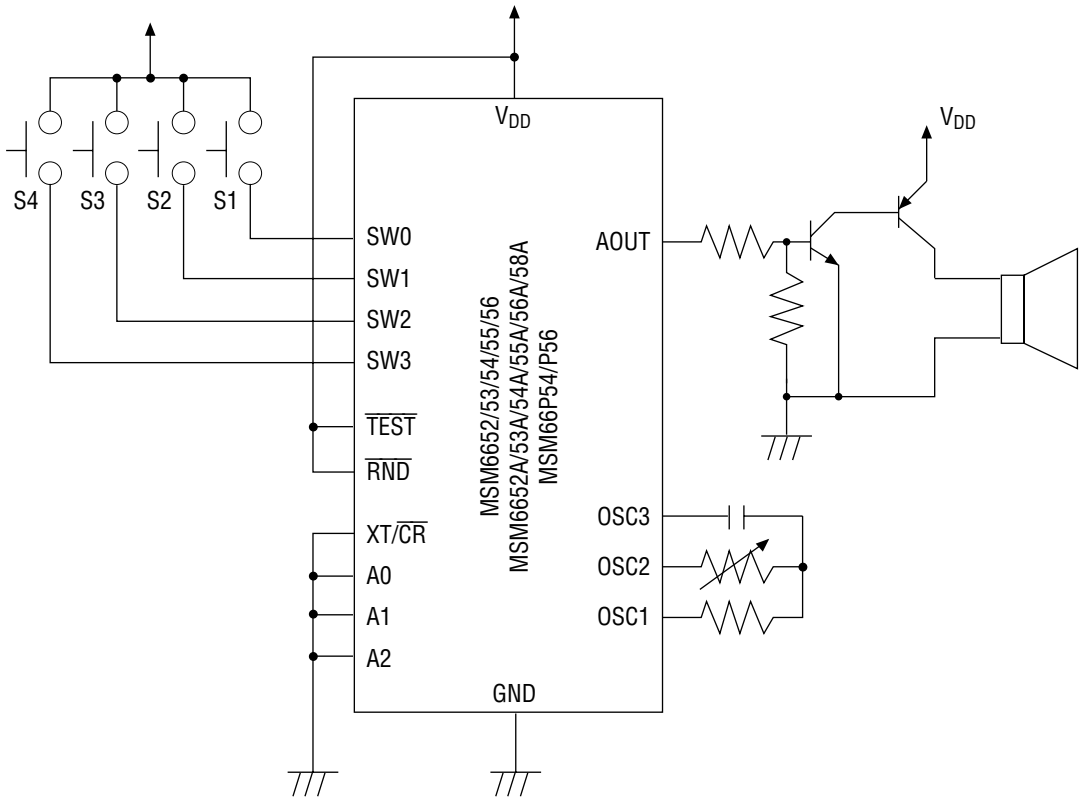## APPLICATION CIRCUITS

(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54/P56-xx)

MSM6652/53/54/55/56
MSM6652A/53A/54A/55A/56A/58A
MSM66P54/P56

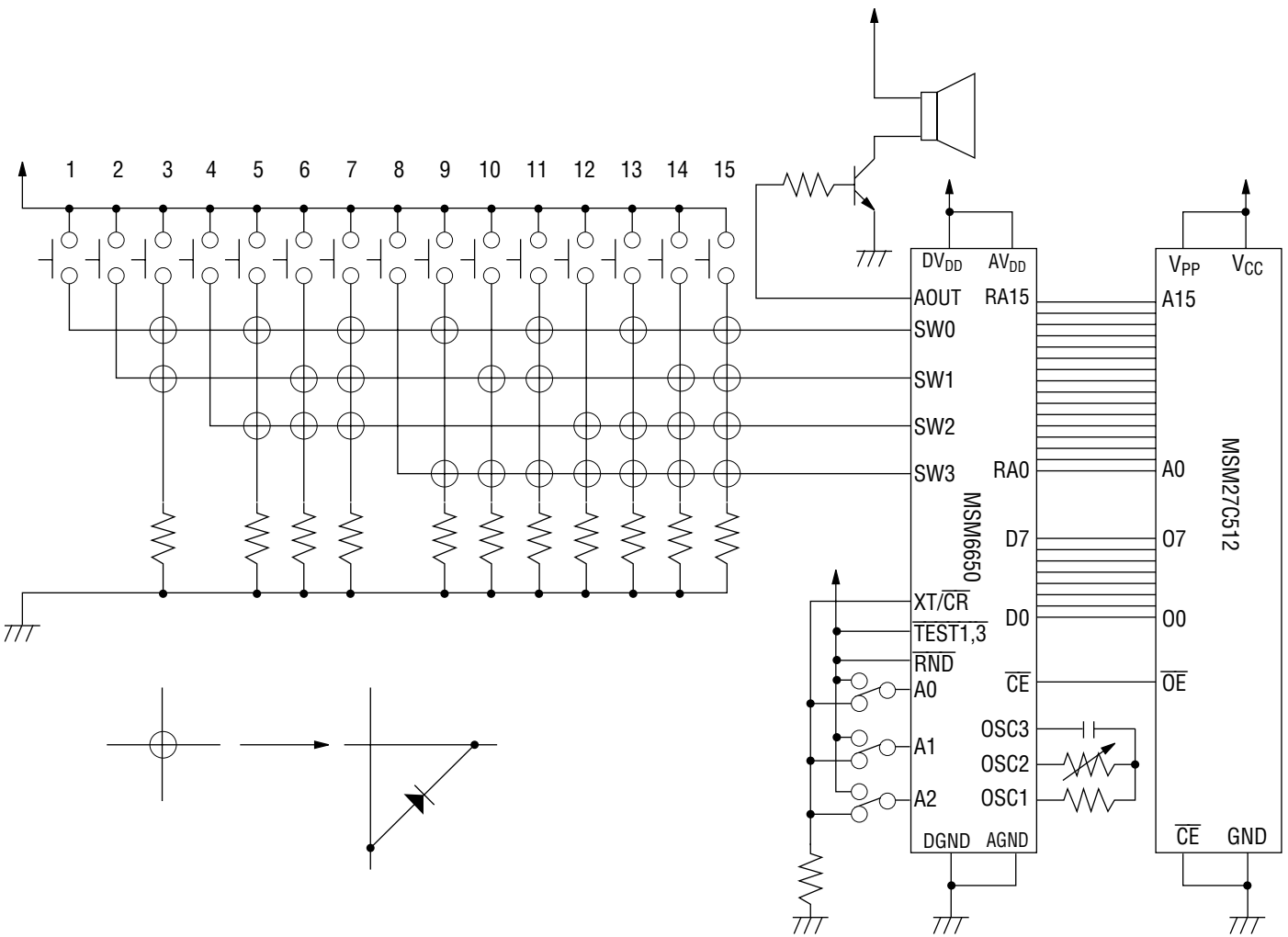Application Circuit in Standalone Mode Supporting 15 Switch-Selected Phrases
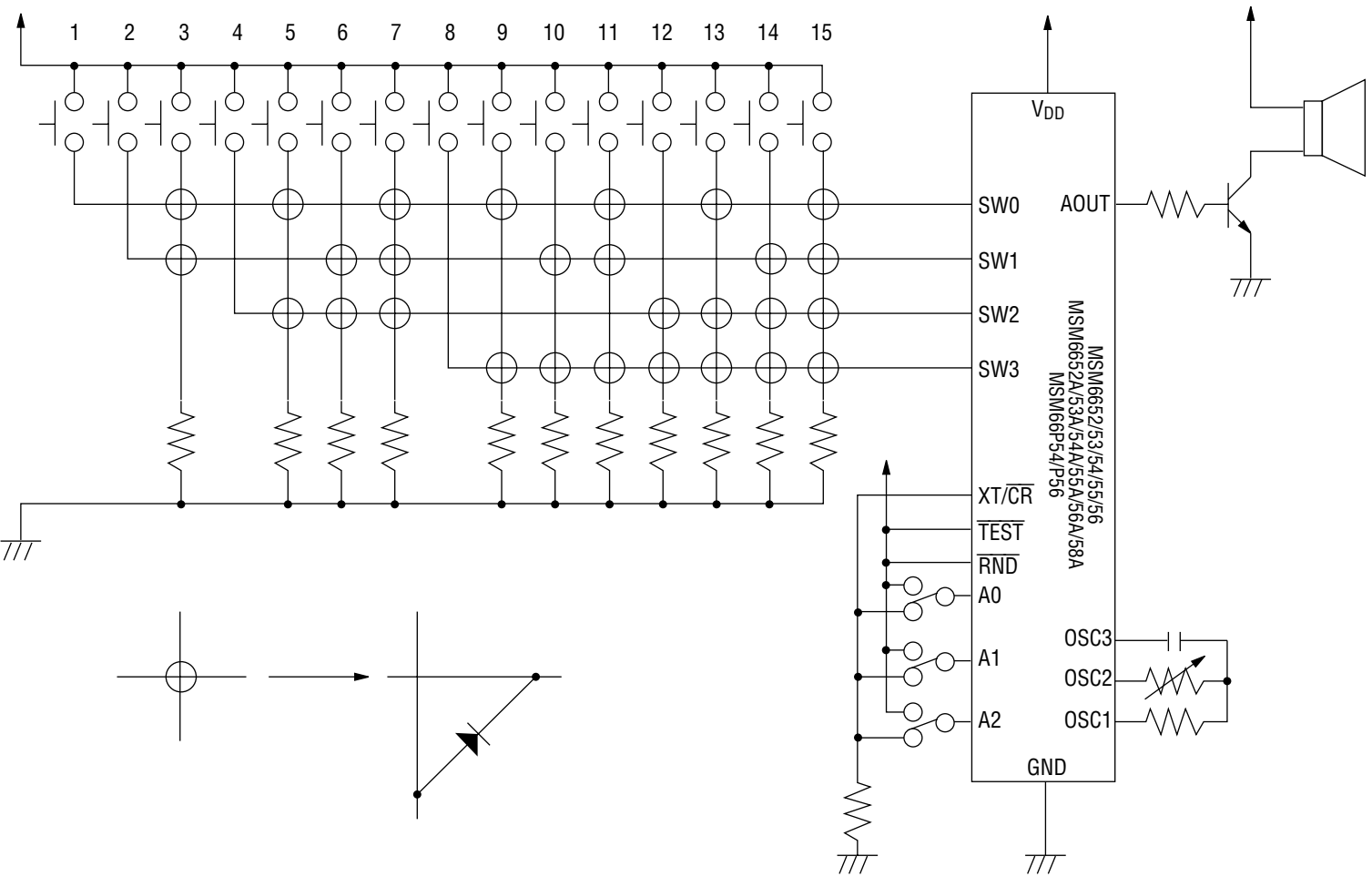
(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54/P56-xx)
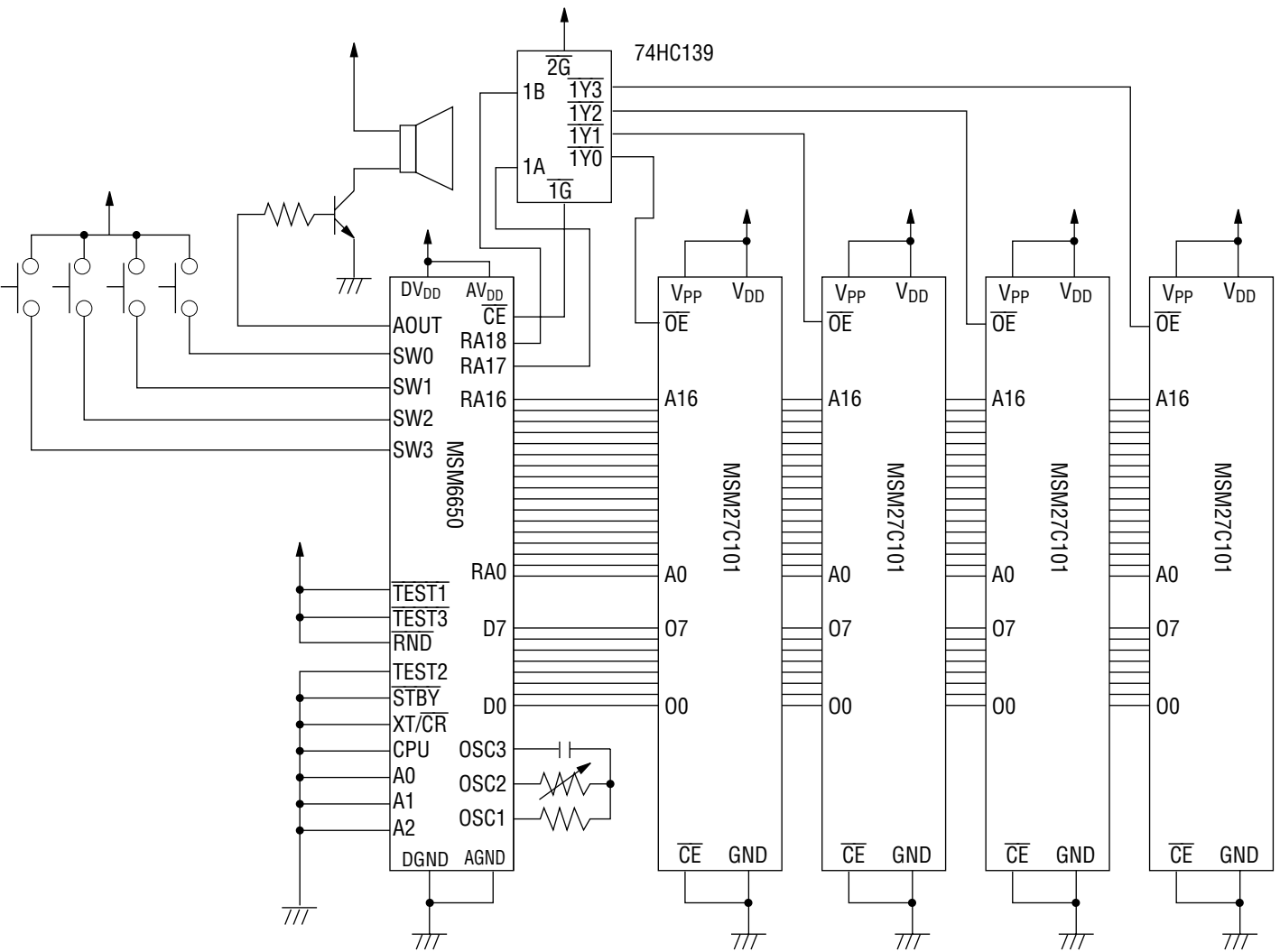

Application Circuit in Standalone Mode Supporting Four Switch-Selected Words

Switches and Playback Addresses

	A2	A1	A0	SW3	SW2	SW1	SW0	ADR
S1	0	0	0	0	0	0	1	01
S2	0	0	0	0	0	1	0	02
S3	0	0	0	0	1	0	0	04
S4	0	0	0	1	0	0	0	08

Application Circuit in Standalone Mode Supporting 15 Switch-Selected Phrases

(MSM6650)

Application Circuit in Standalone Mode Supporting Four 1-Mbit EPROMs

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MICROCONTROLLER INTERFACE MODE

FEATURES

Device name	Data ROM size	Maximum playback time (sec)				
		f_{SAM}=4.0 kHz	f_{SAM}=6.4 kHz	f_{SAM}=8.0 kHz	f_{SAM}=16 kHz	f_{SAM}=32 kHz
MSM6652, 6652A	288 Kbits	16.9	10.5	8.4	4.2	2.1
MSM6653, 6653A	544 Kbits	31.2	19.5	15.6	7.8	3.9
MSM6654, 6654A	1 Mbit	63.8	39.9	31.9	15.9	7.9
MSM6655, 6655A	1.5 Mbits	96.5	60.3	48.2	24.1	12.0
MSM6656, 6656A	2 Mbits	129.1	80.7	64.5	32.2	16.1
MSM6658A	4 Mbits	259.7	162.9	129.8	64.9	32.4
MSM66P54	1 Mbit	63.8	39.9	31.9	15.9	7.9
MSM66P56	2 Mbit	129.1	80.7	64.5	32.2	16.1
MSM6650	64 Mbits (Max)	4194.3	2620.5	2096.4	1048.2	524.1

Note: Actual voice ROM area is smaller by 22 Kbits.

- 4-bit ADPCM or 8-bit PCM sound generation
- Melody function
- Edit ROM function
- Two-channel mixing function
- Fade-out function via four-step sound volume attenuation
- Serial input or parallel input selectable
- Built-in beep tone of 0.5 kHz, 1.0 kHz, 1.3 kHz, or 2.0 kHz selectable with a specific code
- Sampling frequency of 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz, 10.6 kHz, 12.8 kHz, 16.0 kHz, or 32.0 kHz (32 kHz sampling is not possible when using RC oscillation)
- Up to 127 phrases
- Built-in 12-bit D/A converter
- Built-in –40 dB/octave low-pass filter
- Standby function
- Package options:
  18-pin plastic DIP (DIP18-P-300-2.54)   (Product name: MSM6652-xxxRS/MSM6653-xxxRS/
                                                          MSM6654-xxxRS/MSM6655-xxxRS/
                                                          MSM6656-xxxRS/MSM6652A-xxxRS/
                                                          MSM6653A-xxxRS/MSM6654A-xxxRS/
                                                          MSM6655A-xxxRS/MSM6656A-xxxRS/
                                                          MSM6658A-xxxRS)
  24-pin plastic SOP (SOP24-P-430-1.27-K)   (Product name: MSM6652-xxxGS-K/MSM6653-xxxGS-K/
                                                          MSM6654-xxxGS-K/MSM6655-xxxGS-K/
                                                          MSM6656-xxxGS-K/MSM6652A-xxxGS-K/
                                                          MSM6653A-xxxGS-K/MSM6654A-xxxGS-K/
                                                          MSM6655A-xxxGS-K/MSM6656A-xxxGS-K/
                                                          MSM6658A-xxxGS-K/MSM66P54-01GS-K/
                                                          MSM66P54-02GS-K/MSM66P56-01GS-K/
                                                          MSM66P56-02GS-K)
  20-pin plastic DIP (DIP20-P-300-2.54-W1) (Product name: MSM66P54-01RS/MSM66P54-02RS/
                                                          MSM66P56-01RS/MSM66P56-02RS)
  64-pin plastic QFP (QFP64-P-1420-1.00-BK)(Product name: MSM6650GS-BK)
  64-pin plastic SDIP (SDIP64-P-750-1.778)   (Product name: MSM6650SS)
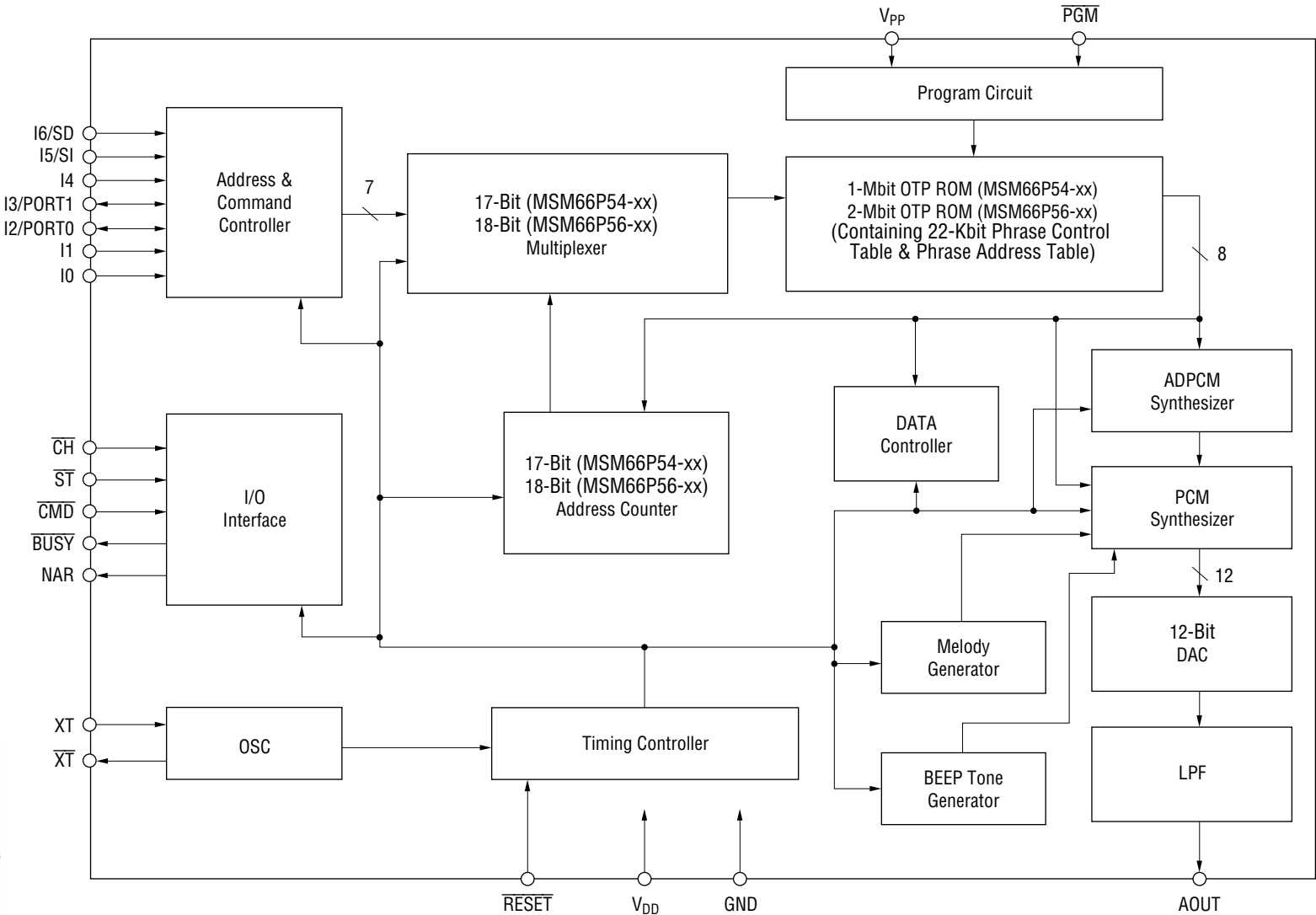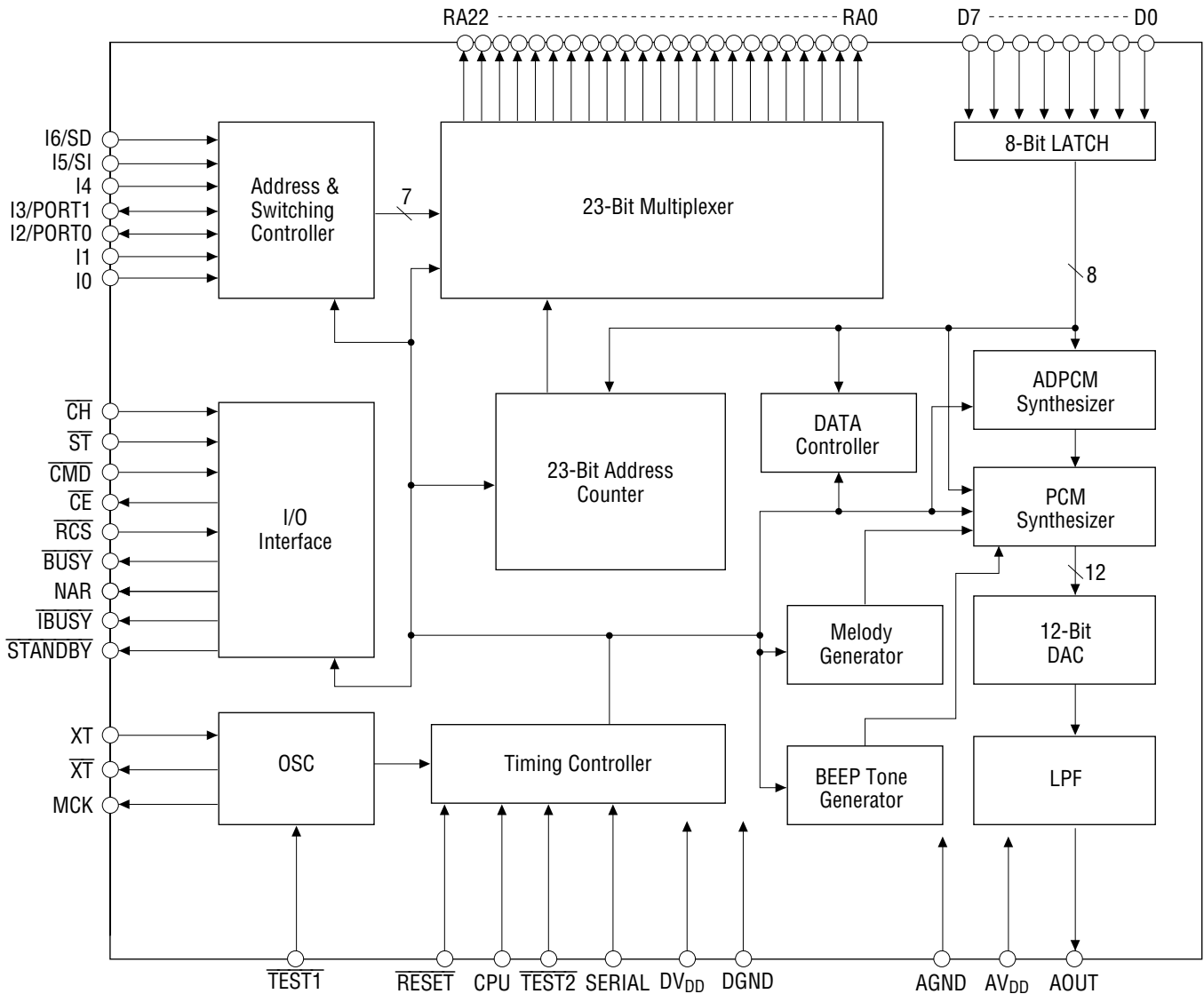
BLOCK DIAGRAMS

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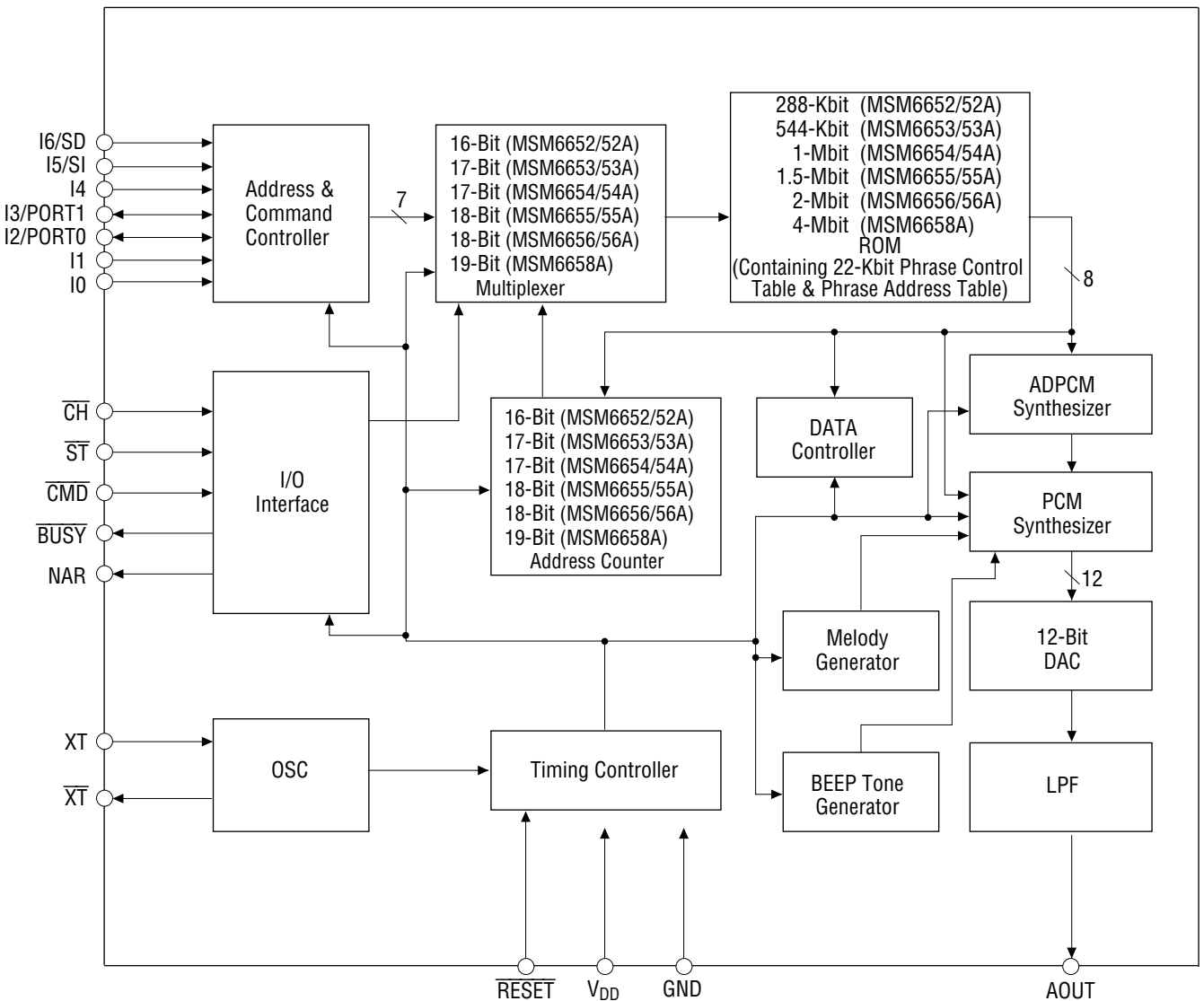
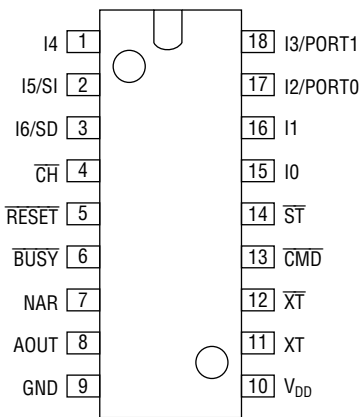## PIN CONFIGURATION (TOP VIEW)

The MSM66P54/P56-xx has two more pins than the MSM6652-6658A while their pin configurations are identical.
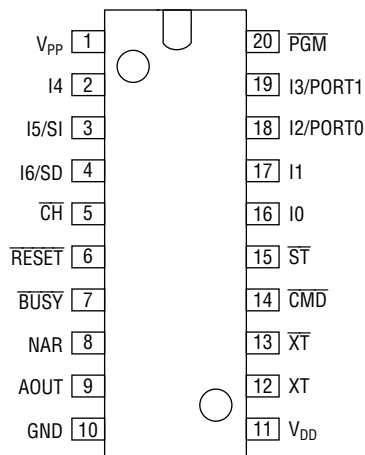
The additional two pins (V_{PP}, $\overline{PGM}$) of the MSM66P54/P56-xx may be open at playback after completion of writing.

MSM6652-6658A (Mask ROM)

I4	1	18	I3/PORT1
I5/SI	2	17	I2/PORT0
I6/SD	3	16	I1
$\overline{CH}$	4	15	I0
$\overline{RESET}$	5	14	$\overline{ST}$
$\overline{BUSY}$	6	13	$\overline{CMD}$
NAR	7	12	$\overline{XT}$
AOUT	8	11	XT
GND	9	10	V_{DD}

18-Pin Plastic DIP

MSM66P54/P56 (OTP)

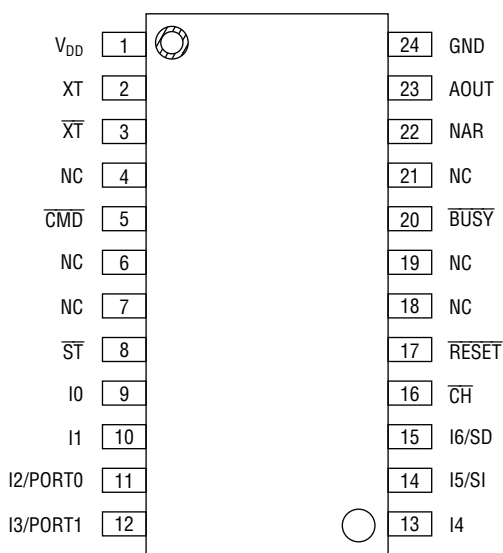|			
V_{PP}	1	20	$\overline{PGM}$
I4	2	19	I3/PORT1
I5/SI	3	18	I2/PORT0
I6/SD	4	17	I1
$\overline{CH}$	5	16	I0
$\overline{RESET}$	6	15	$\overline{ST}$
$\overline{BUSY}$	7	14	$\overline{CMD}$
NAR	8	13	$\overline{XT}$
AOUT	9	12	XT
GND	10	11	V_{DD}

20-Pin Plastic DIP

MSM6652-xxxRS, MSM6653-xxxRS, MSM6654-xxxRS, MSM6655-xxxRS, MSM6656-xxxRS, MSM6652A-xxxRS, MSM6653A-xxxRS, MSM6654A-xxxRS, MSM6655A-xxxRS, MSM6656A-xxxRS, MSM6658A-xxxRS
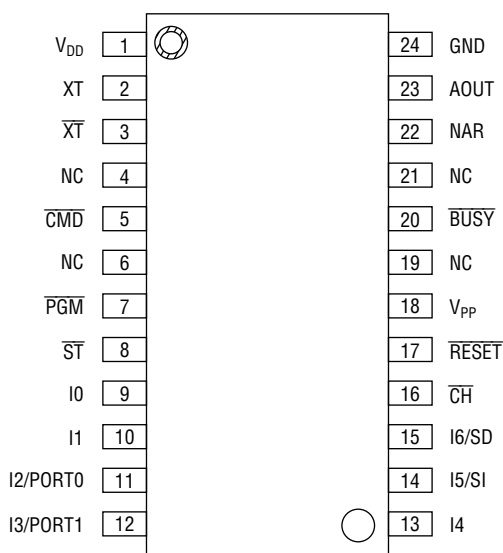
MSM66P54-01/-02RS
MSM66P56-01/-02RS

MSM6652-6658A (Mask ROM)

V_{DD}	1	24	GND
XT	2	23	AOUT
$\overline{XT}$	3	22	NAR
NC	4	21	NC
$\overline{CMD}$	5	20	$\overline{BUSY}$
NC	6	19	NC
NC	7	18	NC
$\overline{ST}$	8	17	$\overline{RESET}$
I0	9	16	$\overline{CH}$
I1	10	15	I6/SD
I2/PORT0	11	14	I5/SI
I3/PORT1	12	13	I4

24-Pin Plastic SOP

MSM66P54/P56 (OTP)

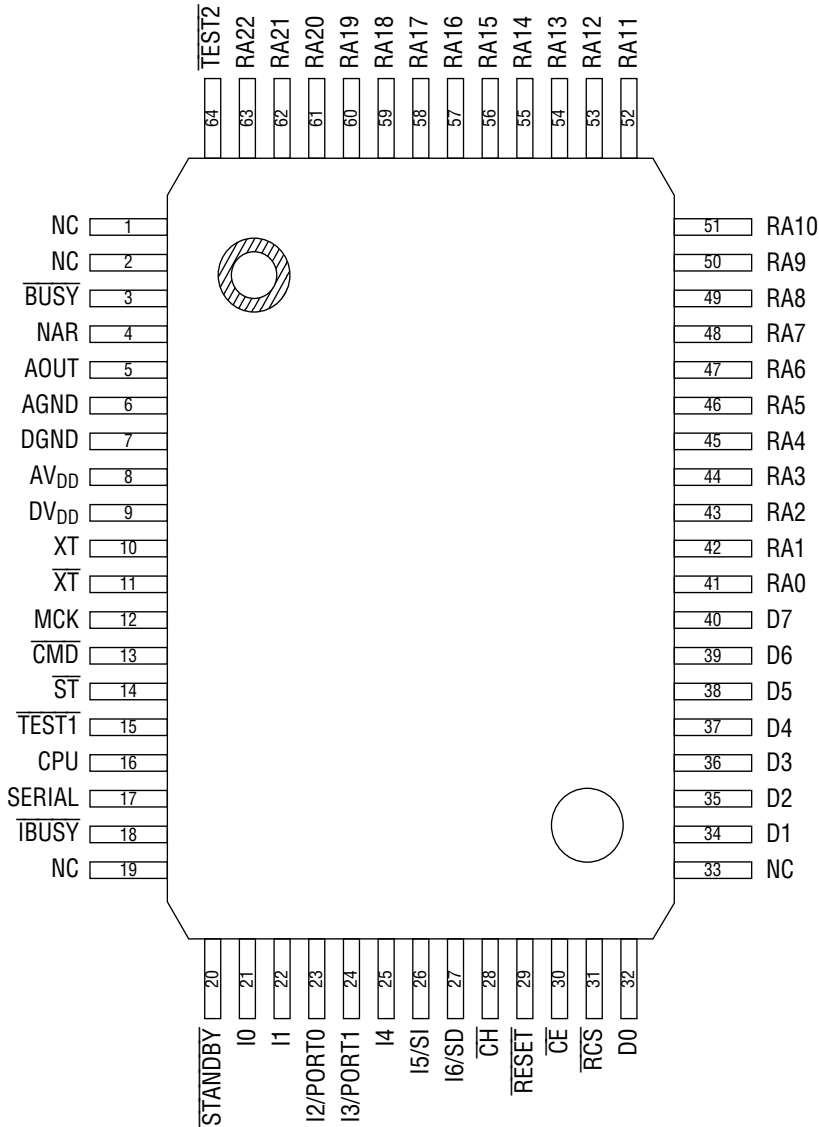|			
V_{DD}	1	24	GND
XT	2	23	AOUT
$\overline{XT}$	3	22	NAR
NC	4	21	NC
$\overline{CMD}$	5	20	$\overline{BUSY}$
NC	6	19	NC
$\overline{PGM}$	7	18	V_{PP}
$\overline{ST}$	8	17	$\overline{RESET}$
I0	9	16	$\overline{CH}$
I1	10	15	I6/SD
I2/PORT0	11	14	I5/SI
I3/PORT1	12	13	I4

24-Pin Plastic SOP

MSM6652-xxxGS-K, MSM6653-xxxGS-K, MSM6654-xxxGS-K, MSM6655-xxxGS-K, MSM6656-xxxGS-K, MSM6652A-xxxGS-K, MSM6653A-xxxGS-K, MSM6654A-xxxGS-K, MSM6655A-xxxGS-K, MSM6656A-xxxGS-K, MSM6658A-xxxGS-K

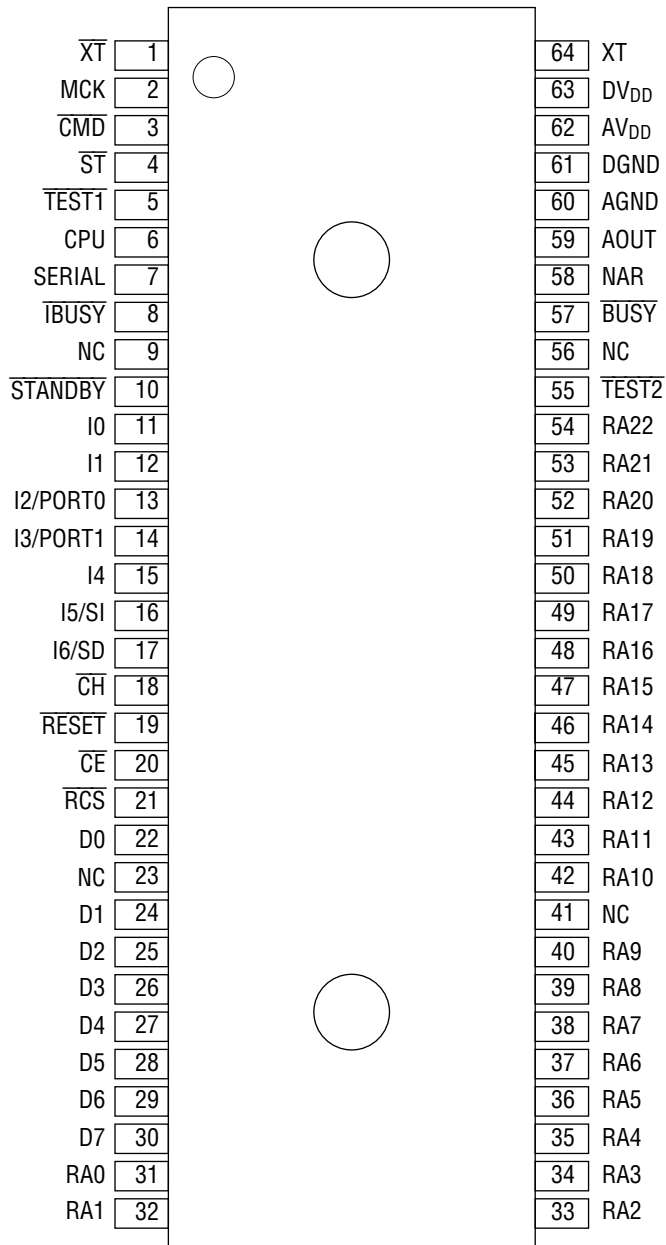MSM66P54-01/-02GS-K
MSM66P56-01/-02GS-K

MSM6650

Product name: MSM6650GS-BK

Pins (top, left to right, 64–52): $\overline{TEST2}$ (64), RA22 (63), RA21 (62), RA20 (61), RA19 (60), RA18 (59), RA17 (58), RA16 (57), RA15 (56), RA14 (55), RA13 (54), RA12 (53), RA11 (52)

Left side (1–19):
Pin	Signal		Pin	Signal
1	NC		51	RA10
2	NC		50	RA9
3	$\overline{BUSY}$		49	RA8
4	NAR		48	RA7
5	AOUT		47	RA6
6	AGND		46	RA5
7	DGND		45	RA4
8	AV_{DD}		44	RA3
9	DV_{DD}		43	RA2
10	XT		42	RA1
11	$\overline{XT}$		41	RA0
12	MCK		40	D7
13	$\overline{CMD}$		39	D6
14	$\overline{ST}$		38	D5
15	$\overline{TEST1}$		37	D4
16	CPU		36	D3
17	SERIAL		35	D2
18	$\overline{IBUSY}$		34	D1
19	NC		33	NC

Bottom pins (20–32): STANDBY (20), I0 (21), I1 (22), I2/PORT0 (23), I3/PORT1 (24), I4 (25), I5/SI (26), I6/SD (27), CH (28), $\overline{RESET}$ (29), $\overline{CE}$ (30), $\overline{RCS}$ (31), D0 (32)

NC : No connection

64-Pin Plastic QFP

Product name: MSM6650SS

$\overline{XT}$	1		64	XT
MCK	2		63	DV_{DD}
$\overline{CMD}$	3		62	AV_{DD}
$\overline{ST}$	4		61	DGND
$\overline{TEST1}$	5		60	AGND
CPU	6		59	AOUT
SERIAL	7		58	NAR
$\overline{IBUSY}$	8		57	$\overline{BUSY}$
NC	9		56	NC
$\overline{STANDBY}$	10		55	$\overline{TEST2}$
I0	11		54	RA22
I1	12		53	RA21
I2/PORT0	13		52	RA20
I3/PORT1	14		51	RA19
I4	15		50	RA18
I5/SI	16		49	RA17
I6/SD	17		48	RA16
$\overline{CH}$	18		47	RA15
$\overline{RESET}$	19		46	RA14
$\overline{CE}$	20		45	RA13
$\overline{RCS}$	21		44	RA12
D0	22		43	RA11
NC	23		42	RA10
D1	24		41	NC
D2	25		40	RA9
D3	26		39	RA8
D4	27		38	RA7
D5	28		37	RA6
D6	29		36	RA5
D7	30		35	RA4
RA0	31		34	RA3
RA1	32		33	RA2

NC : No connection

64-Pin Plastic SDIP

OKI Semiconductor

PIN DESCRIPTIONS

1. MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx
   18-Pin plastic DIP

Pin	Symbol	Type	Description
5	$\overline{\text{RESET}}$	I	**Reset.** The devices enter stanby status when a low level is input to this pin. When RESET, oscillation stops. The AOUT output goes to ground and the IC status is reinitialized. This pin has an internal pull-up resistor.
6	$\overline{\text{BUSY}}$	O	**Busy.** Outputs a "L" level during playback and a "H" level when power is turned ON.
7	NAR	O	The CMD and ST inputs become effective when high. NAR indicates whether the address bus (I0 through I6) is ready to accept another address. When high, it is ready to accept. NAR goes high when power is turned ON.
8	AOUT	O	**Analog Speech Output.** D/A converter output or LPF output is selected by entering the command.
11	XT	I	**Ceramic Oscillator Input.** This pin has an internal 0.5 to 5 MΩ feedback resistor between XT and $\overline{\text{XT}}$. If an external clock is used, this is the clock input pin.
12	$\overline{\text{XT}}$	O	**Ceramic Oscillator Output.** If an external clock is used, leave this pin open.
13	$\overline{\text{CMD}}$	I	**Command Input and Option Control.** This pin is used as command and option input when CMD is at the high level with $\overline{\text{ST}}$ low. If this pin is not used or serial input is optioned, set this pin to "H" level. This pin has an internal pull-up resistor.
14	$\overline{\text{ST}}$	I	**Start.** Speech playback starts at the fall of the $\overline{\text{ST}}$ pulse. The I0 - I6 addresses are latched at the rise of the $\overline{\text{ST}}$ pulse. Input a $\overline{\text{ST}}$ pulse when NAR goes to the high level for channels 1 and 2. This pin has an internal pull-up resistor.
4	$\overline{\text{CH}}$	I	**Channel Control.** Channel 1 is selected when the input is pulled high. Channel 2 is selected when the input is low. This pin has an internal pull-up resistor.
3	I6/SD	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is serial data (command and address) input when serial input is optioned.
2	I5/SI	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is used as serial clock input when serial input is optioned.
1	I4	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
18	I3/PORT1	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
17	I2/PORT0	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
15, 16	I0, I1	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
9	GND	—	**Ground pin.**
10	V_{DD}	—	**Power supply.** Insert a 0.1µF ro more bypass capacitor between this pin and GND.

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2. MSM66P54/P56-xx
20-Pin plastic DIP

Pin	Symbol	Type	Description
6	$\overline{\text{RESET}}$	I	**Reset.** The devices enter stanby status when a low level is input to this pin. When RESET, oscillation stops. The AOUT output goes to ground and the IC status is reinitialized. This pin has an internal pull-up resistor.
7	$\overline{\text{BUSY}}$	O	**Busy.** Outputs a "L" level during playback and a "H" level when power is turned ON.
8	NAR	O	The CMD and ST inputs become effective when high. NAR indicates whether the address bus (I0 through I6) is ready to accept another address. When high, it is ready to accept. NAR goes high when power is turned ON.
9	AOUT	O	**Analog Speech Output.** D/A converter output or LPF output is selected by entering the command.
12	XT	I	**Ceramic Oscillator Input.** This pin has an internal 0.5 to 5 MΩ feedback resistor between XT and $\overline{\text{XT}}$. If an external clock is used, this is the clock input pin.
13	$\overline{\text{XT}}$	O	**Ceramic Oscillator Output.** If an external clock is used, leave this pin open.
14	$\overline{\text{CMD}}$	I	**Command Input and Option Control.** This pin is used as command and option input when CMD is at the high level with $\overline{\text{ST}}$ low. If this pin is not used or serial input is optioned, set this pin to "H" level. This pin has an internal pull-up resistor.
15	$\overline{\text{ST}}$	I	**Start.** Speech playback starts at the fall of the $\overline{\text{ST}}$ pulse. The I0 - I6 addresses are latched at the rise of the $\overline{\text{ST}}$ pulse. Input a $\overline{\text{ST}}$ pulse when NAR goes to the high level for channels 1 and 2. This pin has an internal pull-up resistor.
5	$\overline{\text{CH}}$	I	**Channel Control.** Channel 1 is selected when the input is pulled high. Channel 2 is selected when the input is low. This pin has an internal pull-up resistor.
4	I6/SD	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is serial data (command and address) input when serial input is optioned.
3	I5/SI	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is used as serial clock input when serial input is optioned.
2	I4	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
19	I3/PORT1	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
18	I2/PORT0	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
16, 17	I0, I1	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
10	GND	—	**Ground pin.**
11	V_{DD}	—	**Power supply.** Insert a 0.1μF ro more bypass capacitor between this pin and GND.
1	V_{PP}	—	Supply voltage for writing data to internal OTP ROM.
20	$\overline{\text{PGM}}$	I	Interface with voice analysis edit tools AR203 and AR204. Set to "L" level or leave open during playback. This pin has an internal pull-down resistor.

3. MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54/P56-xx
   24-Pin plastic SOP

Pin	Symbol	Type	Description
17	$\overline{\text{RESET}}$	I	**Reset.** The devices enter stanby status when a low level is input to this pin. When RESET, oscillation stops. The AOUT output goes to ground and the IC status is reinitialized. This pin has an internal pull-up resistor.
20	$\overline{\text{BUSY}}$	O	**Busy.** Outputs a "L" level during playback and a "H" level when power is turned ON.
22	NAR	O	The CMD and ST inputs become effective when high. NAR indicates whether the address bus (I0 through I6) is ready to accept another address. When high, it is ready to accept. NAR goes high when power is turned ON.
23	AOUT	O	**Analog Speech Output.** D/A converter output or LPF output is selected by entering the command.
2	XT	I	**Ceramic Oscillator Input.** This pin has an internal 0.5 to 5 MΩ feedback resistor between XT and $\overline{\text{XT}}$. If an external clock is used, this is the clock input pin.
3	$\overline{\text{XT}}$	O	**Ceramic Oscillator Output.** If an external clock is used, leave this pin open.
5	$\overline{\text{CMD}}$	I	**Command Input and Option Control.** This pin is used as command and option input when CMD is at the high level with $\overline{\text{ST}}$ low. If this pin is not used or serial input is optioned, set this pin to "H" level. This pin has an internal pull-up resistor.
8	$\overline{\text{ST}}$	I	**Start.** Speech playback starts at the fall of the $\overline{\text{ST}}$ pulse. The I0 - I6 addresses are latched at the rise of the $\overline{\text{ST}}$ pulse. Input a $\overline{\text{ST}}$ pulse when NAR goes to the high level for channels 1 and 2. This pin has an internal pull-up resistor.
16	$\overline{\text{CH}}$	I	**Channel Control.** Channel 1 is selected when the input is pulled high. Channel 2 is selected when the input is low. This pin has an internal pull-up resistor.
15	I6/SD	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is serial data (command and address) input when serial input is optioned.
14	I5/SI	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is used as serial clock input when serial input is optioned.
13	I4	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
12	I3/PORT1	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
11	I2/PORT0	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.

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Pin	Symbol	Type	Description
9, 10	I0, I1	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
24	GND	—	**Ground pin.**
1	V_{DD}	—	**Power supply.** Insert a 0.1µF ro more bypass capacitor between this pin and GND.
18	V_{PP}*	—	Supply voltage for writing data to internal OTP ROM.
7	$\overline{PGM}$ *	I	Interface with voice analysis edit tools AR761 and AR762. Set to "L" level or leave open during playback. This pin has an internal pull-down resistor.

*   Pins for MSM66P54/56-xx only

OKI Semiconductor

4. MSM6650
64-Pin plastic QFP (64-Pin plastic SDIP)

Pin	Symbol	Type	Description
29 (19)	$\overline{\text{RESET}}$	I	**Reset.** The devices enter stanby status when a low level is input to this pin. When RESET, oscillation stops. The AOUT output goes to ground and the IC status is reinitalized. This pin has an internal pull-up resistor.
3 (57)	$\overline{\text{BUSY}}$	O	**Busy.** Outputs a "L" level during playback and a "H" level when power is turned ON.
4 (58)	NAR	O	The CMD and ST inputs become effective when high. NAR indicates whether the address bus (I0 through I6) is ready to accept another address. When high, it is ready to accept. NAR goes high when power is turned ON.
5 (59)	AOUT	O	**Analog Speech Output.** D/A converter output or LPF output is selected by entering the command.
10 (64)	XT	I	**Ceramic Oscillator Input.** This pin has an internal 0.5 to 5 MΩ feedback resistor between XT and $\overline{\text{XT}}$. If an external clock is used, this is the clock input pin.
11 (1)	$\overline{\text{XT}}$	O	**Ceramic Oscillator Output.** If an external clock is used, leave this pin open.
13 (3)	$\overline{\text{CMD}}$	I	**Command Input and Option Control.** This pin is used as command and option input when CMD is at the high level with $\overline{\text{ST}}$ low. If this pin is not used or serial input is optioned, set this pin to "H" level. This pin has an internal pull-up resistor.
14 (4)	$\overline{\text{ST}}$	I	**Start.** Speech playback starts at the fall of the $\overline{\text{ST}}$ pulse. The I0 - I6 addresses are latched at the rise of the $\overline{\text{ST}}$ pulse. Input a $\overline{\text{ST}}$ pulse when NAR goes to the high level for channels 1 and 2. This pin has an internal pull-up resistor.
28 (18)	$\overline{\text{CH}}$	I	**Channel Control.** Channel 1 is selected when the input is pulled high. Channel 2 is selected when the input is low. This pin has an internal pull-up resistor.
27 (17)	I6/SD	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is serial data (command and address) input when serial input is optioned.
26 (16)	I5/SI	I	This pin is command and user-defined phrase input when parallel input is optioned. This pin is used as serial clock input when serial input is optioned.
25 (15)	I4	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.
24 (14)	I3/PORT1	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
23 (13)	I2/PORT0	I/O	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, this pin is a port output. The port output is controlled by entering external silence insertion code.
21, 22 (11, 12)	I0, I1	I	This pin is command and user-defined phrase input when parallel input is optioned. When serial input is optioned, set this pin to "L" level. This pin has an internal pull-down resistor.

Pin	Symbol	Type	Description
6 (60)	AGND	—	**Analog ground pin.**
7 (61)	DGND	—	**Digital ground pin.**
8 (62)	AV$_{DD}$	—	**Analog power pin.** Insert a 0.1μF or more bypass capacitor between this pin and AGND.
9 (63)	DV$_{DD}$	—	**Digital power pin.** Insert a 0.1μF or more bypass capacitor between this pin and DGND.
12 (2)	MCK	O	**Main clock output pin.** Use MCK as a connection pin for the MSC1192, etc. When the IC is in standby status, MCK is held high.
16 (6)	CPU	I	**CPU Mode.** Set to "H" level to select Microcontroller Interface Mode.
17 (7)	SERIAL	I	**Serial/Parallel Interface Select.** This input selects either the parallel or the serial input interface. The serial input interface is selected with a high level; the parallel input interface is selected with a low level.
30 (20)	$\overline{CE}$	O	**Chip Enable.** $\overline{CE}$ is a timing output pin to control read of external memory. This pin outputs when $\overline{RCS}$ is at the "L" level. This pin goes high impedance when $\overline{RCS}$ is at the "H" level.
31 (21)	$\overline{RCS}$	I	**Read Chip Select.** The data bits D0-D7 are internally pulled down when $\overline{RCS}$ is high.
32, 34-40 (22, 24-30)	D0 - D7	I	**External Memory Data Bus.** Data is input when RCS is low. When RCS is high, these pins become low due to internal pull-down resistors.
41-63 (31-40, 42-54)	RA0 - RA22	O	**External Memory Address.** These are address pins for an external memory output when $\overline{RCS}$ is low. These pins become high impedance status if $\overline{RCS}$ is in "H" level.
15, 64 (5, 55)	$\overline{TEST1}$, $\overline{2}$	I	**Test.** Set these pins to "H" level.
18 (8)	$\overline{IBUSY}$	O	Outputs a "L" level during playback or when AOUT is at 1/2 V$_{DD}$ (except standby conversion)
20 (10)	$\overline{STANDBY}$	O	Outputs a "L" level during which the device is oscillating.

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ABSOLUTE MAXIMUM RATINGS

(GND=0 V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 to +7.0	V
Input voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	V_{DD}	MSM6652-56, MSM6650, MSM6652A-56A	2.4 to 5.5			V
		MSM6658A, MSM66P54/P56	3.5 to 5.5			V
Operating temperature	T_{op}	—	−40 to +85			°C
Master clock frequency	f_{OSC}	—	**Min.**	**Typ.**	**Max.**	MHz
			3.5	4.096	4.5	

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ELECTRICAL CHARACTERISTICS

DC Characteristics

$(V_{DD}=4.5$ to 5.5 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	—	$0.84 \times V_{DD}$	—	—	V
Low level input voltage	V_{IL}	—	—	—	$0.17 \times V_{DD}$	V
High level output voltage	V_{OH}	I_{OH}=−1 mA	4.6	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
High level input current 1	I_{IH1}	$V_{IH}=V_{DD}$	—	—	10	μA
High level input current 2	I_{IH2}	Internal pull-down resistor	30	90	200	μA
Low level input current 1	I_{IL1}	V_{IL}=GND	−10	—	—	μA
Low level input current 2 *1	I_{IL2}	Internal pull-up resistor	−200	−90	−30	μA
Operating current	I_{DD}	f_{OSC}=4.096 MHz, No load	—	6	10	mA
Standby current	I_{DS}	Ta=−40°C to +50°C	—	—	10	μA
		Ta=−40°C to +85°C	—	—	30	μA
D/A output relative accuracy	$|V_{DAE}|$	When D/A output selected	—	—	40	mV
D/A output impedance	R_{DAO}	When D/A output selected *2	15	25	35	kΩ
		When D/A output selected *3	15	30	45	kΩ
LPF driving resisance	R_{AOUT}	When LPF output selected	50	—	—	kΩ
LPF output impedance	R_{LPF}	I_F=100 μA	—	1	3	kΩ

*1. Applied to $\overline{RESET}$, $\overline{CMD}$, $\overline{ST}$, $\overline{CH}$.
*2. Applied to MSM6652/53/54/55/56, MSM6652A/53A/54A/55A/56A/58A, MSM6650.
*3. Applied to MSM66P54/P56.

### DC Characteristics

$(V_{DD}=2.4$ to 3.6 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	—	$0.84 \times V_{DD}$	—	—	V
Low level input voltage	V_{IL}	—	—	—	$0.17 \times V_{DD}$	V
High level output voltage	V_{OH}	I_{OH}=−1 mA	2.6	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2 mA	—	—	0.4	V
High level input current 1	I_{IH1}	$V_{IH}=V_{DD}$	—	—	10	μA
High level input current 2	I_{IH2}	Internal pull-down resistor	10	30	100	μA
Low level input current 1	I_{IL1}	V_{IL}=GND	−10	—	—	μA
Low level input current 2 (Note)	I_{IL2}	Internal pull-up resistor	−100	−30	−10	μA
Operating current	I_{DD}	f_{OSC}=4.096 MHz, No load	—	4	7	mA
Standby current	I_{DS}	Ta=−40°C to +50°C	—	—	5	μA
		Ta=−40°C to +85°C	—	—	20	μA
D/A output relative accuracy	$|V_{DAE}|$	When D/A output selected	—	—	20	mV
D/A output impedance	R_{DAO}	When D/A output selected	15	25	35	kΩ
LPF driving resistance	R_{AOUT}	When LPF output selected	50	—	—	kΩ
LPF output impedance	R_{LPF}	I_F=100 μA	—	1	3	kΩ

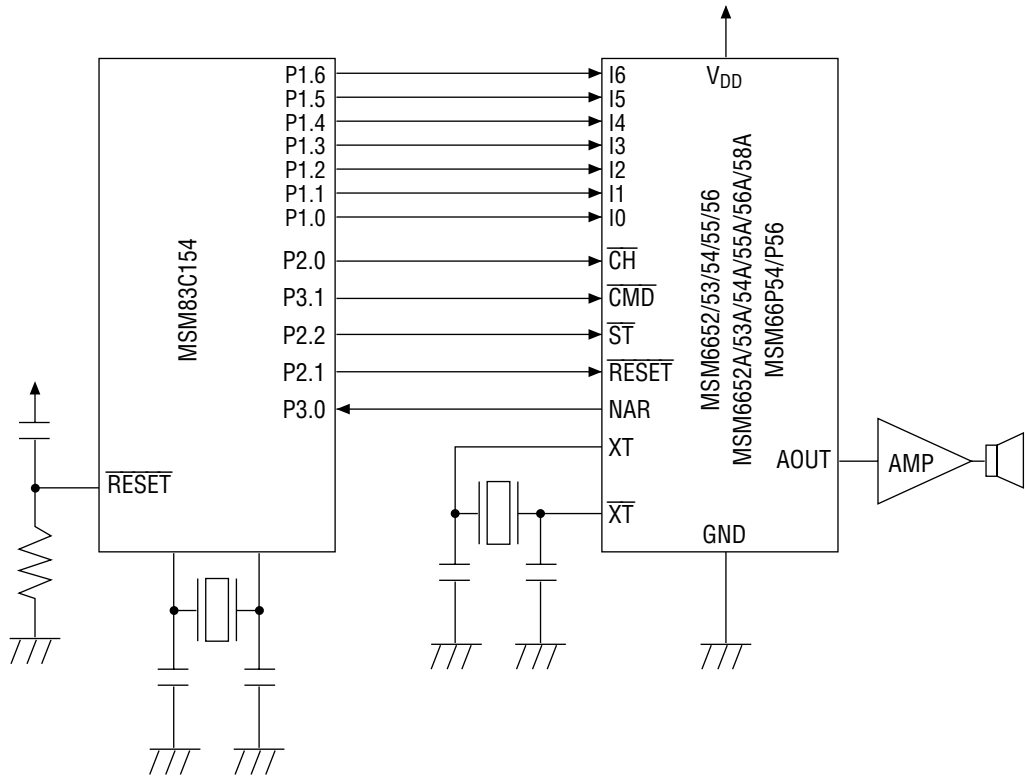Note: Applied to $\overline{RESET}$, $\overline{CMD}$, $\overline{ST}$, $\overline{CH}$.

APPLICATION CIRCUITS

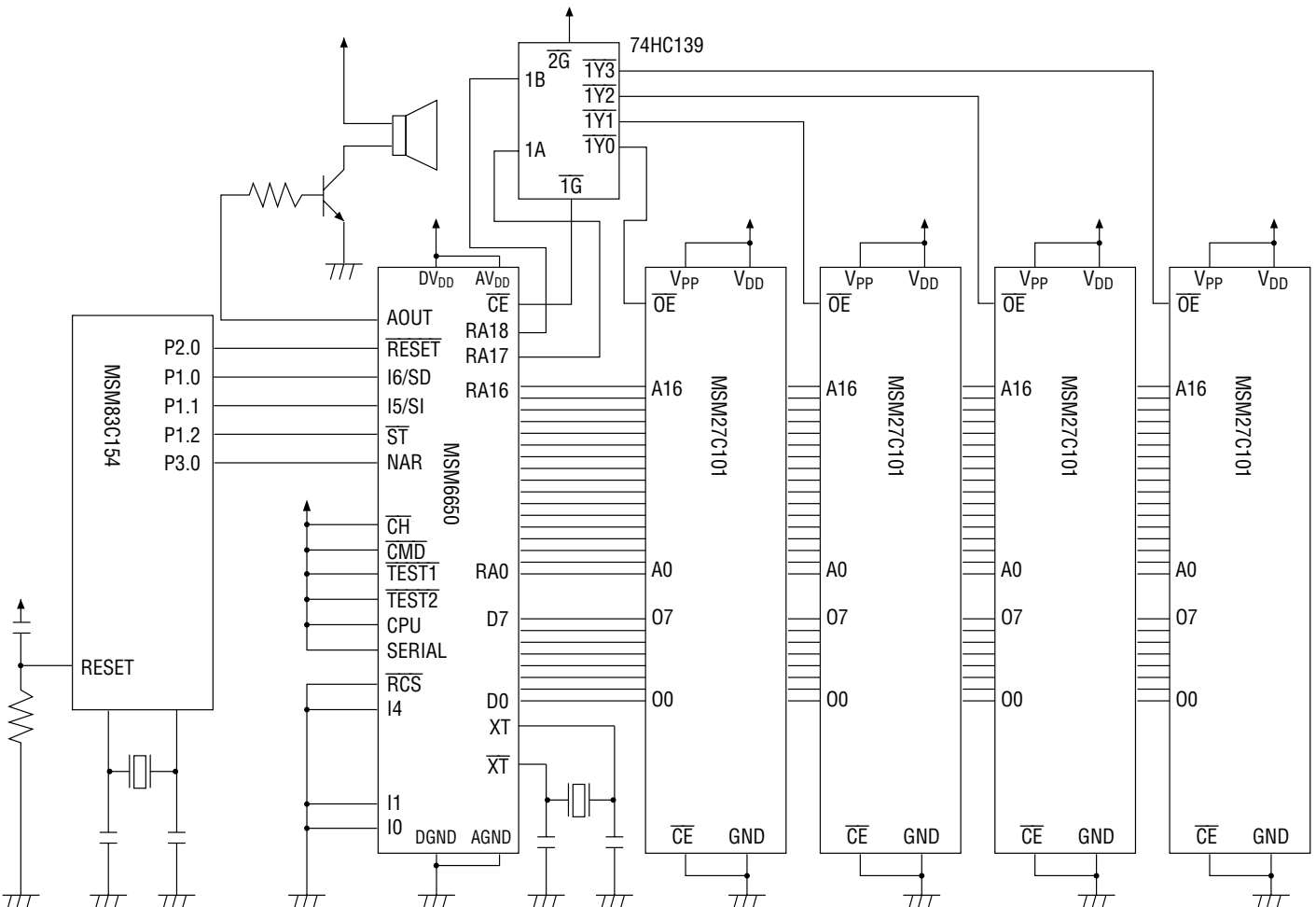(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54/P56-xx)
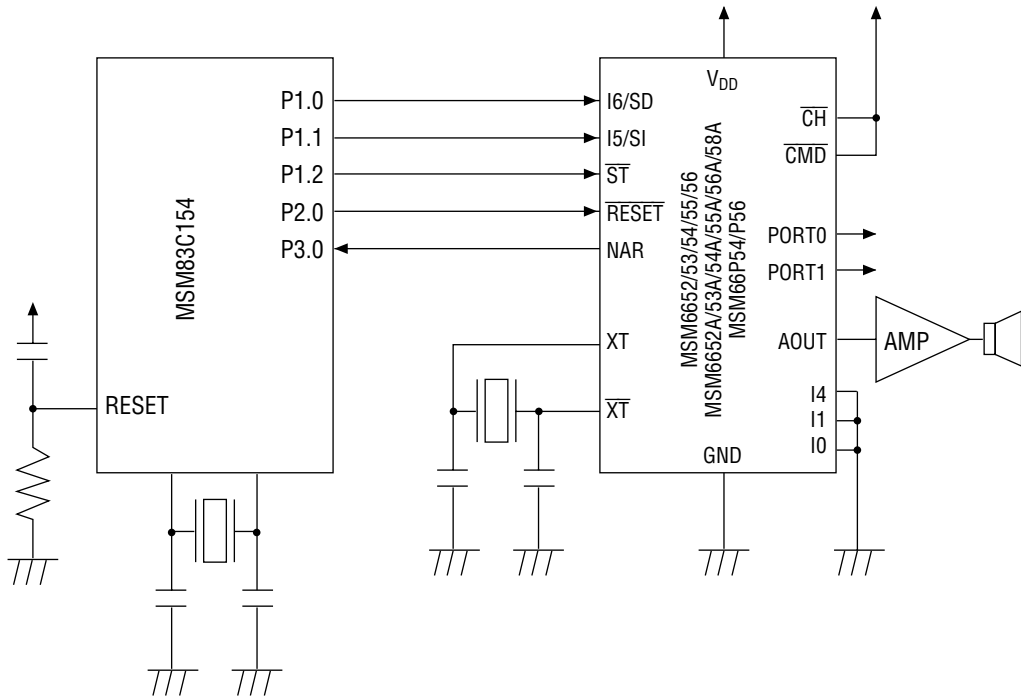
Application Circuit in Serial Input Interface Mode

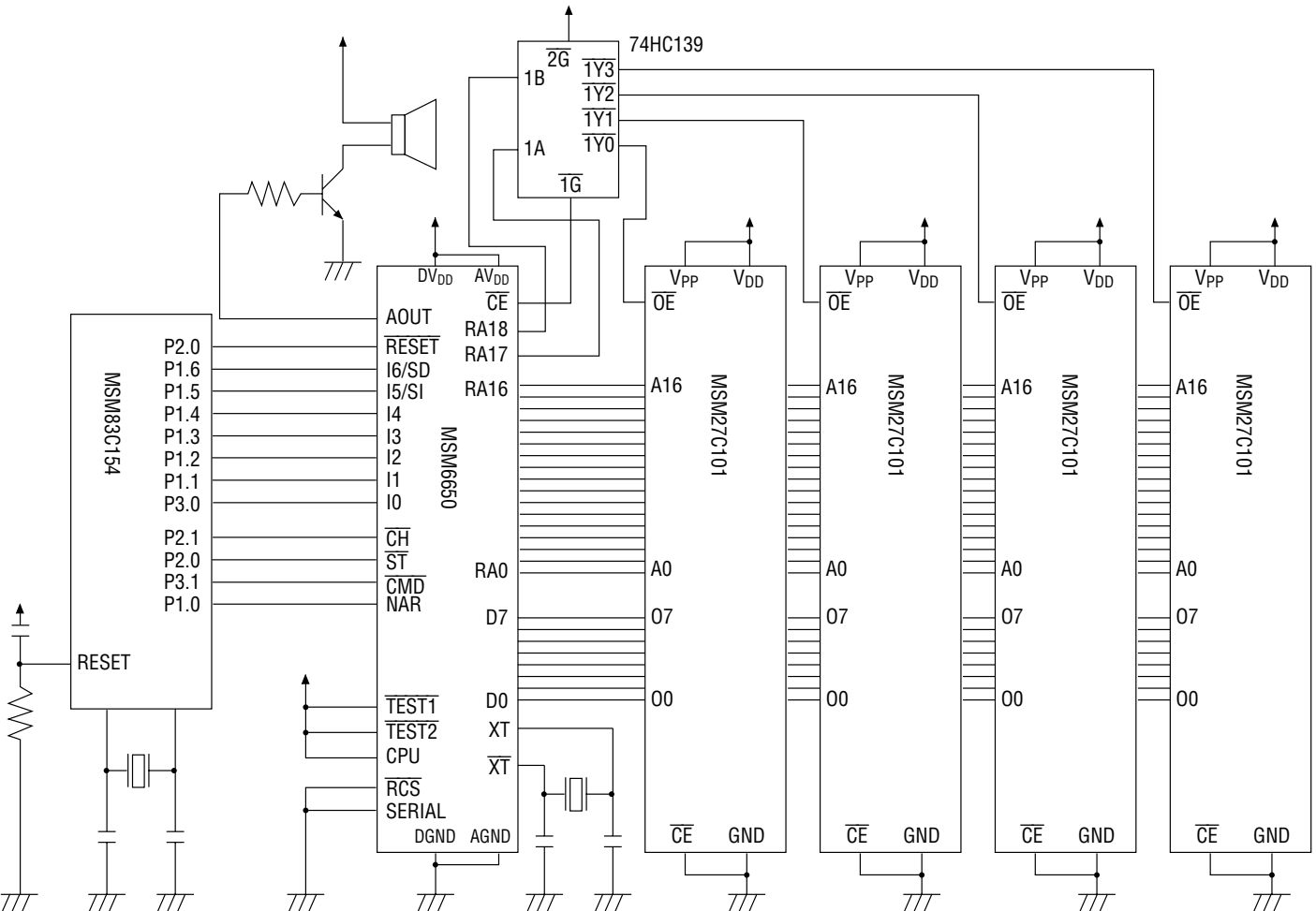(MSM6652/53/54/55/56-xxx, MSM6652A/53A/54A/55A/56A/58A-xxx, MSM66P54/P56-xx)

Application circuit in Parallel Input Interface Mode

(MSM6650)

**Application Circuit in Microcontroller Interface Mode
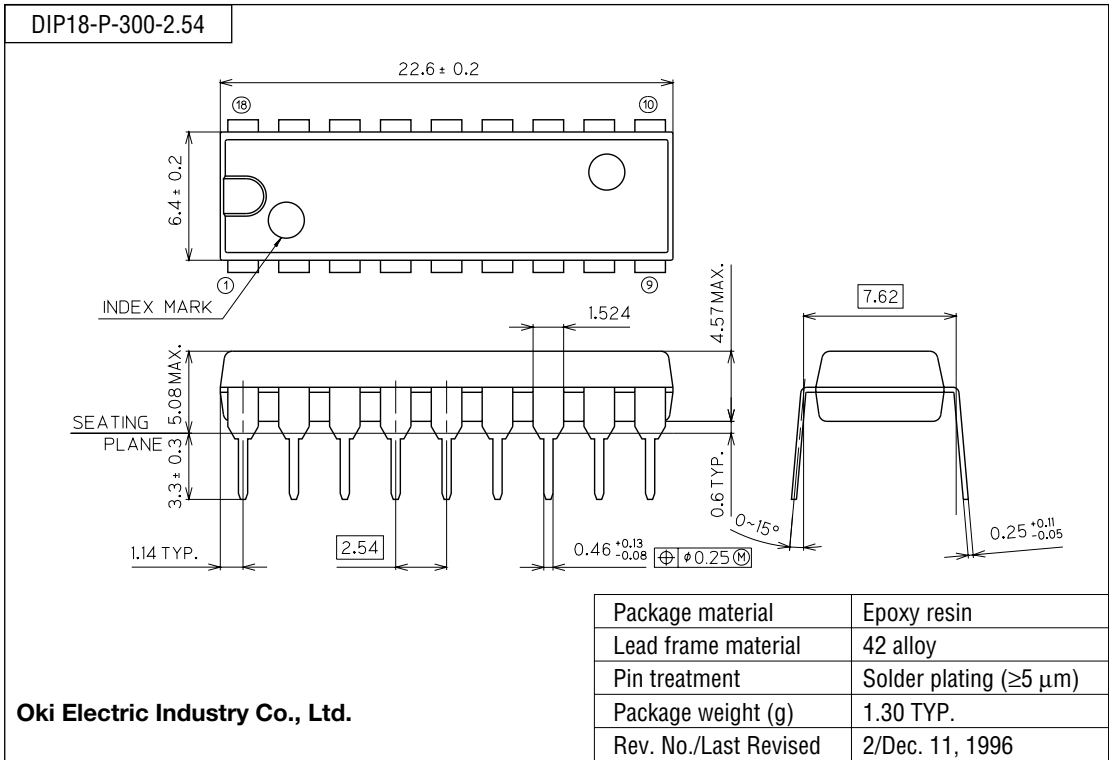Using Four 1-Mbit EPROMs (Serial Input Interface)**

Application Circuit in Microcontroller Interface Mode
Using Four 1-Mbit EPROMs (Parallel Input Interface)

OKI Semiconductor

PACKAGE DIMENSIONS

(Unit : mm)

DIP18-P-300-2.54

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating ($\geq$5 μm)
Package weight (g)	1.30 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

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(Unit : mm)

SOP24-P-430-1.27-K

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating ($\geq$5 μm)
Package weight (g)	0.58 TYP.
Rev. No./Last Revised	5/Oct. 13, 1998

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Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

DIP20-P-300-2.54-W1

INDEX MARK

SEATING PLANE

24.38 ± 0.2
7.3 ± 0.2
4.57 MAX.
5.08 MAX.
3.3 ± 0.76
0.38 MIN.
0.89
1.27
7.62
0.76 TYP.
2.54
0.51 +0.07 −0.14
⊕ φ 0.25 Ⓜ
0~15°
0.25 +0.11 −0.05

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	1.50 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

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(Unit : mm)

QFP64-P-1420-1.00-BK

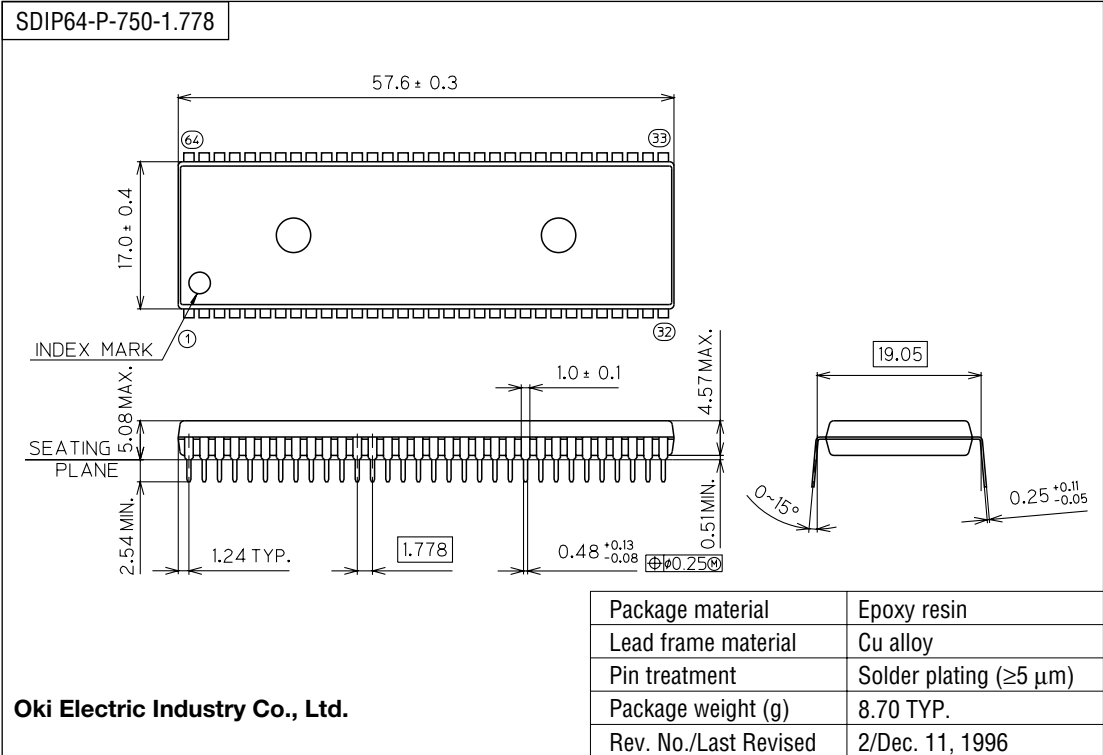| Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating ($\geq$5 μm)
Package weight (g)	1.25 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

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(Unit : mm)

SDIP64-P-750-1.778

Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	8.70 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

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