



12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

General Description

The MAX11080 is a battery-pack fault-monitor IC capable of monitoring up to 12 lithium-ion (Li+) battery cells. This device is designed to provide an overvoltage or undervoltage fault indication when any of the cells cross the user-selectable threshold for longer than the set program-delay interval. The overvoltage levels are pin selectable from +3.3V to +4.8V in 100mV increments, and have a guaranteed accuracy of $\pm 25\text{mV}$ over the entire temperature range. The undervoltage level is also user selectable from +1.6V to +2.8V in 200mV increments. These levels are guaranteed to $\pm 100\text{mV}$ over the entire temperature range. Undervoltage detection can be disabled as one of the user-configuration options.

The MAX11080 has a built-in level-shifter that allows up to 31 MAX11080 devices to be connected in a daisy-chain fashion to reduce the number of interface signals needed for large stacks of series batteries. Each cell is monitored differentially and compared to the overvoltage and undervoltage thresholds. When any of the cells exceed this threshold for longer than the set program delay interval, the MAX11080 inhibits the heartbeat signal from being passed down the daisy chain. Built-in comparator hysteresis prevents threshold chattering.

The MAX11080 is designed to be the perfect complement to the MAX11068 high-voltage measurement IC for redundant fault-monitoring applications. This device is offered in a 9.7mm x 4.4mm, 38-pin TSSOP package with 0.5mm pin spacing. The package is lead-free and RoHS compliant with an extended operating temperature range of -40°C to $+105^{\circ}\text{C}$.

Applications

High-Voltage, Multicell-Series-Stacked Battery Systems
 Electric Vehicles
 Hybrid Electric Vehicles
 Electric Bikes
 High-Power Battery Backup
 Solar Cell Battery Backup
 Super-Cap Battery Backup

Features

- ◆ Up to 12-Cell Li+ Battery Voltage Fault Detection
- ◆ Operation from 6.0V to 72V
- ◆ Pin-Selectable Overvoltage Threshold from +3.3V to +4.8V in 100mV Increments
 $\pm 25\text{mV}$ Overvoltage-Detection Accuracy
- ◆ Pin-Selectable Undervoltage Threshold from +1.6V to +2.8V in 200mV Increments
 $\pm 100\text{mV}$ Undervoltage-Detection Accuracy
- ◆ 300mV Over/Undervoltage-Threshold Detection Hysteresis
- ◆ Programmable Delay Time of Alarm Detection from 3.0ms to 3.32s with an External Capacitor
- ◆ Daisy-Chained Alarm and Shutdown Functions with Heartbeat Status Signal
 Up to 31 Devices Can Be Connected
- ◆ Ultra-Low-Power Dissipation
 Operating-Mode Current Drain: 80 μA
 Shutdown-Mode Current: 2 μA
- ◆ Wide Operating Temperature Range from -40°C to $+105^{\circ}\text{C}$ (AEC-Q100 Type 2)
- ◆ 9.7mm x 4.4mm, 38-Pin TSSOP Package
- ◆ Lead(Pb) Free and RoHS Compliant

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11080GUU+	-40°C to $+105^{\circ}\text{C}$	38 TSSOP
MAX11080GUU/V+	-40°C to $+105^{\circ}\text{C}$	38 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

V denotes an automotive qualified part.

Pin Configuration appears at end of data sheet.

12-Channel, High-Voltage Battery-Pack Fault Monitor

ABSOLUTE MAXIMUM RATINGS

HV, VDD _U , GND _U , DCIN to AGND	-0.3V to +80V
HV to DCIN and C12	-0.3V to +6V
C2–C12 to AGND	-0.3V to (V _{DCIN} + 0.6V)
C _{n+1} to C _n , where n = 2 to 12	-0.3V to +80V
C1 to C0	-0.3V to +20V (Note 1)
C1 to AGND	-0.3V to (V _{DCIN} + 0.6V) (Note 2)
C0 to AGND	-0.3V to +0.9V
$\overline{\text{SHDN}}$, V _{AA} to AGND	-0.3V to +4V
VDD _U to GND _U	-0.3V to +6V
OVSEL ₋ , UVSEL ₋ , TOPSEL to AGND	-0.3V to (+V _{AA} + 0.3V)
CD, ALRM _L to AGND	-0.3V to (+V _{AA} + 0.3V)
ALRM _U to GND _U	-0.3V to (+VDD _U + 0.3V)
CP+ to AGND	(GND _U - 0.3V) to (VDD _U + 0.3V)
CP- to AGND	-0.3V to (GND _U + 0.3V)
CP- to VDD _U	+0.3V

ESD Rating

C ₋ , REF, V _{AA} , VDD _U , GND _U , DCIN, $\overline{\text{SHDN}}$, CP+, CP-, HV, OVSEL ₋ , UVSEL ₋ , TOPSEL, ALRM _U , ALRM _L , AGND, CD	±2kV (Human Body Model, Note 3)
Continuous Power Dissipation (T _A = +70°C) 38-Pin TSSOP (derating 15.9mW/°C above +70°C)	1095.9mW
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-55°C to +150°C
Junction Temperature (continuous)	+150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: The C1 to C0 differential input path is tolerant to 80V as long as the $\overline{\text{SHDN}}$ pin is deasserted.

Note 2: The C1 input is tolerant to a maximum V_{DCIN} + 0.6V. If $\overline{\text{SHDN}}$ is asserted, 20V is the maximum rating.

Note 3: Human Body Model to Specification MIL-STD-883 Method 3015.7.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted. V_{DCIN} = V_{GND_U} = +6.0V to +72V, typical values are at T_A = +25°C, unless otherwise specified from -40°C to +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
C₋ INPUTS						
Common-Mode Input Range	V _{CXIN}	Any two inputs C _n to C _{n+1} for full threshold accuracy (Note 4)	1.5		72	V
Input Current	I _{CXIN}	V _{CELL} = 3.0V	-1	0.05	+1	μA
Overvoltage Threshold	V _{OV}		+3.3		+4.8	V
Overvoltage-Threshold Accuracy				±5	±25	mV
Undervoltage Threshold	V _{UV}		+1.6		+2.8	V
Undervoltage-Threshold Accuracy				±20	±100	mV
Comparator Hysteresis	V _{HYS}			300		mV
CD PIN						
CD Current	I _{CD}	V _{CD} = 0.4V	4.35	6.1	7.65	μA
CD Trip Voltage	V _{CD}	Internal at comparator		1.23		V
Delay-Time Accuracy		Excluding C _{DLY} variation		±20		%
STATUS/CONTROL PORT						
Shutdown Disable ($\overline{\text{SHDN}}$ High Voltage)	$\overline{\text{SHDN}}/V_{IH}$		2.1			V
Shutdown Asserted ($\overline{\text{SHDN}}$ Low Voltage)	$\overline{\text{SHDN}}/V_{IL}$				0.6	V

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

ELECTRICAL CHARACTERISTICS (continued)

($T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. $V_{DCIN} = V_{GND_U} = +6.0V$ to $+72V$, typical values are at $T_A = +25^\circ C$, unless otherwise specified from $-40^\circ C$ to $+105^\circ C$.)

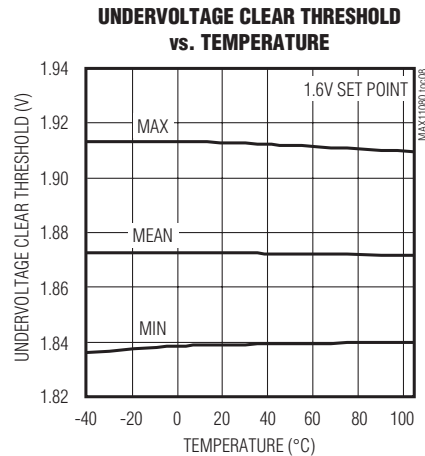
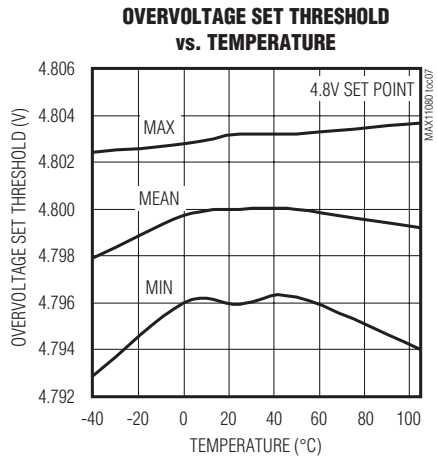
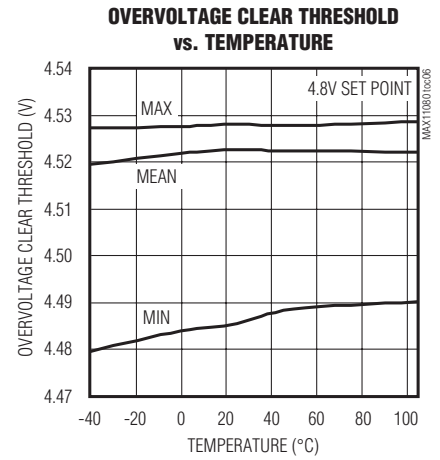
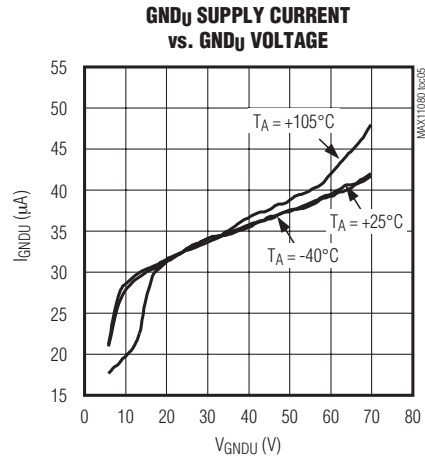
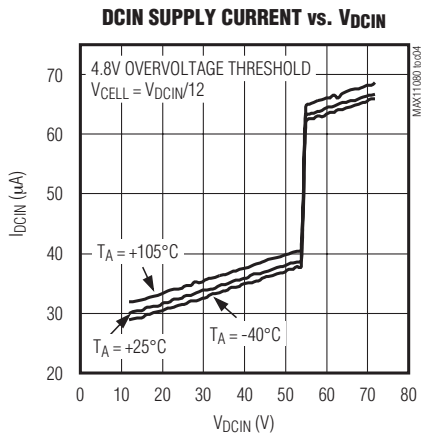
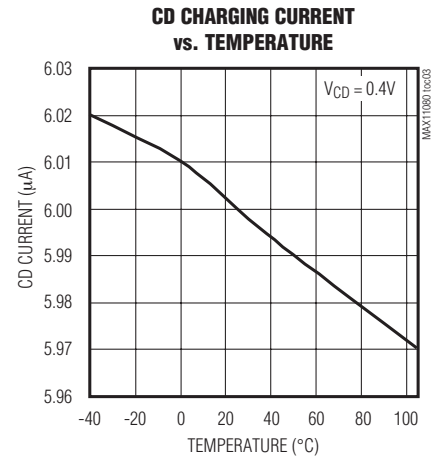
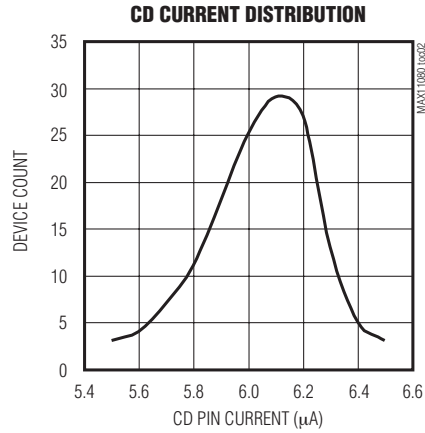
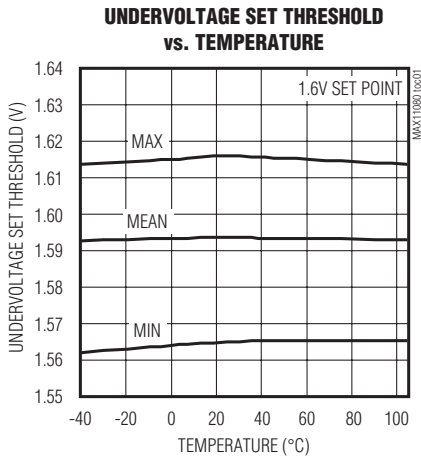
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VDD _U Output High	VDD _U V _{OH}	Output voltage of VDD _U after the 20k Ω /200k Ω resistor-divider to \overline{SHDN}	GND _U + 2.4			V
VDD _U Output Low	VDD _U V _{OL}	Output voltage of VDD _U after the 20k Ω /200k Ω resistor-divider for \overline{SHDN}			GND _U + 0.3	V
ALRM _L Output-Voltage High	ALRM _L V _{OH}	I _{SOURCE} = 150 μ A	2.4			V
ALRM _L Output-Voltage Low	ALRM _L V _{OL}	I _{SINK} = 150 μ A			0.6	V
ALRM _U Input-Voltage High	ALRM _U V _{IH}	Daisy-chained ALRM _U signal as coupled through a 3.3nF high-voltage capacitor and a 150k Ω resistor as referred to GND _U	GND _U + 2.1			V
ALRM _U Input-Voltage Low	ALRM _U V _{IL}	Daisy-chained ALRM _U signal as coupled through a 3.3nF high-voltage capacitor and a 150k Ω resistor as referred to GND _U			GND _U + 0.9	V
Alarm Voltage Output "Heartbeat" Frequency	ALRM _L f _{OUT}	Heartbeat clock rate with no alarm condition	4032	4096	4157	Hz
Alarm Voltage Output Duty Cycle		Heartbeat clock rate with no alarm condition	49.0		51.0	%
LINEAR REGULATOR (V_{AA})						
Input Voltage Range	V _{DCIN}		6		72	V
Output Voltage	V _{AAOUT}	6V < V _{DCIN} < 72V, I _{LOAD} = 0	3.0	3.3	3.6	V
Short-Circuit Current	I _{AASHORTCIRCUIT}	V _{AA} = 0, 6V < V _{DCIN} < 36V			50	mA
Power-On-Reset Trip Level (Note 4)	V _{AARESET}	Falling V _{AA}		2.8		V
	V _{AAVALID}	Rising V _{AA}		3.0		
	V _{AAHYS}	Hysteresis on rising V _{AA}		37		mV
Thermal Shutdown	T _{SHUT}	Rising temperature		+145		$^\circ C$
POWER-SUPPLY REQUIREMENTS (DCIN)						
Current Consumption	I _{DCIN}	Operating mode, $\overline{SHDN} = 1$, 12 battery cells, alarm inactive, V _{DCIN} = V _{GND_U} = 36V		35	40	μA
		Shutdown mode, $\overline{SHDN} = 0$, 12 battery cells, V _{DCIN} = V _{GND_U} = 36V		1.3	2	
I _{GND_U} Operating Mode		$\overline{SHDN} = 1$, battery cells, alarm inactive, V _{DCIN} = V _{GND_U} = 36V		35	40	μA
LOGIC INPUTS AND OUTPUTS						
Threshold Setting	V _{IH}	UVSEL0/UVSEL1/UVSEL2, TOPSEL	V _{AA} - 0.1			V
	V _{IL}	OVSEL0/OVSEL1/OVSEL2/OVSEL3			0.1	

Note 4: Guaranteed by design and not production tested.

12-Channel, High-Voltage Battery-Pack Fault Monitor

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



12-Channel, High-Voltage Battery-Pack Fault Monitor

Pin Description

MAX11080

PIN	NAME	FUNCTION
1	DCIN	DC Power-Supply Input. DCIN supplies the internal 3.3V regulator. This pin should be connected as shown in the application diagrams.
2	HV	High-Voltage Bias. HV is biased by the output of the charge pump to provide a DC supply above the DCIN level. It is used internally to bias the cell-comparator circuitry. Bypass to DCIN with a 1 μ F capacitor.
3, 33	N.C.	No Connection
4	C12	Cell 12 Plus Connection. Top of battery module stack.
5	C11	Cell 12 Minus Connection and Cell 11 Plus Connection
6	C10	Cell 11 Minus Connection and Cell 10 Plus Connection
7	C9	Cell 10 Minus Connection and Cell 9 Plus Connection
8	C8	Cell 9 Minus Connection and Cell 8 Plus Connection
9	C7	Cell 8 Minus Connection and Cell 7 Plus Connection
10	C6	Cell 7 Minus Connection and Cell 6 Plus Connection
11	C5	Cell 6 Minus Connection and Cell 5 Plus Connection
12	C4	Cell 5 Minus Connection and Cell 4 Plus Connection
13	C3	Cell 4 Minus Connection and Cell 3 Plus Connection
14	C2	Cell 3 Minus Connection and Cell 2 Plus Connection
15	C1	Cell 2 Minus Connection and Cell 1 Plus Connection
16	C0	Cell 1 Minus Connection
17	UVSEL0	Undervoltage Threshold Select 2 to 0. Used to select one of eight undervoltage alarm threshold settings. The parts have internal pulldown; these pins should only be tied to V _{AA} or AGND to set the logic state.
18	UVSEL1	
19	UVSEL2	
20	OVSEL0	Overvoltage Threshold Select 3 to 0. Used to select one of 16 overvoltage alarm threshold settings. The parts have internal pulldown; these pins should only be tied to V _{AA} or AGND to set the logic state.
21	OVSEL1	
22	OVSEL2	
23	OVSEL3	
24	V _{AA}	+3.3V Analog Supply Output. Bypass with a 1 μ F capacitor to AGND.
25, 29, 30, 32	AGND	Analog Ground. Should be connected to the negative terminal of cell 1.
26	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. This pin completely shuts down the MAX11080 internal regulator and oscillators when the pin is less than 0.6V as referenced to AGND. The host controller should drive $\overline{\text{SHDN}}$ for the first pack. $\overline{\text{SHDN}}$ for daisy-chained modules should be connected to the lower neighboring module's V _{DDU} through a 20k Ω series resistor.
27	ALRML	Lower Port Alarm Output. This output is an alarm indicator for overvoltage, undervoltage, and setup faults. The alarm signal is daisy chained and driven from the highest module down to the lowest. The alarm output is nominally a clocked "heartbeat" signal that provides a 4kHz clock when no alarm is present. The ALRML can also be configured as level signal and set to "low" for no alarm and "high" for alarm state. See the <i>TOPSEL Function</i> section for details. This signal swings between V _{AA} and AGND, and is active high in the alarm state.
28	CD	Programmable Delay Time. Connect a capacitor from this pin to AGND to set the hold time required for a fault condition before the alarm is set. The capacitor should be a ceramic capacitor in the 15nF to 16.5 μ F range.

12-Channel, High-Voltage Battery-Pack Fault Monitor

Pin Description (continued)

PIN	NAME	FUNCTION
31	TOPSEL	Input to Indicate Topmost Device in the Daisy Chain. This pin should be connected to AGND for all devices except the topmost. For the top device, this pin should be connected to V _{AA} .
34	ALRM _U	Upper Port Alarm Input. This input receives the ALRM _L output signal from an upper neighboring module. It swings between VDD _U and GND _U .
35	GND _U	Level-Shifted Upper Port Ground. Upper port-supply return and supply input for the charge pump and HV supplies. This pin should be connected to the DCIN takeoff point on the battery stack as shown in the application diagrams.
36	VDD _U	Level-Shifted Upper Port Supply. Upper port-supply output for the daisy-chained bus. This is a regulated output voltage from the internal charge pump that is level-shifted above the DCIN pin voltage level. It should be bypassed with a 1μF capacitor to GND _U .
37, 38	CP-, CP+	Charge-Pump Capacitor. Negative/positive input for the internal charge pump. Connect a 0.01μF high-voltage capacitor between CP+ and CP-.

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

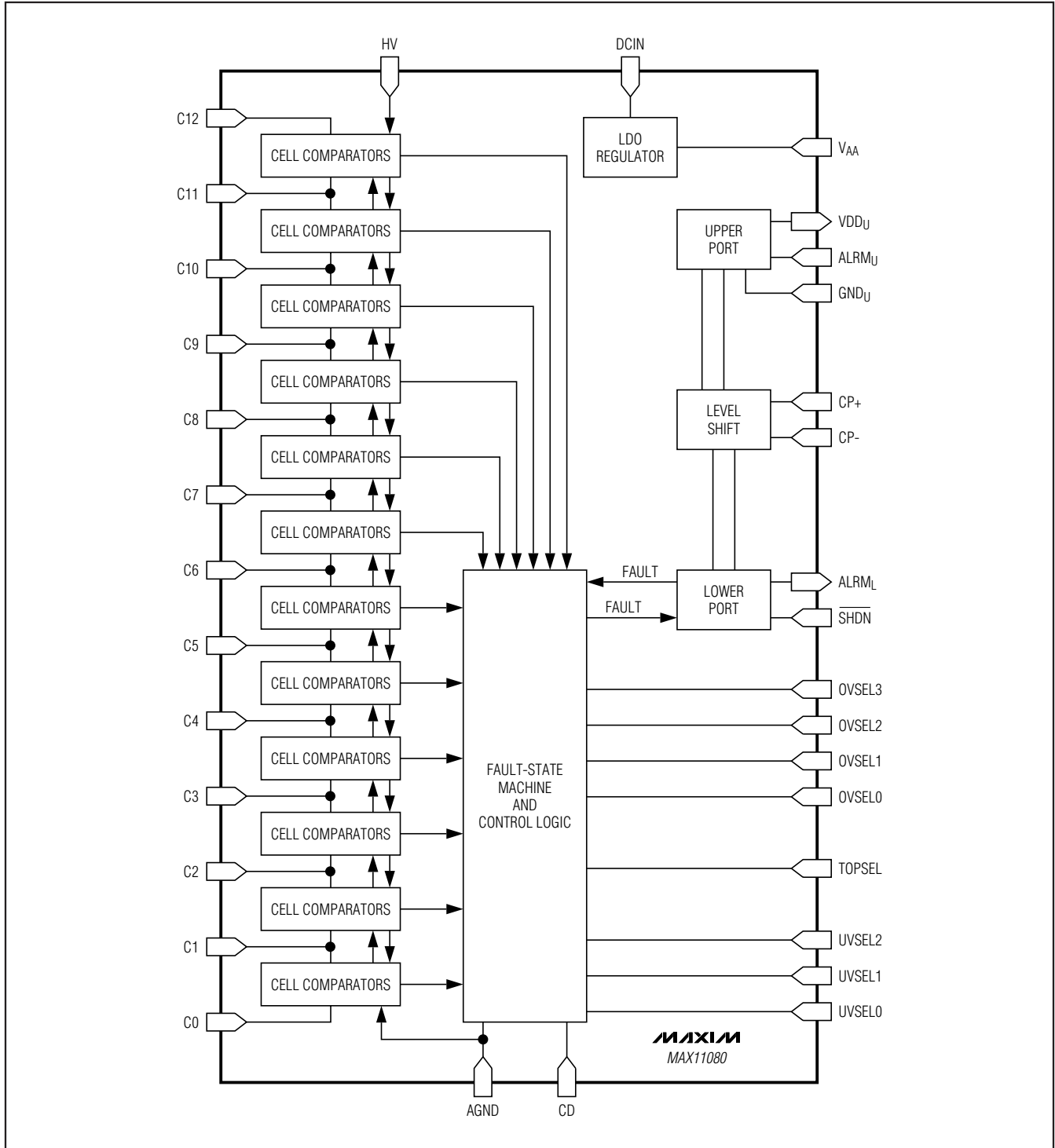


Figure 1. Functional Diagram

12-Channel, High-Voltage Battery-Pack Fault Monitor

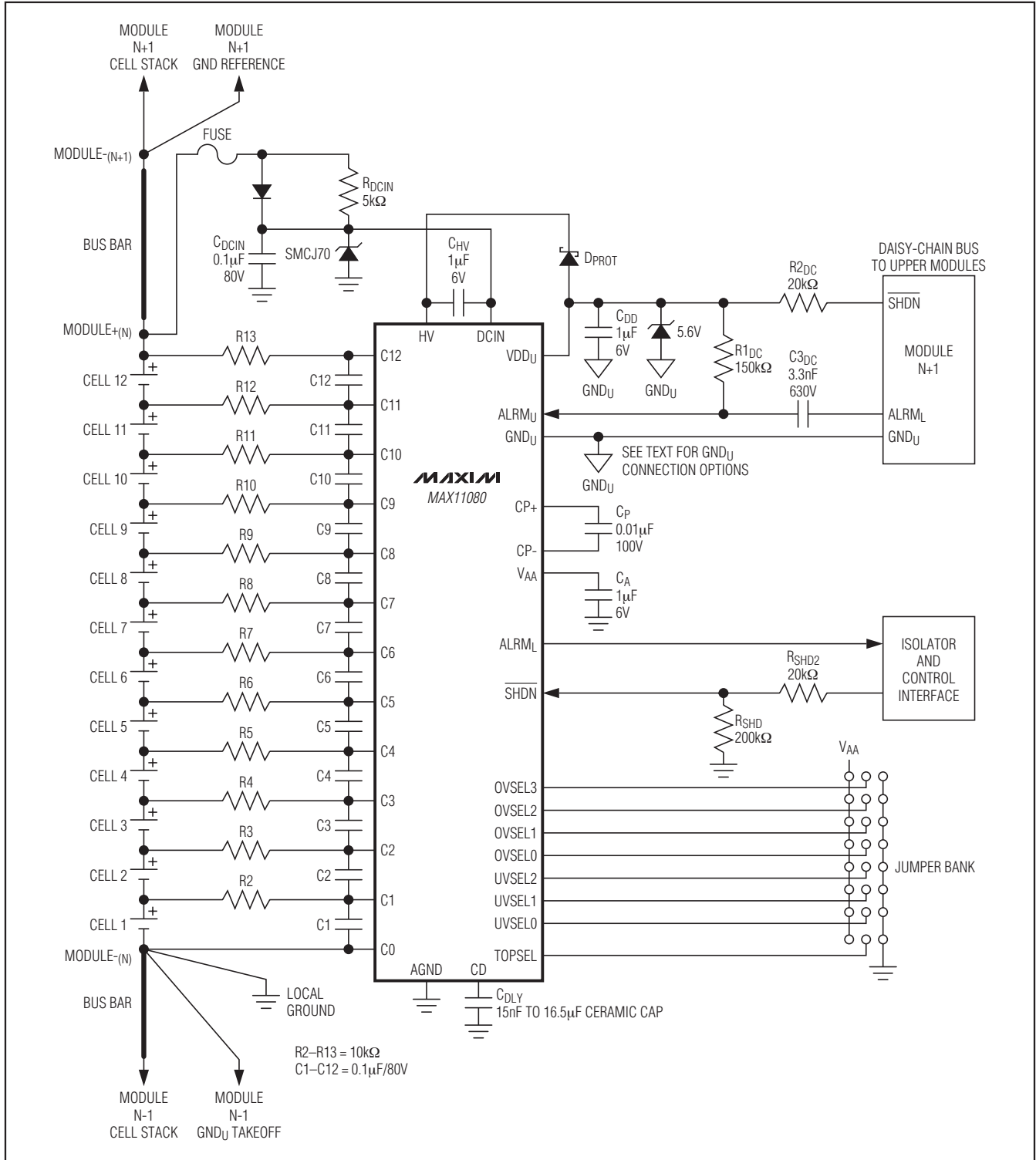


Figure 2. Application Circuit Diagram for a 12-Cell System

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

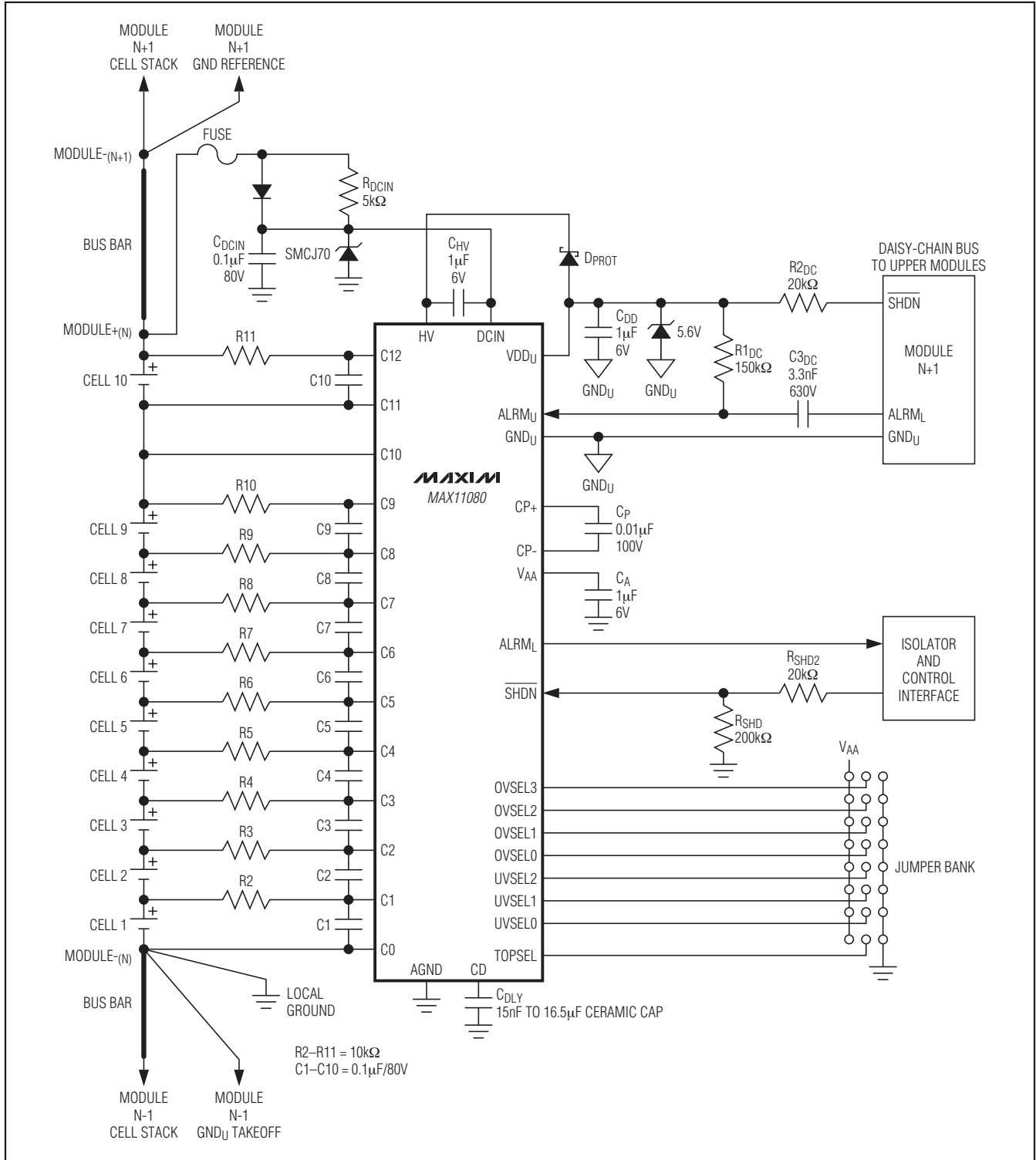


Figure 3. Application Circuit Diagram for a 10-Cell System

12-Channel, High-Voltage Battery-Pack Fault Monitor

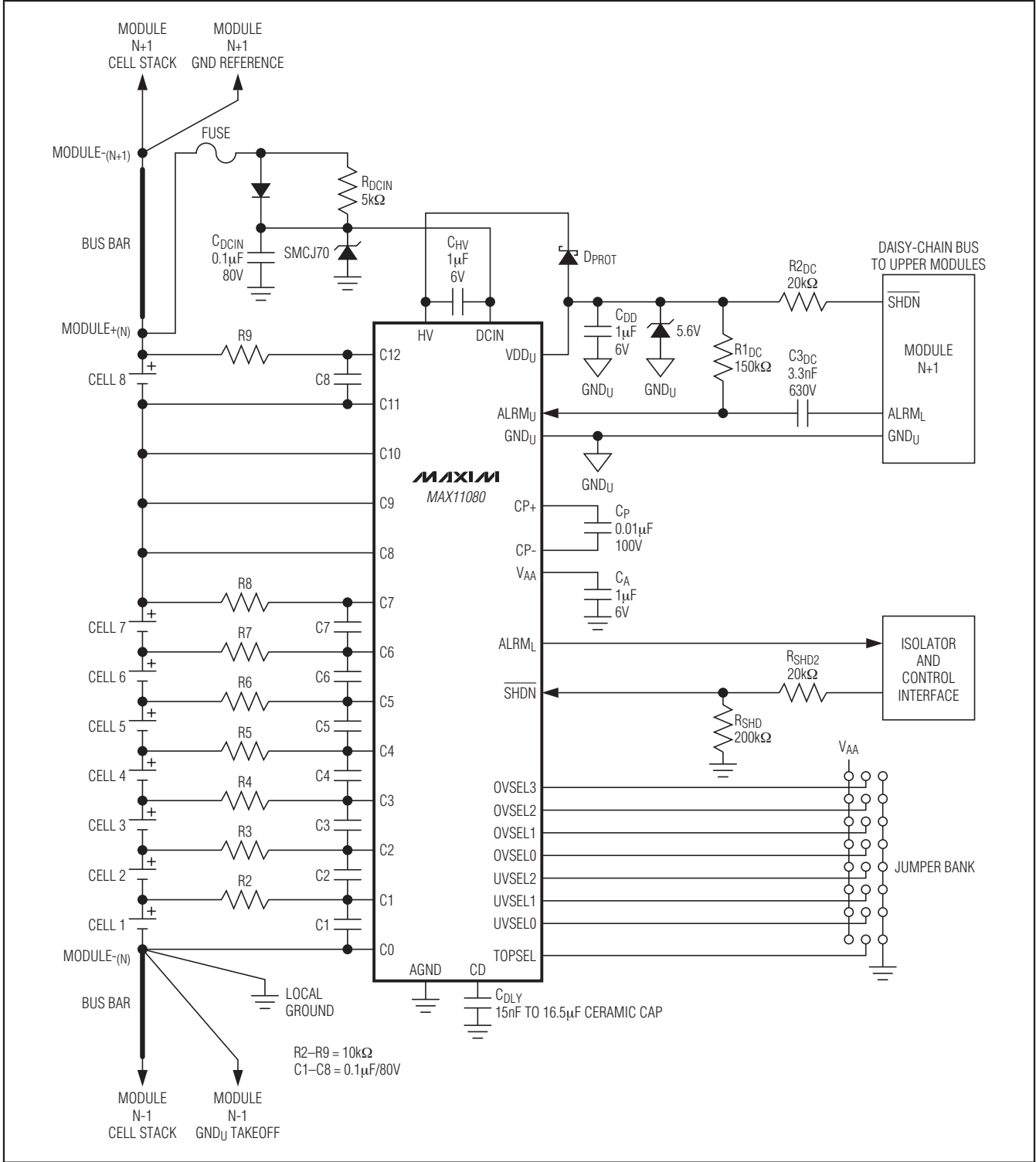
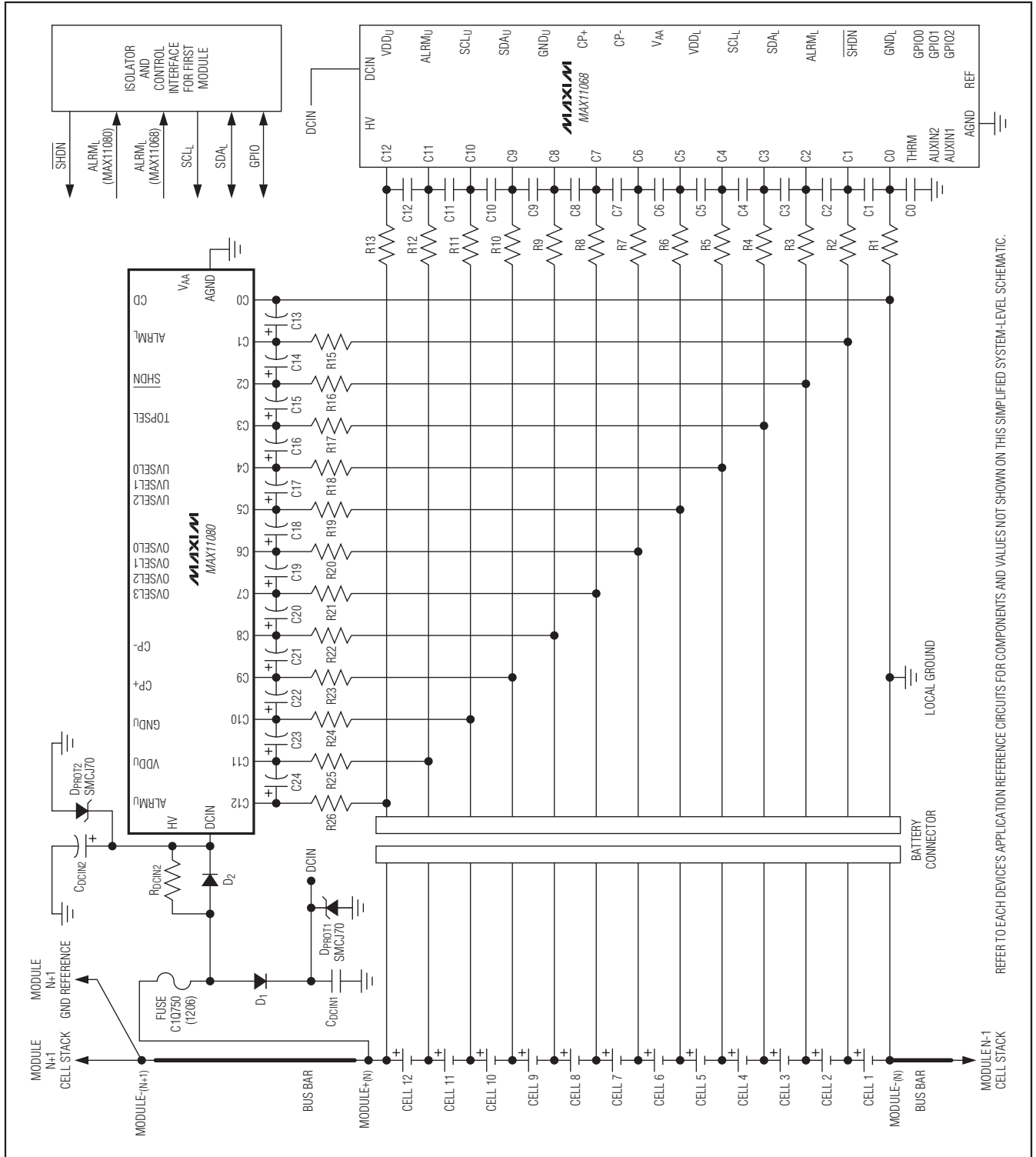


Figure 4. Application Circuit Diagram for an 8-Cell System

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080



REFER TO EACH DEVICE'S APPLICATION REFERENCE CIRCUITS FOR COMPONENTS AND VALUES NOT SHOWN ON THIS SIMPLIFIED SYSTEM-LEVEL SCHEMATIC.

Figure 5. Battery Module System with Redundant Fault-Detection Application Schematic

12-Channel, High-Voltage Battery-Pack Fault Monitor

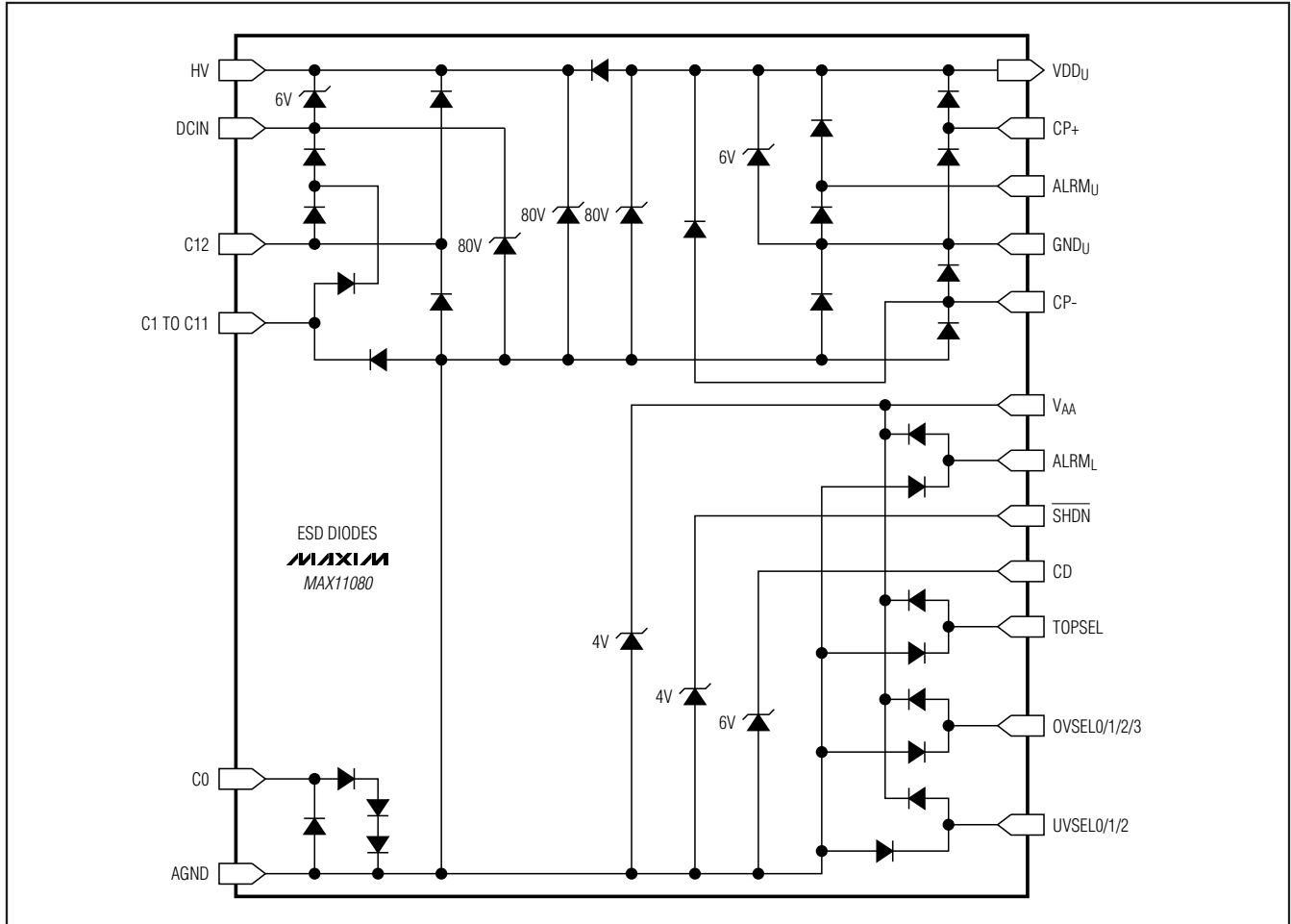


Figure 6. ESD Diode Diagram

Detailed Description

Figure 1 shows the functional diagram; Figure 2 shows the application circuit diagram for a 12-cell system while Figure 3 shows the application circuit design for a 10-cell system and Figure 4 for an 8-cell system. Figure 5 is the application schematic for the battery module system with redundant fault detection.

Architectural Overview

The MAX11080 is a battery-pack fault-monitor IC capable of monitoring up to 12 Li+ battery cells. This device is designed to provide an overvoltage or undervoltage alarm indicator when any of the cells cross the user-selectable threshold for longer than the configured decision delay interval. The MAX11080 also incorporates a daisy-chain bus for use in high-voltage stacked-battery operation. The daisy-chain bus relays shutdown

and alarm communication across up to 31 stacked modules without the need for isolation between each module. This results in a simplified system with reduced cost. The MAX11080 is ideal as an ultra-low-power, redundant cell fault monitor that is the perfect complement to the MAX11068 high-voltage battery measurement IC. Both ICs in concert form a powerful Li+ battery system monitor with redundant overvoltage and undervoltage fault detection.

Overvoltage and Undervoltage Fault Detection

Figure 7 summarizes the fault-detection mechanism for a set of differential cell inputs in the MAX11080.

First, the differential cell inputs are attenuated by a factor of four while being level-shifted and converted to a single-ended voltage referenced to AGND. The ground-

12-Channel, High-Voltage Battery-Pack Fault Monitor

referenced voltage is then connected to a set of over-voltage and undervoltage comparators. The threshold references for the comparators are set by the UVSEL_ and OVSEL_ input pins. When one of the cell voltages exceeds V_{OV} or is below V_{UV} when V_{UV} is enabled, the internal cell out-of-range signal for the given cell is set and logically ORed with the same signal for the other cell positions to create an overall out-of-range signal.

When any cells are out-of-range as indicated by the internal out-of-range signal, an internal current source begins to charge the capacitor C_{DLY} connected to the

CD pin. If the voltage at the CD pin reaches V_{CD} , the $ALRM_L$ line is set to V_{AA} (+2.4V minimum as referred to AGND). Normally, the $ALRM_L$ line is a heartbeat signal with pulses occurring every 250 μ s. If all cell voltages transition from out-of-range to in-range before the voltage at pin CD reaches V_{CD} , an internal switch clamps the CD pin to GND. This action discharges C_{DLY} and, because the delay had not yet expired, no alarm occurs. Discharging C_{DLY} ensures that the full delay time occurs for the next overvoltage or undervoltage event. Figure 8 summarizes the C_{DLY} circuit.

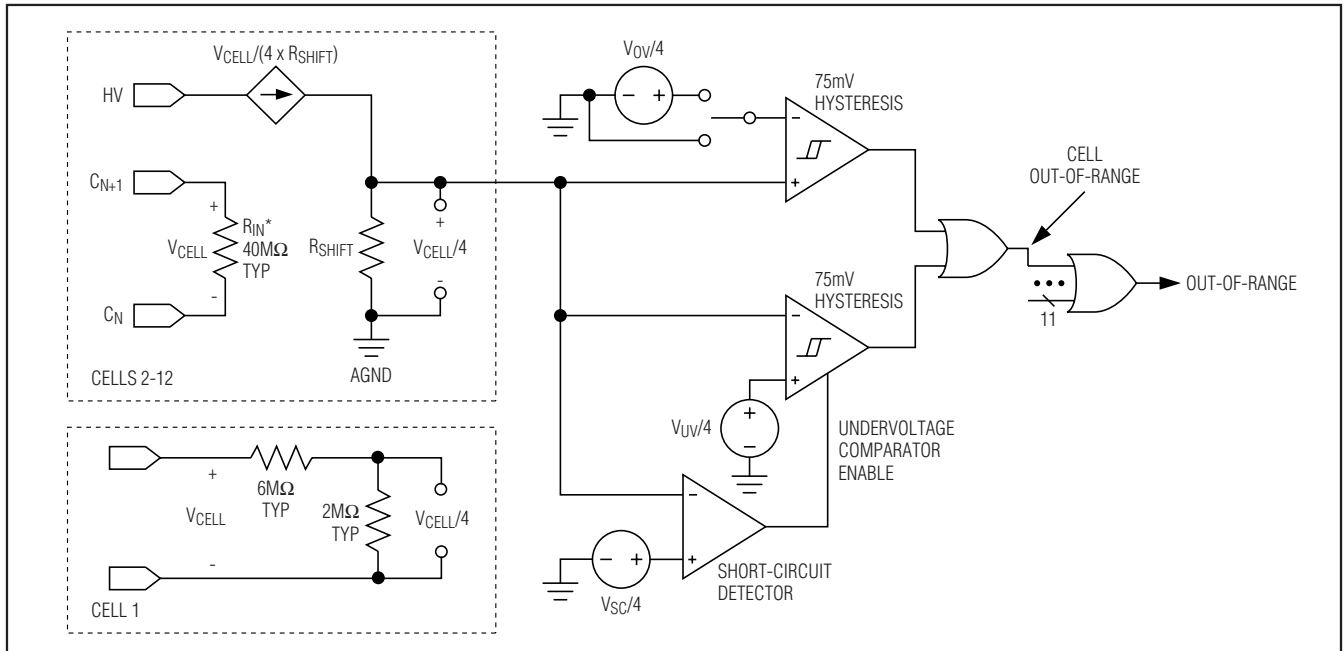


Figure 7. Cell Differential Input and Comparator Block Diagram

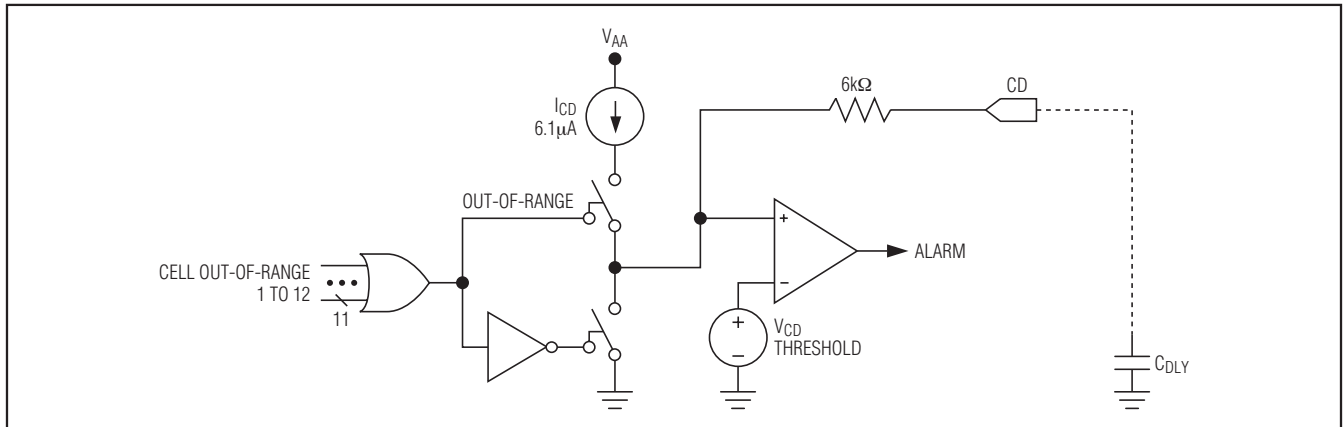


Figure 8. C_{DLY} Circuit Block Diagram

12-Channel, High-Voltage Battery-Pack Fault Monitor

Once the ALRM_L pin is forced high due to an alarm (+2.4V minimum as referred to AGND), it transitions back to a heartbeat signal only after all battery cells meet the following condition:

$$(V_{OV} - V_{HYS}) > V_{CELL(ALL)} > (V_{UV} + V_{HYS})$$

Examples of cell-voltage readings and their effect on the alarm status are shown in Figures 9 and 10 for single- and multiple-cell systems. In the case where an upper module is forwarding an active alarm condition down the daisy chain, that condition continues to be propagated toward the host regardless of the alarm state of any lower module. Furthermore, to circumvent the possibility of a short-circuited capacitor connected to CD preempting the fault-time validation process, a redundant built-in delay of 4s nominal is asserted as a backup. If the V_{CD} threshold is not reached within 4s of an out-of-range event, the alarm becomes active.

Programmable Delay Time

The alarm trigger delay time is calculated according to the following equations:

$$t_{DLY} = (V_{CD} \times C_{DLY}) / I_{CD}$$

$$C_{DLY} = (t_{DLY} \times I_{CD}) / V_{CD}$$

The effective I_{CD} value of the current source is 6.1μA typical and the threshold voltage, V_{CD}, is 1.23V typical. The V_{CD} threshold is specified at an internal node prior to the resistor in series with the CD pin as shown in Figure 8. The threshold voltage seen at the pin is approximately 1.18V due to the drop associated with the typical I_{CD} value and the 6kΩ resistor. The MAX11080 can operate with capacitor values from 15nF (3.0ms) to 16.5μF (3.32s). Each capacitor should have a voltage tolerance of 5V minimum.

Cell-Voltage Threshold Selection

The overvoltage and undervoltage threshold selection is configured through the OVSEL_{_} and UVSEL_{_} inputs. The overvoltage selection can be configured from 3.3V to 4.8V in 100mV increments. The undervoltage threshold can be configured from 1.6V to 2.8V in 200mV increments. The undervoltage detection can also be disabled. See Tables 1 and 2 for the proper configuration settings.

Immunity to unintended changes in the threshold voltage setting (due to accidental pin-to-pin short circuits, for example) is provided. The customer-programmed selection is sensed and stored at power-up and any subsequent change to the input pin status is ignored.

Table 1. Overvoltage Threshold Selection

THRESHOLD (V)	OVERVOLTAGE SELECTION			
	OVSEL3	OVSEL2	OVSEL1	OVSEL0
3.3	0	0	0	0
3.4	0	0	0	1
3.5	0	0	1	0
3.6	0	0	1	1
3.7	0	1	0	0
3.8	0	1	0	1
3.9	0	1	1	0
4.0	0	1	1	1
4.1	1	0	0	0
4.2	1	0	0	1
4.3	1	0	1	0
4.4	1	0	1	1
4.5	1	1	0	0
4.6	1	1	0	1
4.7	1	1	1	0
4.8	1	1	1	1

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

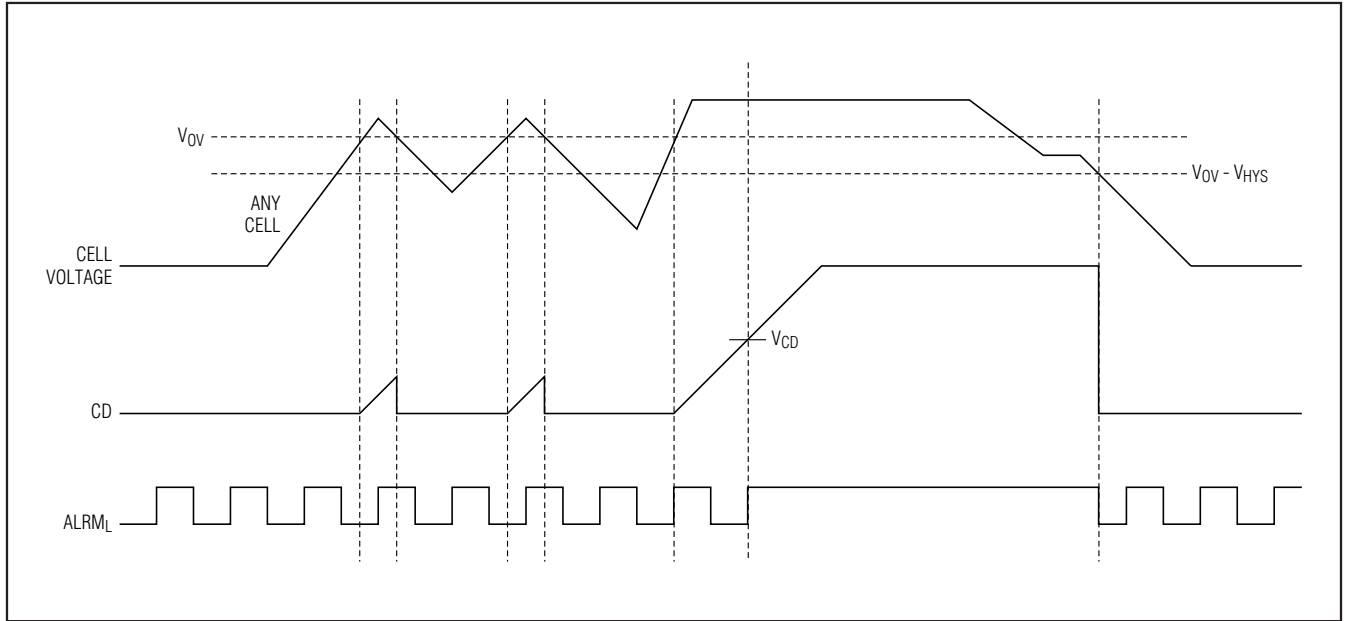


Figure 9. Single-Cell Overvoltage Detection Example

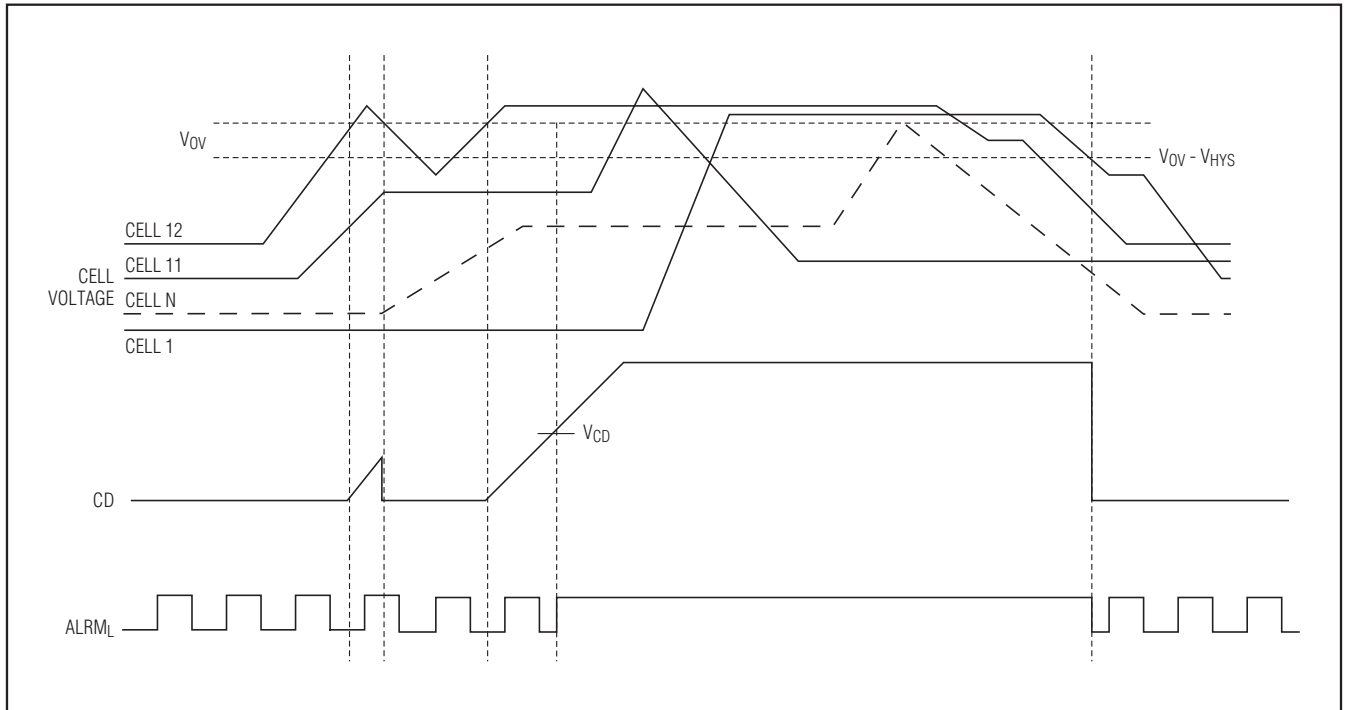


Figure 10. Multiple-Cell Overvoltage Detection Example

12-Channel, High-Voltage Battery-Pack Fault Monitor

Table 2. Undervoltage Threshold Selection

THRESHOLD (V)	UNDervOLTAGE SELECTION		
	UVSEL2	UVSEL1	UVSEL0
Disabled	0	0	0
1.6	0	0	1
1.8	0	1	0
2.0	0	1	1
2.2	1	0	0
2.4	1	0	1
2.6	1	1	0
2.8	1	1	1

Internal Linear Regulator

The MAX11080 has an internal linear regulator for generating the internal supply from DCIN (Figure 11). The regulator can accept a supply voltage on the DCIN pin from +6.0V to +72V, which it regulates to 3.3V to run the voltage-detection system, control logic, and low-side alarm-pulse interface. When the SHDN pin is not active and a sufficient voltage is applied to DCIN, the output of the regulator becomes active. The regulator is paired with a power-on-reset (POR) circuit that senses

its output voltage and holds the MAX11080 in a reset state until the internal supply has reached a sustainable threshold of +3.0V ($\pm 5\%$). The internal comparators have built-in hysteresis that can reject noise on the supply line. Because secondary metal batteries are never fully discharged to 0V, the MAX11080 is designed for a hot-swap insertion of the battery cells. Once the POR threshold is reached, approximately 1ms later the internal reset signal disables, the internal oscillator starts, and the charge pump begins operating. The charge

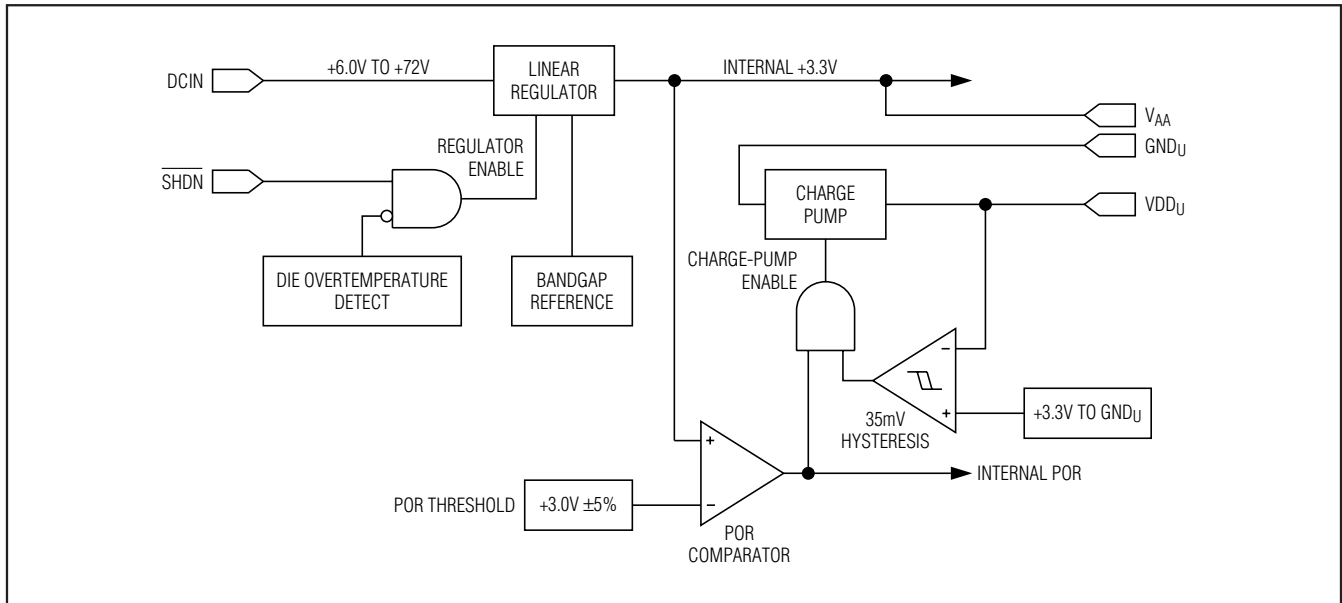


Figure 11. Internal Linear Regulator Block Diagram

12-Channel, High-Voltage Battery-Pack Fault Monitor

pump reaches regulation in approximately 3ms. The MAX11080 associated with the top module in the battery pack is identified as detailed in the *TOPSEL Function* section. This is followed by a self-test of the overvoltage comparators and detection of the number of cells connected. At this time in the power-on sequence, the MAX11080 is ready for operation. When the charge pump achieves regulation of 3.3V between VDD_U and GND_U , it switches to a standby mode until the voltage drops by about 35mV. The specified accu-

racy and full operation of the MAX11080 are not guaranteed until a minimum of 6.0V is applied to the DCIN pin.

The linear regulator also incorporates a thermal shutdown feature. If the MAX11080 die temperature rises above +145°C, the device shuts down. After a thermal shutdown, the die temperature must cool 15°C below the shutdown temperature before the device restarts.

Figure 12 shows the linear regulator power-up sequence and Figure 13 shows the low DCIN POR event.

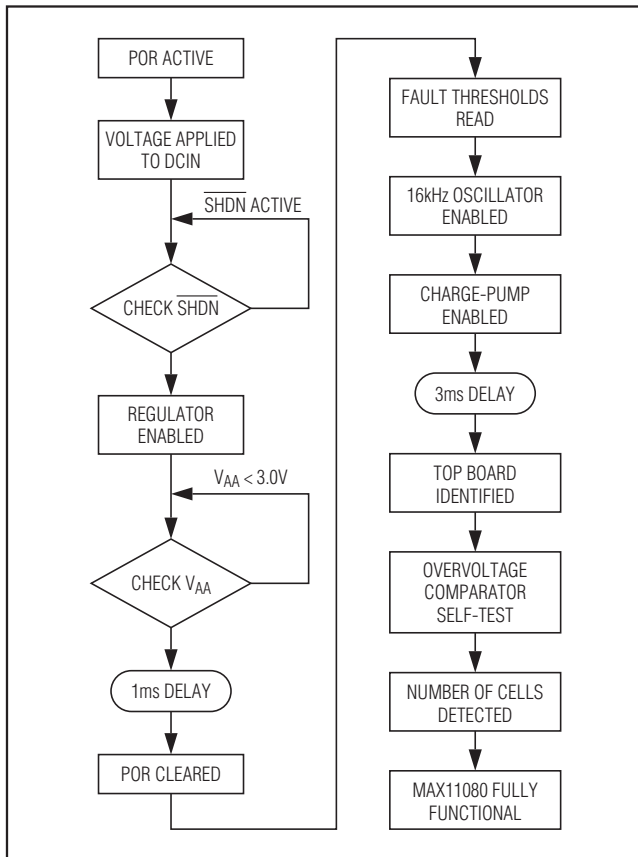


Figure 12. Linear Regulator Power-Up Sequence

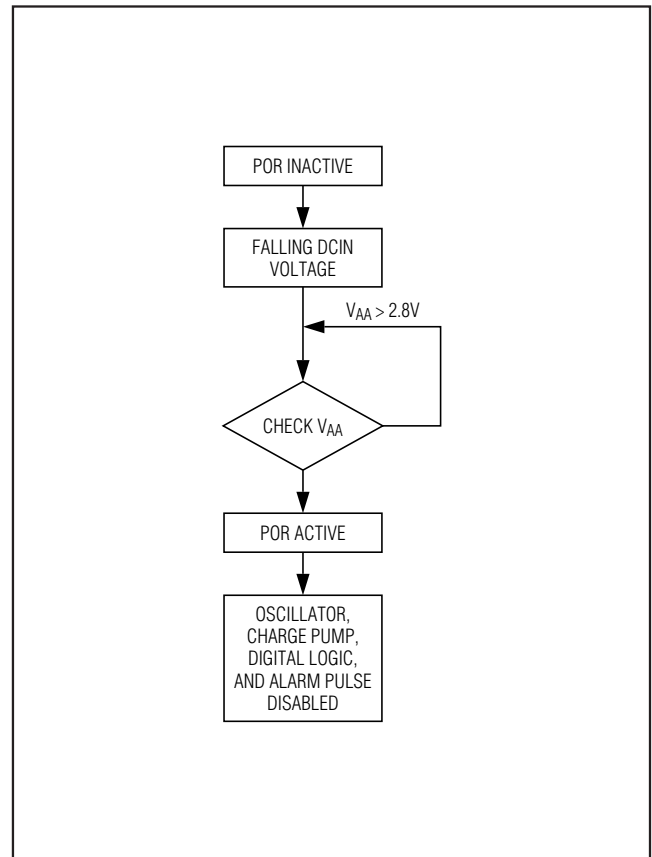


Figure 13. Low DCIN POR Event

12-Channel, High-Voltage Battery-Pack Fault Monitor

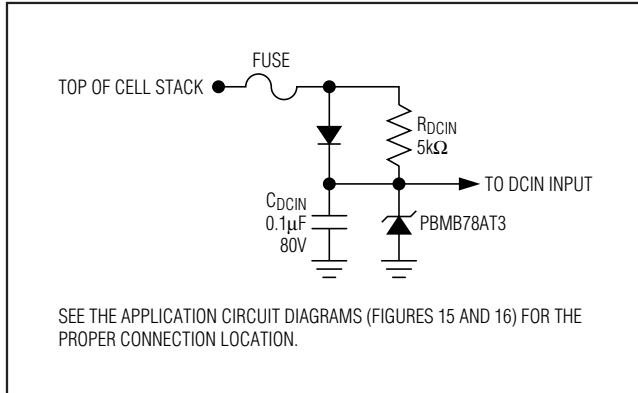


Figure 14. Battery Module Surge and Overvoltage Protection Circuit

DCIN and GND_U Supply Connections

A surge voltage is produced by the electric motor during regenerative braking conditions. The MAX11080 is designed to tolerate an absolute maximum of 80V under this condition. The MAX11080 should be protected against higher voltages with an external voltage suppressor such as the PBMB78AT3 on the DCIN connection point. This protection circuit also helps to reduce power spikes that can occur during the insertion of the battery cells. During negative voltage excursions, the protection circuit stores enough charge to power the regulator through the transient. Figure 14 shows the clamp configuration to protect the DCIN supply input.

The DCIN input contains a comparator circuit to detect an open circuit on this pin for fault-management purposes. Whenever a nominal voltage of two silicon diode drops appears between C12 and DCIN following the power-up sequence, the ALRM_L output is asserted as a fault indication. This voltage drop must appear for at least the delay time set by C_{DLY} to result in a fault. The voltage drop from C12 to DCIN during normal operation should be kept at no more than 0.5V to prevent erroneous tripping of the DCIN open-circuit comparator under worst-case circumstances (lowest silicon diode forward bias voltage). The diode D_{DCIN} is used to supply the transient current demanded at startup by the decoupling circuit. In parallel with this diode, R_{DCIN} provides the supply path during normal operation. It is selected to be 5kΩ so that the maximum voltage drop between C12 and DCIN is about 0.25V with nominal supply currents.

High-power batteries are often used in noisy environments subject to high dV/dt or dI/dt supply noise and EMI noise. For example, the supply noise of a power

inverter driving a high horse-power motor produces a large square wave at the battery terminals, even though the battery is also a high-power battery. Typically, the battery dominates the task of absorbing this noise, since it is impractical to put hundreds of farads at the inverter.

The MAX11080 is designed with several mechanisms to deal with extremely noisy environments. First, the major power-supply inputs that see the full battery-stack voltage are 80V tolerant. This is high enough to handle the large voltage changes on the battery stack that can occur when the batteries transition between charge and discharge conditions. Next, the linear regulator has high PSRR to produce a clean low-voltage power supply for the internal circuitry. This allows DCIN to be connected directly to the stack voltage. Finally, GND_U serves two purposes. It supplies the internal charge pump with its power and acts as the reference ground for the upper alarm communication port. The charge pump creates a secondary low-voltage supply that is referenced to GND_U. Because the level-shifted supply VDD_U is referenced to GND_U, the entire upper alarm communication port glides smoothly on GND_U and it is effectively immune to noise on GND_U. The upper alarm signal is internally shifted down to AGND level where it is processed by the digital logic. There are two connection methods that can be used for GND_U depending on application requirements.

For the top module in a system, or where GND_U cannot be DC-coupled to the next higher module for other reasons, GND_U should be connected to the same location as DCIN. This connection is valid as long as the voltage difference between the top of Stack(n) and the bottom of Stack(n+1) during worst-case conditions does not exceed the margin of the alarm pin signaling levels. When GND_U is not DC-coupled to the far side of the bus bar, it can be AC-coupled to the far side to maintain alarm communication when the bus bar is open-circuit. In that case, the two sides of the AC-coupling capacitor can be at different DC potentials, but the alarm communication signal continues to be passed across the capacitor connection. It is recommended that an AC- or DC-coupled version of GND_U is paired with the alarm signal through the communication bus wiring, possibly by twisted pair wire, for maximum noise immunity and minimum emissions.

The preferred connection to reject noise between modules is when a DC connection can be made from GND_U to AGND of the next module. It is again recommended that the DC-coupled GND_U signal is routed adjacent to the alarm signal as part of the communication bus for maximum noise immunity and minimum emissions.

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

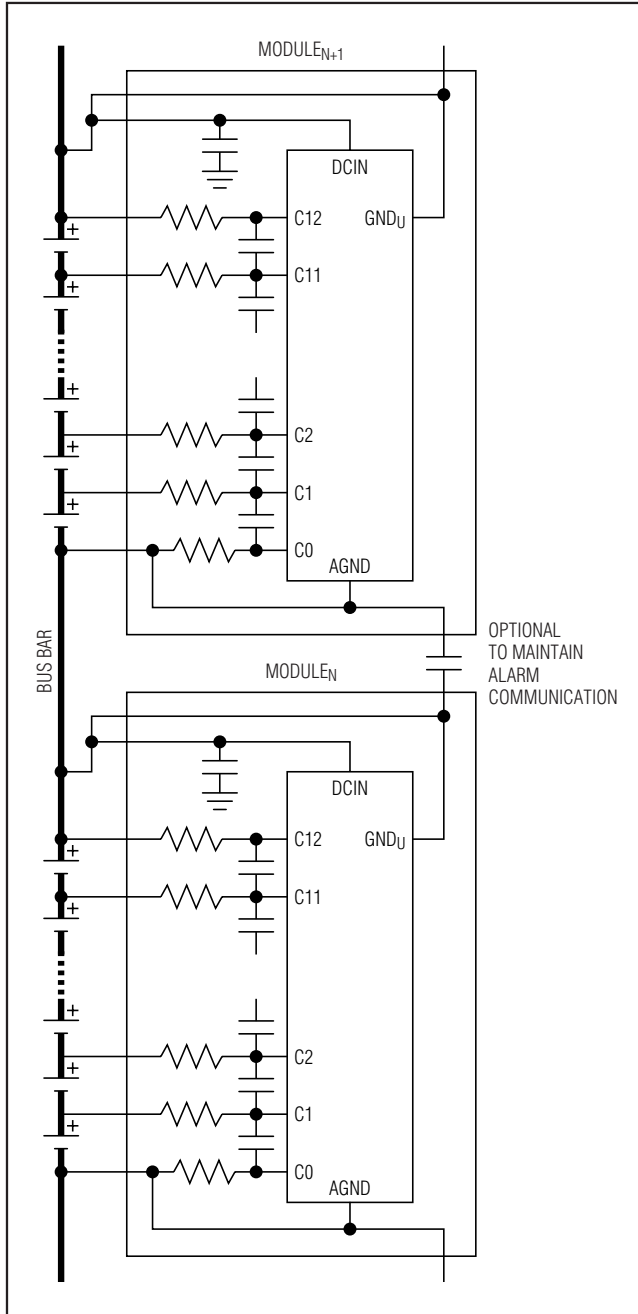


Figure 15. GND_U Connection: AC-Coupled to Next Module, DC-Coupled to Present Module

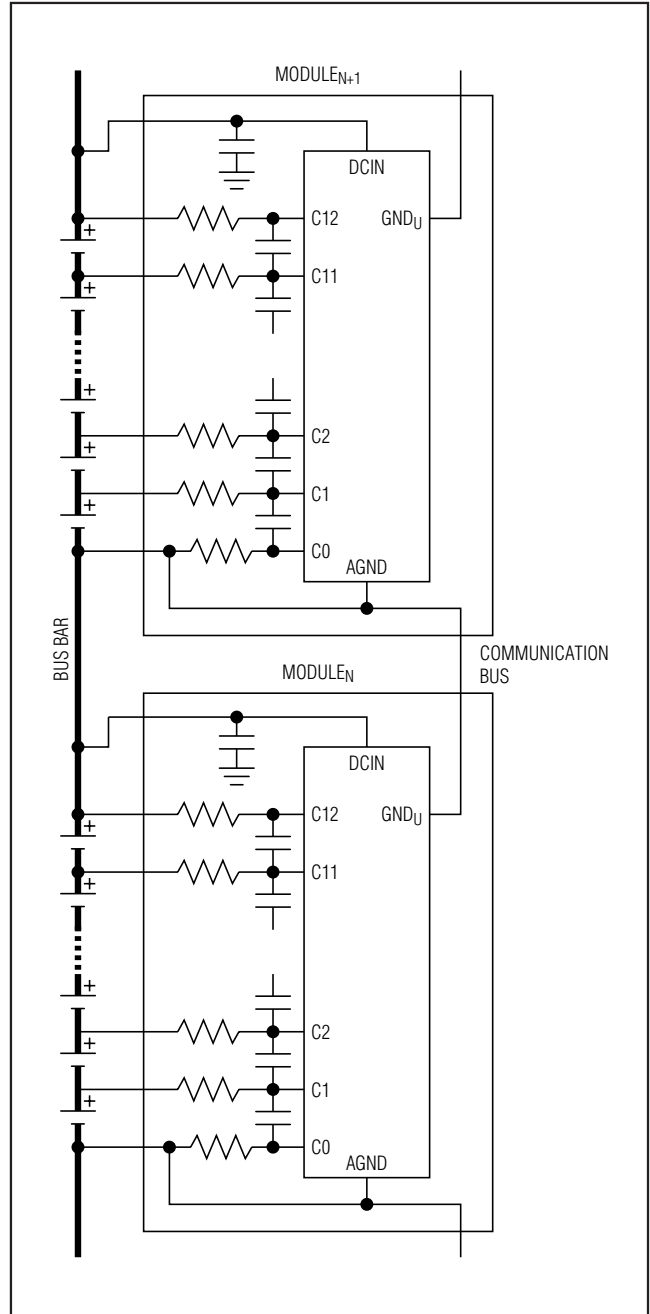


Figure 16. GND_U Connection: DC-Coupled with the Communication Bus

12-Channel, High-Voltage Battery-Pack Fault Monitor

Shutdown Control

The $\overline{\text{SHDN}}$ pin connections of the MAX11080 operate in a manner that allows the shutdown/wake-up command to trickle up through the series of daisy-chained packs. Because the internal linear regulator is powered down during shutdown, the shutdown function must operate when V_{AA} is absent and it, therefore, cannot depend on a Schmitt trigger input. A special low-current, high-voltage circuit is used to detect the state of the $\overline{\text{SHDN}}$ pin. The shutdown pin has a +1.8V minimum threshold for the inactive state. When $\overline{\text{SHDN}} > 1.8\text{V}$, the MAX11080 turns on and begins regulating V_{DDU} and V_{DDL} . If $\overline{\text{SHDN}} < 0.6\text{V}$, the MAX11080 shuts down. For automatic shutdown when the pack is removed from the system, connect a 200k Ω resistor from $\overline{\text{SHDN}}$ to AGND.

Once $\overline{\text{SHDN}}$ is driven high, the power-up sequence follows that described for the internal linear regulator. The $\overline{\text{SHDN}}$ signal of the next higher module should be connected to V_{DDU} through a 20k Ω resistor pullup. This connection ensures that the next module in the daisy chain is enabled as V_{DDU} of the lower module powers up. This action propagates up the daisy chain until the last battery module is enabled. The shutdown of a V_{DDU} supply pulls the connected $\overline{\text{SHDN}}$ pin of the upper module toward GND_L and propagates the shutdown signal up the daisy chain.

A shutdown signal propagated from the first daisy-chain device to the last incurs a certain amount of delay. A deasserted shutdown signal is not propagated to the next higher module until the charge pump has regulated the level-shifted upper port supply, V_{DDU} , to a value greater than the $\overline{\text{SHDN}}$ V_{IH} level. This time depends on both the charge-pump capacitor used and the value of the V_{DDU} decoupling capacitor. A typical time delay of 10ms can be expected from the time the $\overline{\text{SHDN}}$ pin reaches the deasserted state until V_{DDU} reaches its full specified value.

C1 Input Absolute Maximum Rating

The C1 input is limited to $V_{DCIN} - 0.6\text{V}$ above AGND or a maximum of 20V if the $\overline{\text{SHDN}}$ pin is asserted. If an application requires that the 20V restriction be removed during active shutdown, then a 4.0V zener diode can be added from V_{AA} to AGND. This protects V_{AA} and allows the C1 input to go to $V_{DCIN} - 0.6\text{V}$ regardless of the $\overline{\text{SHDN}}$ state. It also allows the differential C1 to C0 voltage to range from -0.3V to +80V.

Cell-Connection Detection

An individual MAX11080 can be connected to as many as 12 series-connected cells. To accommodate configurations with fewer cells, unused cell inputs must be shorted together. The designer can choose which cell inputs

to leave unused. The example application circuits in this document have chosen to populate the uppermost cell position and group the unused inputs just under this cell.

At power-up, the part compares the voltage applied to each cell input with a nominal cell-detection threshold voltage of 0.7V. If the cell voltage is less than the cell-detection threshold, undervoltage detection is disabled for that cell input. If the voltage at the input is 0.7V or greater, undervoltage detection is specified by the state of the UVSEL_- inputs. Overvoltage detection is always enabled for all cell-voltage inputs. The cell-connection detection occurs just before the MAX11080 is fully functional as shown in Figure 12 under "Number of Cells Detected."

TOPSEL Function

The TOPSEL pin is used to indicate to a device whether it is the top device in the daisy-chain stack. The top daisy-chain device is responsible for generating the heartbeat signal at the top of the ALRM_- pin bus. This heartbeat propagates along the chain toward the host. To designate a device as the top device, the TOPSEL pin should be connected to V_{AA} . For all other devices in a daisy chain, this pin should be connected to AGND. The TOPSEL pin has a weak internal pulldown resistor, but this resistor should not be relied upon as the sole means of setting the TOPSEL logic level. The logic level of the TOPSEL pin is not latched internally at startup and is continuously sampled during operation. The ALRM_U input should be connected to GND_U for the top module as good design practice to prevent noise pickup even though the input logic level is ignored.

For the single device application, the device enters the "level" mode when the TOPSEL is connected to AGND. The ALRM_L shows the level of AGND for no alarm state and V_{AA} for alarm state. ALRM_U has to be tied to GND_U for this mode. The following table summarizes the operation of TOPSEL and ALRM_L :

TOPSEL	ALRM_U	ALRM_L	
		No alarm	alarm
0	0	0	1
1	X	Heartbeat	1

Internal Self-Test

The MAX11080 performs an internal self-test during power-up according to the linear regulator power-up flowchart (Figure 12). Each overvoltage comparator is tested for the ability to detect an internally generated overvoltage test condition. This is done by using the ground voltage level as the threshold reference in place of the usual threshold level. Figure 8 shows the connec-

12-Channel, High-Voltage Battery-Pack Fault Monitor

tion for this test-mode compare level. If all comparators can detect the internally generated overvoltage test event, part operation continues. If any comparator fails to detect the internally generated overvoltage test event, a fault is signaled using the ALRM_L pin. The device must be power cycled to retest the comparators and attempt to clear this fault condition.

Failure Mode and Effects Analysis

High-voltage battery-pack systems can be subjected to severe stresses during in-service fault conditions and could experience similar conditions during the manufacturing and assembly process. The MAX11080 is designed with high regard to these potential states.

Open and short circuits at the package level must be readily detected for fault diagnosis and should be tolerated whenever possible. A number of circuits are employed within the MAX11080 specifically to detect such conditions and progress to a known device state. Table 3 summarizes other conditions typical in a normal manufacturing process along with their effect on the MAX11080 device.

See Table 4 for the FEMA analysis of the MAX11080. If the cell voltage is within the monitor range, the heart-beatsignal on the ALRML resumes once the fault condition (either open or short) is removed, unless specified.

Table 3. System Fault Modes

CONDITION	EFFECT	DESIGN RECOMMENDATION
PCB or IC package open or short circuit—no stack load	Refer to the pin-level FMEA analysis spreadsheet available from the factory	The built-in features of the MAX11080 should ensure low FMEA risk in most cases.
Random connection of cells to IC—no stack load	No effect	The series resistors on the cell inputs of the MAX11080 as well as the internal design ensure protection against random power supply or ground connections.
Random connection of modules—no stack load	No effect	Each module is referenced to its neighbor, so no special connection order is necessary.
Random connect/disconnect of communication bus—no stack load; AC- or DC-coupled	Communication from host to the first break in the daisy-chain bus	The level-shifted interface design of the MAX11080 ensures that the $\overline{\text{SHDN}}$, GND _U , and ALRM _U communication bus can be connected at any time with no load.
Random connect/disconnect of communication bus—with stack load; AC- or DC-coupled	Communication from host to the first break in the daisy-chain bus	The level-shifted interface design of the MAX11080 ensures that the $\overline{\text{SHDN}}$, GND _U , ALRM _U communication bus can be connected at any time as long as the power bus is properly connected.
Connect/disconnect module interconnect (bus bar)—no stack load	No effect for DC- or AC-coupled communication bus	A break in the power bus does not cause a problem as long as there is no load on the stack.
Removal/fault of module interconnect (bus bar)—with stack load	No effect for AC-coupled communication bus; device damage for DC-coupled bus	An AC-coupled bus with isolation on the $\overline{\text{SHDN}}$ pin or a redundant bus-bar connection should be used to protect against this case.
Removal/fault of module interconnect (bus bar)—with stack under charge	No effect for AC-coupled communication bus; device damage for DC-coupled bus	An AC-coupled bus with isolation on the $\overline{\text{SHDN}}$ pin or a redundant bus-bar connection should be used to protect against this case.

12-Channel, High-Voltage Battery-Pack Fault Monitor

Table 4. FEMA Analysis (Note 5)

PIN NUMBER	NAME	ACTION	EFFECT
1	DCIN	Open (or Disconnected)	ALRM _L goes high (see Note 6).
		Short to Pin 2	ALRM _L goes high.
2	HV	Open (or Disconnected)	ALRM _L goes high.
		Short to Pin 3	No effect.
3	N.C.	Open (or Disconnected)	No effect.
		Short to Pin 4	No effect.
4	C12	Open (or Disconnected)	<ul style="list-style-type: none"> If open occurs before power-up, the part works as if C12 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C12 to C11 is disabled and is not enabled even if the pin is reconnected. If open occurs after power-up, it is considered a zero voltage input. ALRM_L goes high when the undervoltage is enabled.
		Short to Pin 5	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C12 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C12 to C11 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C12 to C11. ALRM_L goes high when the undervoltage is enabled.
5	C11	Open (or Disconnected)	ALRM _L goes high because it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 6	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C11 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C11 to C10 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C11 to C10. ALRM_L goes high when the undervoltage is enabled.
6	C10	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 7	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C10 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C10 to C9 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C10 to C9. ALRM_L goes high when the undervoltage is enabled.
7	C9	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 8	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C9 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C9 to C8 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C9 to C8. ALRM_L goes high when the undervoltage is enabled.

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

Table 4. FEMA Analysis (Note 5) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
8	C8	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 9	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C8 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C8 to C7 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C8 to C7. ALRM_L goes high when the undervoltage is enabled.
9	C7	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 10	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C7 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C7 to C6 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C7 to C6. ALRM_L goes high when the undervoltage is enabled.
10	C6	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 11	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C6 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C6 to C5 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C6 to C5. ALRM_L goes high when the undervoltage is enabled.
11	C5	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 12	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C5 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C5 to C4 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C5 to C4. ALRM_L goes high when the undervoltage is enabled.
12	C4	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 13	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C4 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C4 to C3 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C4 to C3. ALRM_L goes high when the undervoltage is enabled.

12-Channel, High-Voltage Battery-Pack Fault Monitor

Table 4. FEMA Analysis (Note 5) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
13	C3	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 14	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C3 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C3 to C2 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C5 to C4. ALRM_L goes high when the undervoltage is enabled.
14	C2	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 15	<ul style="list-style-type: none"> If short occurs before power-up, the part works as if C2 does not exist because the internal circuit detects the situation and assumes it is what the application intended to do. The monitoring of C2 to C1 is disabled and is not enabled even if the short is removed. If short occurs after power-up, the situation is treated as a zero voltage input for C2 to C1. ALRM_L goes high when the undervoltage is enabled.
15	C1	Open (or Disconnected)	ALRM _L goes high as it causes an overvoltage to the affected input pair even if the overvoltage is set to the maximum.
		Short to Pin 16	ALRM _L goes high irrespective of whether undervoltage is enabled/disabled and before <i>and</i> after power-up.
16	C0	Open (or Disconnected)	ALRM _L goes high irrespective of whether undervoltage is enabled/disabled and before <i>and</i> after power-up.
		Short to Pin 17	<ul style="list-style-type: none"> ALRM_L goes high if pin 17 is pulled high by V_{AA}. The part consumes a large current as V_{AA} is shorted to AGND (connected to C0). If pin 17 is tied to AGND, there is no effect.
17	UVSEL0	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 7). The effect depends on the intended undervoltage setting.
		Short to Pin 18	<ul style="list-style-type: none"> If pin 17 and pin 18 have the same intended value, there is no effect for the short. If pin 17 and pin 18 have a different setting, the V_{AA} is shorted to AGND. ALRM_L goes low.
18	UVSEL1	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 7). The effect depends on the intended undervoltage setting.
		Short to Pin 19	<ul style="list-style-type: none"> If pin 18 and pin 19 have the same intended value, there is no effect for the short. If pin 18 and pin 19 have a different setting, the V_{AA} is shorted to AGND. ALRM_L goes low.
19	UVSEL2	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 7). The effect depends on the intended undervoltage setting.
		Short to Pin 20	<ul style="list-style-type: none"> If pin 19 and pin 20 have the same intended value, there is no effect for the short. If pin 19 and pin 20 have the different setting, the V_{AA} is shorted to AGND. ALRM_L goes low.

12-Channel, High-Voltage Battery-Pack Fault Monitor

Table 4. FEMA Analysis (Note 5) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
20	OVSEL0	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 7). The effect depends on the intended overvoltage setting.
		Short to Pin 21	<ul style="list-style-type: none"> If pin 20 and pin 21 have the same intended value, there is no effect for the short. If pin 20 and pin 21 have a different setting, the V_{AA} is shorted to AGND. ALRM_L goes low.
21	OVSEL1	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 7). The effect depends on the intended overvoltage setting.
		Short to Pin 22	<ul style="list-style-type: none"> If pin 21 and pin 22 have the same intended value, there is no effect for the short. If pin 21 and pin 22 have a different setting, the V_{AA} is shorted to AGND. ALRM_L goes low.
22	OVSEL2	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 7). The effect depends on the intended overvoltage setting.
		Short to Pin 23	<ul style="list-style-type: none"> If pin 22 and pin 23 have the same intended value, there is no effect for the short. If pin 22 and pin 23 have a different setting, the V_{AA} is shorted to AGND. ALRM_L goes low.
23	OVSEL3	Open (or Disconnected)	The pin defaults to low due to the internal pulldown (see Note 7). The effect depends on the intended overvoltage setting.
		Short to Pin 24	<ul style="list-style-type: none"> If pin 23 is set high, there is no effect for the short. If pin 23 is set low, the V_{AA} is shorted to AGND. ALRM_L goes low.
24	V _{AA}	Open (or Disconnected)	ALRM _L goes high.
		Short to Pin 25	ALRM _L goes low.
25	AGND	Open (or Disconnected)	V _{AA} goes to approximately 100mV and ALRM _L is approximately 0.5V. There is no heartbeat if there is a one before the opening.
		Short to Pin 26	The device is in shutdown mode. ALRM _L is low.
26	$\overline{\text{SHDN}}$	Open (or Disconnected)	The pin is internally pulled down and the device goes to the shutdown mode. ALRM _L is low.
		Short to Pin 27	ALRM _L goes high and stays high even if the short is removed. The internal detect circuit considers this a major failure and the part has to be repowered up to come out of this state.
27	ALRM _L	Open (or Disconnected)	The signal at the ALRM _L cannot be seen by the host.
		Short to Pin 28	ALRM _L goes high and stays high even if the short is removed. The internal detect circuit considers this a major failure and the part has to be repowered up to come out of this state.
28	CD	Open (or Disconnected)	The delay between the fault condition and alarm setting (ALRM _L goes high) goes to the minimum. This means there is almost no delay.
		Short to Pin 29	The delay between the fault condition and alarm setting (ALRM _L goes high) is approximately 4s, which is set by the internal watchdog.

12-Channel, High-Voltage Battery-Pack Fault Monitor

Table 4. FEMA Analysis (Note 5) (continued)

PIN NUMBER	NAME	ACTION	EFFECT
29	AGND	Open (or Disconnected)	No effect.
		Short to Pin 30	No effect.
30	AGND	Open (or Disconnected)	No effect.
		Short to Pin 31	If pin TOPSEL is set high (V_{AA}), it causes the short between V_{AA} and AGND. ALRM _L is low. There is no effect if TOPSEL is set low.
31	TOPSEL	Open (or Disconnected)	If the part is the topmost device in the daisy chain, the ALRM _L is set high as the state of TOPSEL is low (internally pulled down). There are no other effects as the state of the pin stays the same (both low).
		Short to Pin 32	No effect if TOPSEL is set low. If TOPSEL is set high, it causes the short between V_{AA} and AGND and ALRM _L is low.
32	AGND	Open (or Disconnected)	No effect.
		Short to Pin 33	No effect.
33	N.C.	Open (or Disconnected)	No effect.
		Short to Pin 34	No effect.
34	ALRM _U	Open (or Disconnected)	ALRM _U is internally pulled up to VDD _U . There is no effect to the topmost device. Otherwise, the communication of the chain is broken and the alarm signal from the parts close to the topmost device are not passed through. Since ALRM _L is a reflection of ALRM _U , the state of ALRM _L is high for the no-alarm state.
		Short to Pin 35	No effect for the topmost device. Otherwise, the communication of the chain is broken and the alarm signal from the parts close to the topmost are not passed through. Since ALRM _L is a reflection of ALRM _U , the state of ALRM _L is low for the no-alarm state.
35	GND _U	Open (or Disconnected)	The ALRM _L goes high. VDD _U floats down approximately 4V. (See Note 8.)
		Short to Pin 36	The ALRM _L is high. (See Note 8.)
36	VDD _U	Open (or Disconnected)	ALRM _L goes high. HV is approximately 0.4V below DCIN. (See Note 8.)
		Short to Pin 37	ALRM _L goes high. VDD _U is approximately 0.5V lower than GND _U . (See Note 8.)
37	CP-	Open (or Disconnected)	ALRM _L goes high. VDD _U and HV collapse.
		Short to Pin 38	ALRM _L goes high. VDD _U is approximately 0.5V lower than GND _U . (See Note 8.)
38	CP+	Open (or Disconnected)	ALRM _L goes high. VDD _U and HV collapse. (See Note 8.)

Note 5: If the cell voltage is within the monitor range, the heartbeat signal on the ALRML resumes once the fault condition is removed.

Note 6: The voltage level of high is equal to V_{AA} and low is equal to AGND.

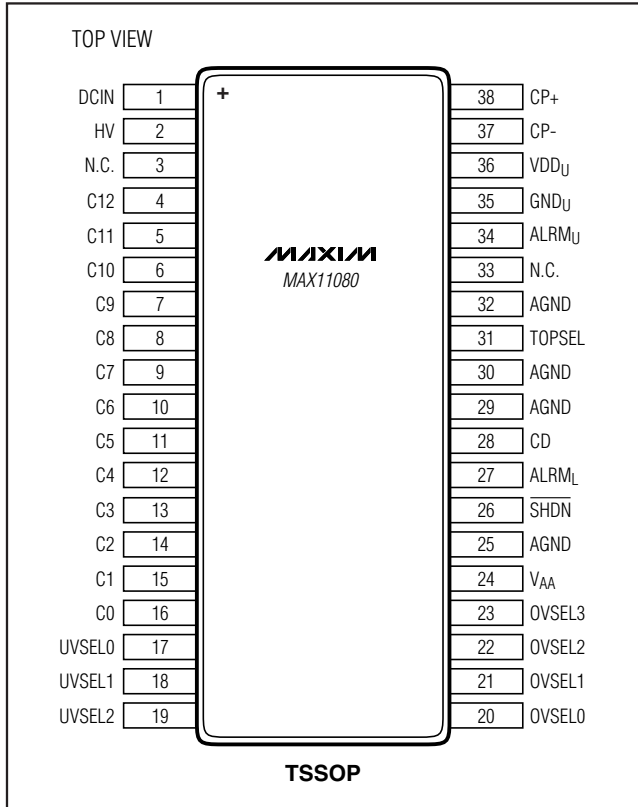
Note 7: Even if the pin has internal pulldown, the pulldown is very weak and the pin should be tied to AGND for logic 0 setting.

Note 8: $VDD_U - GND_U = 3.3 - V$ and $HV - DCIN = 3.6V$ for the typical configuration. When VDD_U and HV collapse, $VDD_U - GND_U \approx 0 - V$ and $HV - DCIN \approx -0.4V$.

12-Channel, High-Voltage Battery-Pack Fault Monitor

MAX11080

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
38 TSSOP	U38-1	21-0081

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