Data Sheet
June 1992

AT&T Microelectronics

ATT1736F/1765F/17128F Serial E² ROM

Features

- Reprogrammable Flash-EECMOS
- 36,288 x 1 bit, 65,536 x 1 bit, and 131072 x 1 bit serial E² ROMs for FPGA configuration
- Designed to store configuration programs for programmable gate arrays
- Daisy-chain configuration support for multiple FPGAs
- Cascadable to provide more memory for additional configurations
- Cascadable to support future higher-density arrays
- Stores configurations for single or multiple FPGAs
- Low-power EECMOS process
- 8-pin, plastic DIP
- Programming support from leading programmer manufacturers
- Pin-for-pin functional replacements for *Xilinx XC1700* devices

Description

The ATT1736F/1765F/17128F Serial E² Configuration ROM (SeROM) devices serve as easy-to-use, cost-effective, reprogrammable, and nonvolatile configuration memories for the AT&T 3000 family and ORCA Series of field-programmable gate arrays (FPGAs). SeROM devices of all sizes are currently available in the industry-standard, 8-pin, plastic, skinny dual-in-line package (DIP).

The ATT1700 SeROM devices are pin-for-pin functional replacements for normal read operation for the *Xilinx XC1700* family of serial ROM devices. The AT&T 1700 SeROM family can be programmed by a variety of commercially available programming units fielded by qualified third-party programmable device support of vendors such as BP Microsystems, Data I/O, and Stag Microsystems. A listing of qualified (AT&T tested and verified) third-party programming platforms is scheduled to be available by the fourth quarter of 1992.

For multiple FPGA devices connected in a daisy-chain configuration, or for extremely large FPGA devices requiring large configuration memories, cascaded SeROM devices offer an almost unlimited memory capacity.

Since the AT&T SeROM family is manufactured by using proprietary AT&T (Flash-EECMOS) non-destructive programming technology, an individual SeROM can be reliably reprogrammed a minimum of 10 times†. A SeROM that has been reprogrammed 10 or fewer times† is designed to meet all published data book specifications.

In a design environment where long-term data retention and tolerance to harsh environments are not at issue, SeROMs can typically be reprogrammed **hundreds** of times. Programmed information is not lost upon the removal, or momentary interruption, of operating voltage at the SeROM's power supply connections. The SeROM is truly nonvolatile and is projected to have a data-retention period in excess of 10 years*.

Unlike other ROM/PROM technologies, Flash-EECMOS technology offers the benefits of 100% testability, high-speed operation, low power, and split-second erasure for high-reliability reprogramming. The AT&T SeROM device offers a combination of flexibility, reliability, and bit capacity not available with other FPGA-specific data storage mechanisms.

* These figures are based upon preproduction analysis. Actual production figures may vary.

Description (continued)

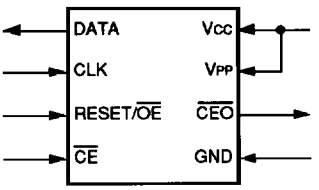


Figure 1. ATT1736F/1765F/17128F Functionality During READ

Pin Information

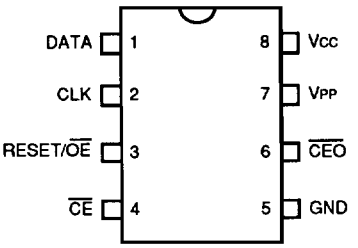


Figure 2. 8-Pin DIP Diagram

Table 1. Pin Descriptions

Pin #	Symbol	Type	Name/Function
1	DATA	O	**3-State DATA Out for Reading.** Output pin for normal read operation.
2	CLK	I	**Clock Input.** Used to increment the internal address and bit counters for normal read operation.
3	RESET/ OE	I	**RESET/Output Enable.** A low level on both the CE and RESET/ OE inputs enables the data output driver. A high level on RESET/ OE resets both the address and bit counters. The logic polarity of this input is programmable as either RESET/ OE or RESET /OE. This document describes the pin as RESET/ OE .
4	CE	I	**Chip Enable.** A low level on both CE and RESET/ OE enables the data output driver. A high level on CE disables both the address and bit counters and forces the device into a low-power mode. Used for device selection.
5	GND	—	**Ground Pin.**
6	CEO	O	**Chip Enable Out.** This signal is asserted low on the clock cycle following the last bit read from the memory. It will stay low as long as CE and OE are both low. It will then follow CE , but if RESET/ OE goes high, CEO will stay high until the entire ROM is read again.
7	VPP	I	**Programming Voltage Supply.** Must be connected directly to Vcc for normal read operation.
8	Vcc	I	**+5 V Power Supply.**

Functional Description

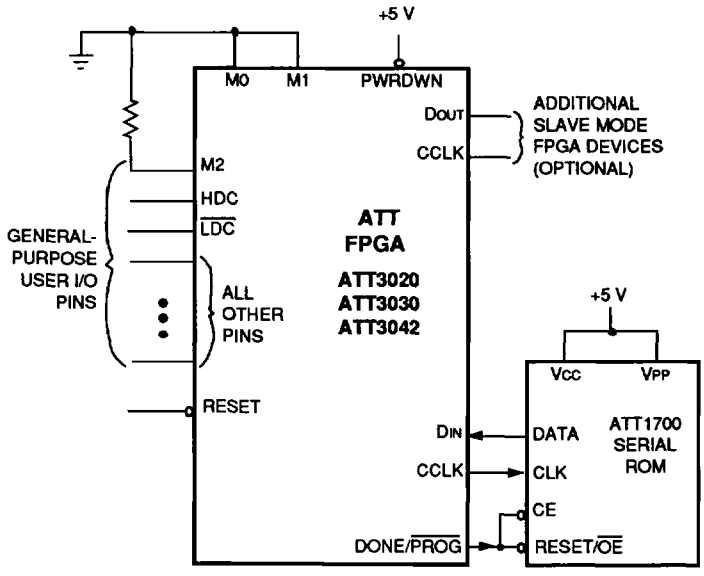


Figure 3. Master Serial Mode Configuration

FPGA Master Serial Mode Summary

The I/O and logic functions of the AT&T programmable gate array, and their associated interconnections, are established by a configuration program. The program is loaded either automatically upon powerup, or on command, depending on the state of the three FPGA mode pins. In master mode, the field-programmable gate array automatically loads the configuration program from an external memory. The serial configuration ROM has been designed for compatibility with the master serial mode.

Upon powerup or upon reconfiguration, an FPGA will enter master serial mode whenever all three of the FPGA's mode select pins are low (M0 = 0, M1 = 0, M2 = 0). Data is read from the serial E^2 configuration ROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master serial mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure the FPGA. Data from the serial configuration ROM is read sequentially, accessed via the internal address and bit counters, which are incremented on every valid rising edge of CCLK.

Programming the FPGA with Counters Reset upon Completion

Figure 3 illustrates the connections between an FPGA and its SeROM. The DATA line from the SeROM is connected to the DIN input of the FPGA. The CCLK output from the FPGA is connected to the CLK input of the SeROM. At powerup or upon reconfiguration, the DONE/ PROG signal goes low (pulled low by the FPGA at reset or by external circuitry for reconfiguration), enabling the SeROM and its DATA output.

Functional Description (continued)

Programming the FPGA with Counters Reset upon Completion (continued)

During the configuration process, CCLK will clock data out of the SeROM on every rising clock edge. At the completion of configuration, the DONE/ PROG signal will go high and reset the internal address counters of the SeROM.

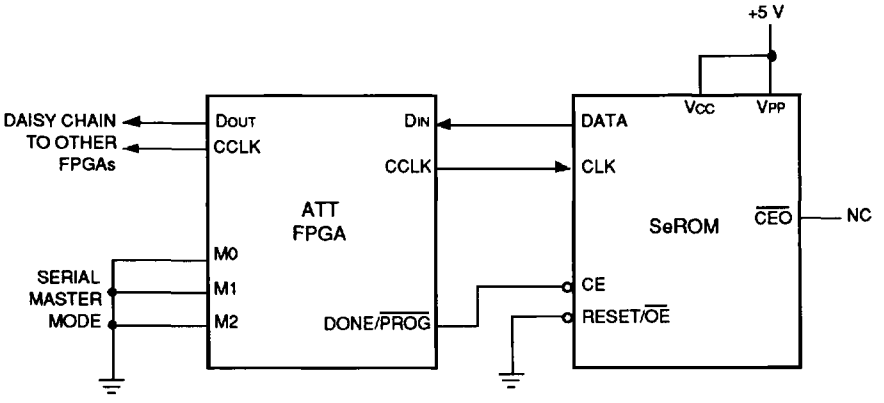
If the user-programmable, dual-function DIN and CCLK pins are used only for the configuration process, they should be programmed on the FPGA so that no nodes are floating or in contention. For example, both DIN and CCLK can be programmed as output highs during normal operation. An alternate method is to program both DIN and CCLK as inputs, with external pull-up resistors attached.

If DIN and CCLK are used for another function after configuration, the user must avoid contention. The low during configuration (LDC) pin can be used to control the SeROM's CE and OE inputs to disable the SeROM's DATA pin, one clock cycle before DONE/ PROG is active.

If the FPGA is reprogrammed after initial powerup, note that the FPGA requires several microseconds to respond after the DONE/ PROG pin is pulled low. In this case, the LDC pin can be used instead of the DONE/ PROG pin to control the SeROM.

Programming the FPGA with Counters Unchanged upon Completion

When multiple FPGA configurations for a single FPGA are stored in a serial configuration ROM, the OE pin of the SeROM should be tied low as illustrated in Figure 4. Upon powerup, the internal address counters will be reset and configuration will begin with the first program stored in memory. Since the OE pin is held low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE/ PROG line is pulled low and configuration begins at the last value of the address counters.



Notes:
If M2 is tied directly to ground, it should be programmed as an input during operation.

If the FPGA is reset during configuration, it will abort back to initialization state. DONE/ PROG will not go high, so an external signal is required to reset the ATT1700 counters.

Figure 4. Address Counters Not Reset

Functional Description (continued)

Cascading SeROMs

For multiple FPGAs configured in a daisy chain, or for future FPGAs requiring larger configuration memories, cascaded SeROMs provide additional memory.

After the last bit from the first SeROM is read, the SeROM asserts its CEO output low and disables its own DATA line. The next SeROM recognizes the low level on its CE input and enables its own DATA output. (See Figure 5.)

After configuration is complete, the address counters of all of the cascaded SeROMs will be reset when DONE/ PROG output from the FPGA goes high, forcing the RESET/ OE on each SeROM to go high.

If the address counters are not reset upon completion, then the OE inputs can be tied to ground, as illustrated in Figure 4.

To reprogram the FPGA with another program, the DONE/ PROG line goes low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.

The DONE/ PROG signal is an open collector type of output and may be bused. Extremely large, cascaded serial memories in some systems may require additional logic if the rippled chip enable is too slow to activate successive SeROMs.

Standby Mode

The ATT1700 enters a low-power standby mode whenever CE is asserted high. In this mode, the SeROM consumes less than 0.5 mA of current. The output remains in a high-impedance state regardless of the state of the RESET/ OE input.

RESET/ OE Polarity

The ATT1700 enables the user to choose the reset/output enable polarity as either RESET/ OE or RESET /OE. The PROM programmer software prompts the user for the desired polarity.

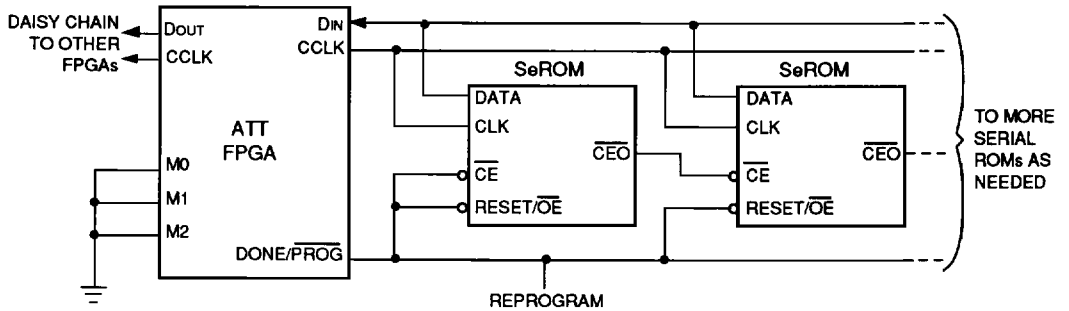


Figure 5. Cascading SeROMs

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	125	°C
Soldering Temperature (10 s)	T_{SOL}	—	260	°C
Supply Voltage	V_{CC}	–0.5	7.0	V
Input Voltage	V_{IN}	–0.5	V_{CC} + 0.5	V
Voltage Applied to 3-state Output	V_{TS}	–0.5	V_{CC} + 0.5	V

Electrical Characteristics

Table 2. dc Characteristics

Parameter	Symbol	Min	Max	Unit
Supply Voltage Relative to GND:				
Commercial/Industrial	V_{CC}	4.5	5.5	V
(–40 °C to +85 °C)	V_{PP}*	4.5	5.5	V
Input Voltage:				
Low	V_{IL}	0	0.8	V
High	V_{IH}	2.0	V_{CC}	V
Output Voltage:				
Low	V_{OL} (I_{OL} = 4 mA)	—	0.32	V
High	V_{OH} (I_{OH} = –4 mA)	3.86	—	V
Supply Current:				
Active Mode	I_{CCA} (I_{CC} + I_{PP})	—	10	mA
Standby Mode	I_{CCS} (I_{CC} + I_{PP})	—	0.5	mA
Input or Output Leakage Current	I_L	–10	10	µA

* During normal read operation, V_{PP} must be connected to V_{CC}.

Timing Characteristics

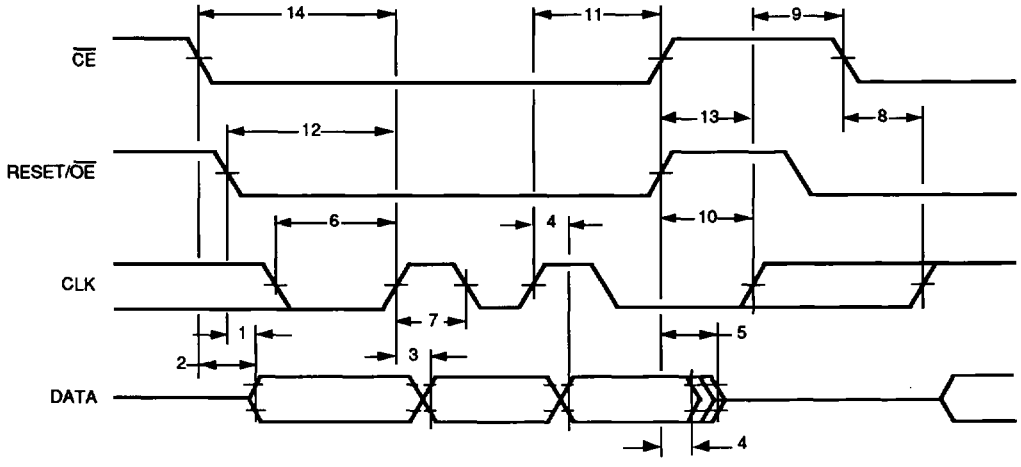


Figure 6. ac Characteristics 1

Table 3. ac Characteristics

Reference Number	Symbol	Parameter	Min	Max	Unit
1	toe	$\overline{OE}$ to Data Delay	—	100	ns
2	tce	$\overline{CE}$ to Data Delay	—	250	ns
3	tcac	CLK to Data Delay	—	400	ns
4	toh	Data Hold from $\overline{CE}$, $\overline{OE}$, or CLK	0	—	ns
5	tdf	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay	—	50	ns
6	tlc	CLK Low Time	200	—	ns
7	thc	CLK High Time	200	—	ns
8	tscel	$\overline{CE}$ Low Setup Time to CLK*	100	—	ns
9	thcel	$\overline{CE}$ High Hold Time to CLK†	0	—	ns
10	thoe	$\overline{OE}$ High Time ($\overline{CE}$ can be high or low)‡	100	—	ns
11	thcbh	$\overline{CE}$ Low Hold Time to CLK*	100	—	ns
12	tsre	$\overline{OE}$ Setup Time to CLK§	100	—	ns
13	tsceh	$\overline{CE}$ High Setup Time to CLK†	100	—	ns
14	tscel1	$\overline{CE}$ Low Setup Time to First CLK§	250	—	ns

* Guarantees counters will change.
† Guarantees counters will not change.
‡ Guarantees counters are reset.
§ Guarantees first bit access.

Timing Characteristics (continued)

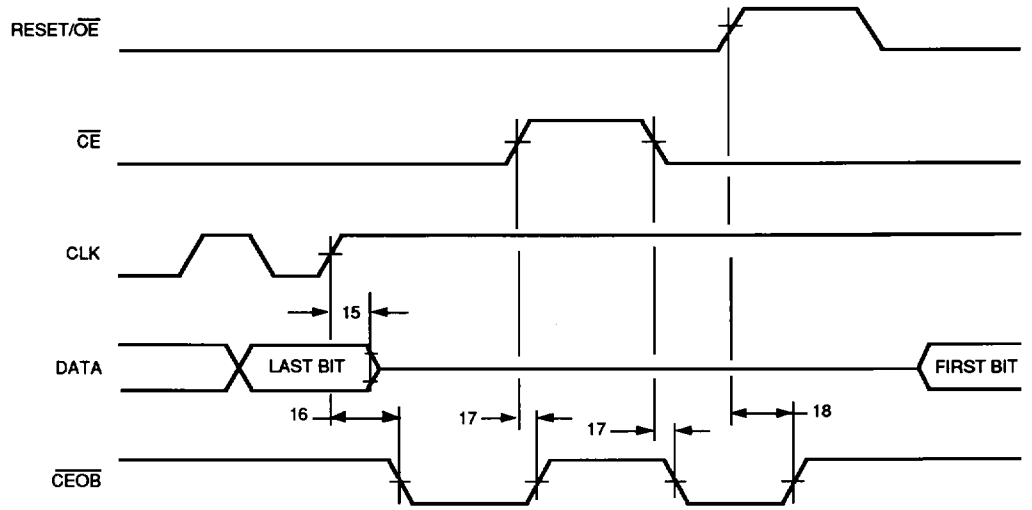
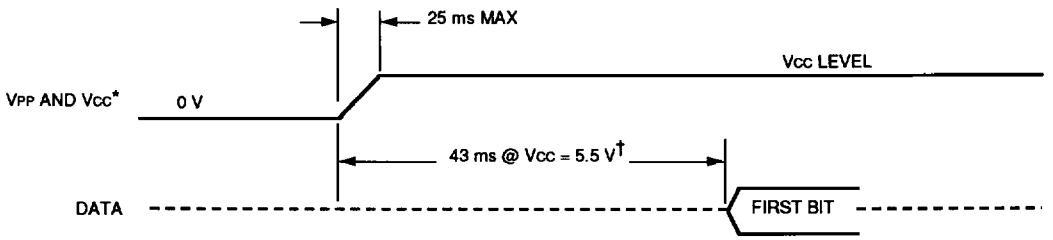


Figure 7. ac Characteristics 2

Table 4. ac Characteristics

Reference Number	Symbol	Parameter	Min	Max	Unit
15	tcdf	CLK to Data Disable Delay	—	40	ns
16	tock	CLK to $\overline{CEO}$ Delay	—	100	ns
17	toce	$\overline{CE}$ to $\overline{CEO}$ Delay	—	100	ns
18	tooe	$\overline{OE}$ to $\overline{CEO}$ Delay	—	100	ns



* VCC and VPP are tied together during a normal read operation.
† First bit data is not valid before 43 ms after powerup.

Figure 8. Powerup