TSM2314

SOT-23

Pin Definition:
1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
20	33 @ V_{GS} = 4.5V	4.9
	40 @ V_{GS} = 2.5V	4.4
	100 @ V_{GS} = 1.8V	2.9

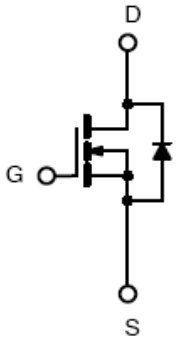
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM2314CX RF	SOT-23	3Kpcs / 7” Reel

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current, V_{GS} @4.5V.		I_D	4.9	A
Pulsed Drain Current, V_{GS} @4.5V		I_{DM}	15	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	1.0	A
Maximum Power Dissipation	Ta = 25°C	P_D	1.25	W
	Ta = 75°C		0.8	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JF}$	75	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	120	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

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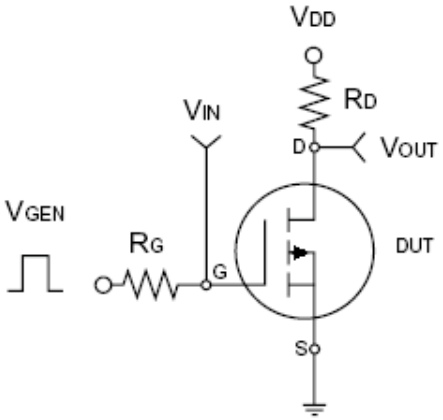
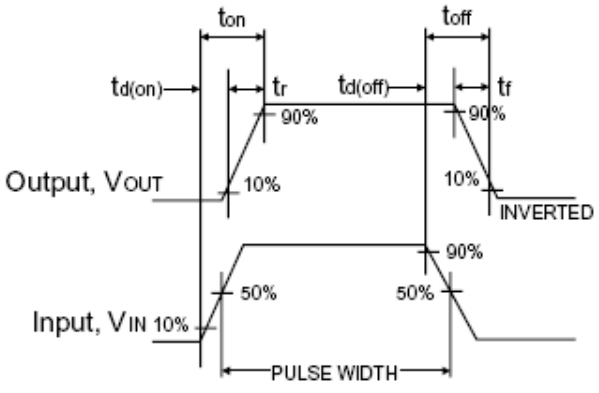
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	0.45	--	1	V
Gate Body Leakage	V_{GS} = ±4.5V, V_{DS} = 0V	I_{GSS}	--	--	±1.5	μA
Zero Gate Voltage Drain Current	V_{DS} = 16V, V_{GS} = 0V	I_{DSS}	--	--	1.0	μA
On-State Drain Current	V_{DS} ≥ 10V, V_{GS} = 4.5V	$I_{D(ON)}$	15	--	--	A
Drain-Source On-State Resistance	V_{GS} = 4.5V, I_D = 4.9A	$R_{DS(ON)}$	--	27	33	mΩ
	V_{GS} = 2.5V, I_D = 4.4A		--	33	40	
	V_{GS} = 1.8V, I_D = 2.9A		--	80	100	
Forward Transconductance	V_{DS} = 15V, I_D = 5.0A	g_{fs}	--	40	--	S
Diode Forward Voltage	I_S = 1.0A, V_{GS} = 0V	V_{SD}	--	0.8	1.2	V
Dynamic[b]						
Total Gate Charge	V_{DS} = 10V, I_D = 5.0A, V_{GS} = 4.5V	Q_g	--	11	14	nC
Gate-Source Charge		Q_{gs}	--	1.5	--	
Gate-Drain Charge		Q_{gd}	--	2.1	--	
Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	900	--	pF
Output Capacitance		C_{oss}	--	140	--	
Reverse Transfer Capacitance		C_{rss}	--	100	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = 10V, R_L = 10Ω, I_D = 1A, V_{GEN} = 4.5V, R_G = 6Ω	$t_{d(on)}$	--	0.53	0.8	nS
Turn-On Rise Time		t_r	--	1.4	2.2	
Turn-Off Delay Time		$t_{d(off)}$	--	13.5	20	
Turn-Off Fall Time		t_f	--	5.9	9	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



Switching Test Circuit



Switchin Waveforms