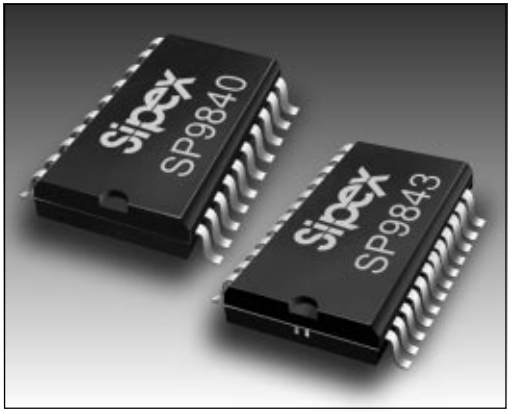
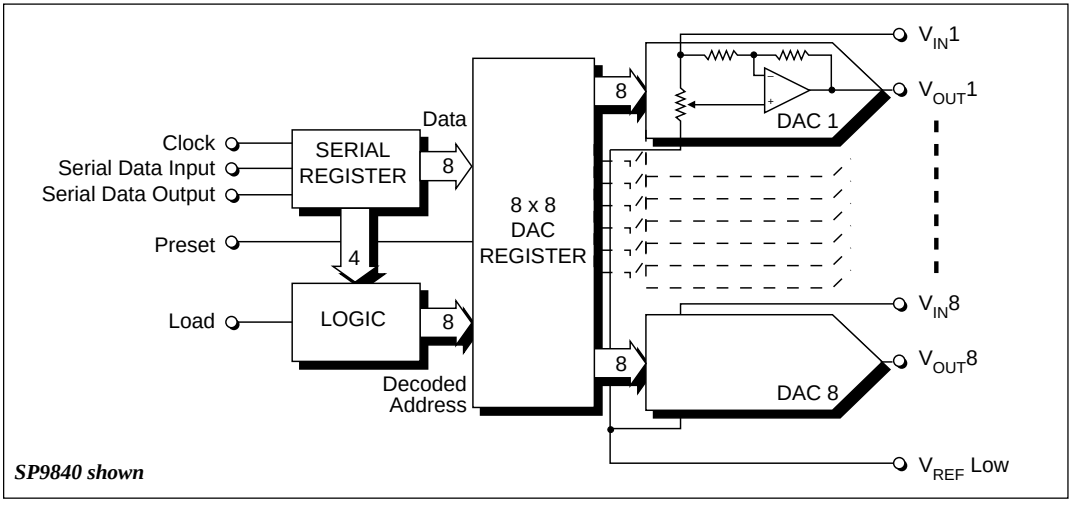
8-Bit Octal, 4-Quadrant Multiplying, BiCMOS DAC

- Replaces 8 Potentiometers and 8 Op amps
- Operates from Single +5V Supply
- 5 MHz 4-Quadrant Multiplying Bandwidth
- Eight Inputs/Eight Outputs (SP9840) Four Inputs/Eight Outputs (SP9843)
- 3-Wire Serial Input
- 0.8MHz Data Update Rate
- +3.25V Output Swing
- Midscale Preset
- Programmable Signal Inversion
- Low 70mW Power Dissipation (9mW/DAC)



DESCRIPTION…

The **SP9840** and **SP9843** are general purpose octal DACs in a single package. The **SP9840** features eight individual reference inputs, while the **SP9843** provides four pair of voltage reference inputs. Both parts feature 5MHz bandwidth, four–quadrant multiplication, and a three–wire serial interface. Other features include midscale preset, programmable signal inversion and low power dissipation from a single +5V supply. Devices are available in commercial and industrial temperature ranges.

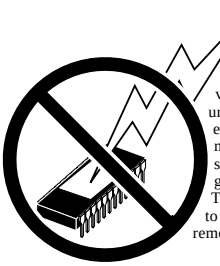


SP9840 shown

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{DD} to GND ..... -0.3V, +7V
$V_{IN}X$ to GND ..... V_{DD}
$V_{REF}L$ to GND ..... V_{DD}
$V_{OUT}X$ to GND ..... V_{DD}
Short Circuit $I_{OUT}X$ to GND ..... Continuous
Digital Input & Output Voltage to GND ..... V_{DD}
Operating Temperature Range
Commercial ..... 0°C to +70°C
Extended Industrial ..... -40°C to +85°C
Maximum Junction Temperature (T_J max) ..... +150°C
Storage Temperature ..... -65° to 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_J max - T_A)/8JA
Thermal Resistance 8_{JA}
P-DIP ..... 57°C/W
SOIC-24 ..... 70°C/W



CAUTION:
While all input and output pins have internal protection networks, these parts should be considered ESD (ElectroStatic Discharge) sensitive devices. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(V_{DD} = +5V, All $V_{IN}X$= 0V, $V_{REF}L$ = 1.625V, T_A = 25° C for commercial–grade parts; $T_{MIN} \le T_A = T_{MAX}$ for industrial–grade parts; specifications apply to all DAC's unless noted otherwise.)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SIGNAL INPUTS					
Input Voltage Range	0		3.25	V	V_{DD} = 4.75V, V_{REFL} = 1.625V
Input Resistance					D = $2B_H$, Code Dependent
SP9840	3.1	6.2		kΩ	
SP9843	1.55	3.1		kΩ	
Input Capacitance					Note 1
SP9840		19	30	pF	
SP9843		38	60	pF	
V_{REFL} Resistance	0.68	1.3		kΩ	Note 1 and 2
V_{REFL} Capacitance		190	250	pF	Note 1
DIGITAL INPUTS					
Logic High	2.4			V	
Logic Low			0.8	V	
Input Current			±10	µA	
Input Capacitance			8	pF	
Input Coding		Offset Binary			Note 3
STATIC ACCURACY					
Resolution		8		Bits	
Integral Nonlinearity		±0.75	±1.5	LSB	Note 4
Differential Nonlinearity		±0.3	±1	LSB	Note 4
Half-Scale Output Voltage	1.600	1.625	1.650	V	$\overline{PR}$ = LOW, V_{REFL} = 1.625V
Minimum Output Voltage		20	100	mV	D=FF_H; I_{SINK} = 0.1mA
Output Voltage Drift		25		µV/°C	$\overline{PR}$ = LOW
DYNAMIC PERFORMANCE					
Multiplying Gain Bandwidth	3	5		MHz	V_{IN}(X) = 100mV_{P-P} + 1.625V dc
Slew Rate					Measured 10% to 90%
Positive	3.0	7.9		V/µs	ΔV = 3.2V
Negative	–3.0	–8.3		V/µs	ΔV = –3.2V
Total Harmonic Distortion		0.003		%	V_{IN}(X) = 3V_{P-P} +1.625V dc, D=FF_H; 1KHz, f_{LP}=80KHz
Output Settling Time		0.7		µs	±1 LSB Error Band
Crosstalk	60	70		dB	Note 5
Digital Feedthrough		6		nVs	D = 0_H to FF_H
Wideband Noise		42.5		µVrms	V_{OUT} = 3.25V, 400Hz to 80kHz
SINAD		89		dB	V_{IN}(X) = 3V_{P-P} +1.625V dc, D=FF_H; 1KHz, f_{LP}=80KHz
Digital Crosstalk		6		nVs	Note 6

SPECIFICATIONS (continued)

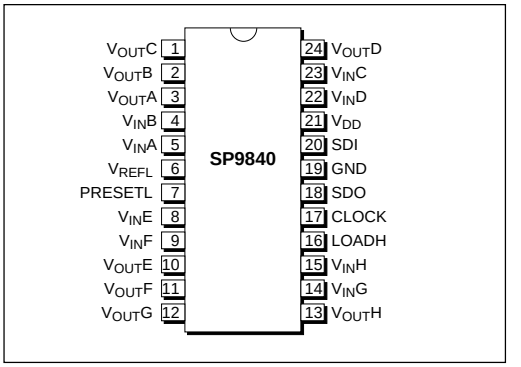
V_{DD} = +5V, All V_{IN}X= +0V, V_{REF}L = 1.625, T_A = 25° C for commercial–grade parts; $T_{MIN} \le T_A = T_{MAX}$ for industrial–grade parts; specifications apply to all DAC's unless noted otherwise.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DAC OUTPUTS					
Voltage Range	0		V_{DD} – 1.5	V	R_L = 5kΩ, V_{DD} = 4.75V
Output Current	±10	±15		mA	Note 7
Capacitive Load		47,000		pF	No Oscillation
DIGITAL OUTPUT					
Logic High	3.5			V	I_{OH} = –0.4mA
Logic Low			0.4	V	I_{OL} = 1.5mA
POWER REQUIREMENTS					
Power Supply Range	4.75	5.00	5.25	V	To rated specifications
Positive Supply Current		14		mA	$\overline{PR}$ = LOW
Power Dissipation		70		mW	$\overline{PR}$ = LOW
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range					
Commercial	0		+70	°C	
Industrial	–40		+85	°C	
Storage Temperature Range	–65		+150	°C	
Package					
SP9840N	24–pin, 0.3" Plastic DIP				
SP9840S	24–pin 0.3" SOIC				
SP9843S	20–pin, 0.3" SOIC				Note 8

Notes:

1. Code dependent
2. All $V_{IN}(x)$ = GND; D = 55_H
3. Offset binary refers to the output voltage with respect to the signal ground at V_{REFL}. For a positive $V_{IN}(x)$, the output will increase from negative fullscale to V_{REFL} to positive (fullscale–1 LSB) as the input code is incremented from 0 to 128 to 255. Note that when $V_{IN}(x)$ is tied to ground and V_{REFL} is driven to +1.625V, as in the production tests above, then the resulting DC at $V_{OUT}(x)$ will decrease from +2V_{REFL} to V_{REFL}/128 as the code is increased from 00_H to FF_H, due to the $V_{IN}(x)$ input being tied negative with respect to V_{REFL}.
4. The op amp limits linearity for V_{OUT} <100mV. When $V_{IN}(x)$ is driven above ground such that the output voltage remains above 100mV, then the linearity specifications apply to all codes. For V_{REFL}=1.625V, and $V_{IN}(x)$=GND, codes 248 through 255 are not included in differential or integral linearity tests. Integral and differential linearity are computed with respect to the best fit straight line through codes 0 through 248.
5. SP9840 is measured between adjacent channels, F=100kHz. SP9843 is measured between adjacent pairs, F=100kHz.
6. SP9843 only; measured between channels with shared input; D = $7F_H$ to 80_H
7. ΔV_{OUT} < 10mV, V_{REFL} = 1.625V, $\overline{PR}$ = LOW.
8. For plastic DIP, consult factory

SP9840 PINOUT



Pin 1 — $V_{OUT}C$ — DACC Voltage Output.

Pin 2 — $V_{OUT}B$ — DACB Voltage Output.

Pin 3 — $V_{OUT}A$ — DACA Voltage Output.

Pin 4 — $V_{IN}B$ — DAC B Reference Voltage Input.

Pin 5 — $V_{IN}A$ — DAC A Reference Voltage Input.

Pin 6 — $V_{REF}L$ — DAC Reference Voltage Input Low, common to all DACs.

Pin 7 — PRESETL — Preset Input; active low; all DAC registers forced to 80_H.

Pin 8 — $V_{IN}E$ — DAC E Reference Voltage Input.

Pin 9 — $V_{IN}F$ — DAC F Reference Voltage Input.

Pin 10 — $V_{OUT}E$ — DACE Voltage Output.

Pin 11 — $V_{OUT}F$ — DACF Voltage Output.

Pin 12 — $V_{OUT}G$ — DACG Voltage Output.

Pin 13 — $V_{OUT}H$ — DACH Voltage Output.

Pin 14 — $V_{IN}G$ — DACG Reference Voltage Input.

Pin 15 — $V_{IN}H$ — DACH Reference Voltage Input.

Pin 16 — LOADH — Load DAC Register Strobe; active high input that transfers the data bits from the Serial Input Register into the decoded DAC Register. Refer to Table 1.

Pin 17 — CLOCK — Serial Clock Input; positive-edge triggered.

Pin 18 — SDO — Serial Data Output; active totem-pole output.

Pin 19 — GND — Ground.

Pin 20 — SDI — Serial Data Input.

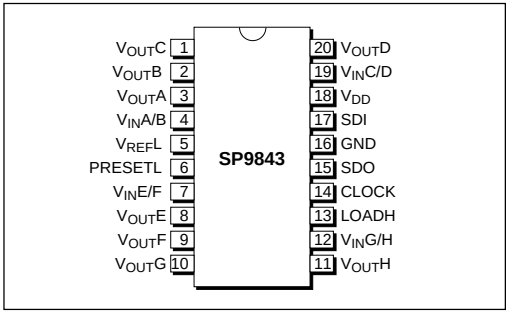
Pin 21 — V_{DD} — Positive 5V Power Supply.

Pin 22 — $V_{IN}D$ — DACD Reference Voltage Input.

Pin 23 — $V_{IN}C$ — DACC Reference Voltage Input.

Pin 24 — $V_{OUT}D$ — DACD Voltage Output.

SP9843 PINOUT



Pin 1 — $V_{OUT}C$ — DACC Voltage Output.

Pin 2 — $V_{OUT}B$ — DACB Voltage Output.

Pin 3 — $V_{OUT}A$ — DACA Voltage Output.

Pin 4 — $V_{IN}A/B$ — DACA and B Reference Voltage Input.

Pin 5 — $V_{REF}L$ — DAC Reference Voltage Input Low, common to all DACs.

Pin 6 — PRESETL — Preset Input; active low; all DAC registers forced to 80_H.

Pin 7 — $V_{IN}E/F$ — DAC E and F Reference Voltage Input.

Pin 8 — $V_{OUT}E$ — DACE Voltage Output.

Pin 9 — $V_{OUT}F$ — DACF Voltage Output.

Pin 10 — $V_{OUT}G$ — DACG Voltage Output.

Pin 11 — $V_{OUT}H$ — DACH Voltage Output.

Pin 12 — $V_{IN}G/H$ — DACG and H Reference Voltage Input.

Pin 13 — LOADH — Load DAC Register Strobe; active high input that transfers the data bits from the Serial Input Register into the decoded DAC Register. Refer to Table 1.

Pin 14 — CLOCK — Serial Clock Input; positive-edge triggered.

Pin 15 — SDO — Serial Data Output; active totem-pole output.

Pin 16 — GND — Ground.

Pin 17 — SDI — Serial Data Input.

Pin 18 — V_{DD} — Positive 5V Power Supply.

Pin 19 — $V_{IN}C/D$ — DACC and D Reference Voltage Input.

Pin 20 — $V_{OUT}D$ — DACD Voltage Output.

SP9840/SP9843
Theory of Operation

Each of the eight channels of the **SP9840/9843** can be used for signal reconstruction, as a programmable DC source, or as a programmable signed attenuator of –1 to +0.992 times a multiplying AC reference input. The rugged wideband output amplifiers provide both current sink and source capability to DC applications, even into difficult loads. The DC source mode mimics the functionality of a programmable trimpot, with the added benefit of a low–impedance buffered output. The amplifier's bandwidth and high open loop gain allow use in programmable signed attenuator applications where even low–distortion, high resolution signals, such as audio, must be gated on and off, programmable phase shifted by 0° or 180° or gain controlled over a –42 to 0dB range at either phase.

Each channel consists of a voltage–output DAC, realized using CMOS switches and thin–film resistors in an inverted R–2R configuration. Each DAC drives the positive terminal of an op amp, configured for a gain of –1 to +1 using equal value thin–film feedback and gain–setting resistors. Signal return is the V_{REFL} pin, the common reference input return for the eight DAC–op amp channels.

As shown in *Figure 1*, the DAC section can be thought of as a potentiometer across $V_{IN}(X)$ to V_{REFL}. If this potentiometer is set to its minimum value of 0/256, the potentiometer will have no effect on the gain, and the output will be $-R_F/R_{IN} = -1$ times the input. If the potentiometer could be set to 256/256, then the amplifier positive terminal would see 100% of any input and no current would flow through R_{IN}. The circuit would behave as a non–inverting unity gain circuit, although with a noise gain of two, not one. In reality, the "potentiometer" can only be set to 255/256, and the maximum positive gain is 0.992 times the voltage between $V_{IN}(X)$ and V_{REFL}.

The true relation between the DC levels at the $V_{IN}(X)$ pins, $V_{REF}L$ and the output can be described as:

$$V_{OUT} = \left(\left(\frac{D}{128}\right) - 1\right) * (V_{IN} - V_{REFL}) + V_{REFL} \quad \text{F1}$$

where D is programmable from 0 to 255.

For single supply operation V_{REFL} is usually externally driven to some voltage above ground — typically 1.5 to 2.5V. IF V_{REFL} is driven to 1.5V, and $V_{IN}(X)$ is grounded, then code 0 would output +3.0V, and code 255 would output +11.7mV. If V_{REFL} were grounded and $V_{IN}(X)$ driven to 1.5V, then codes between 0 and 128 would attempt to drive the output below ground, which will saturate the output amplifier at some voltage slightly above ground.

USING THE SP9840/9843
Multiplication of Input Voltages

While both the **SP9840** and **SP9843** are capable of four–quadrant multiplication, this terminology is not

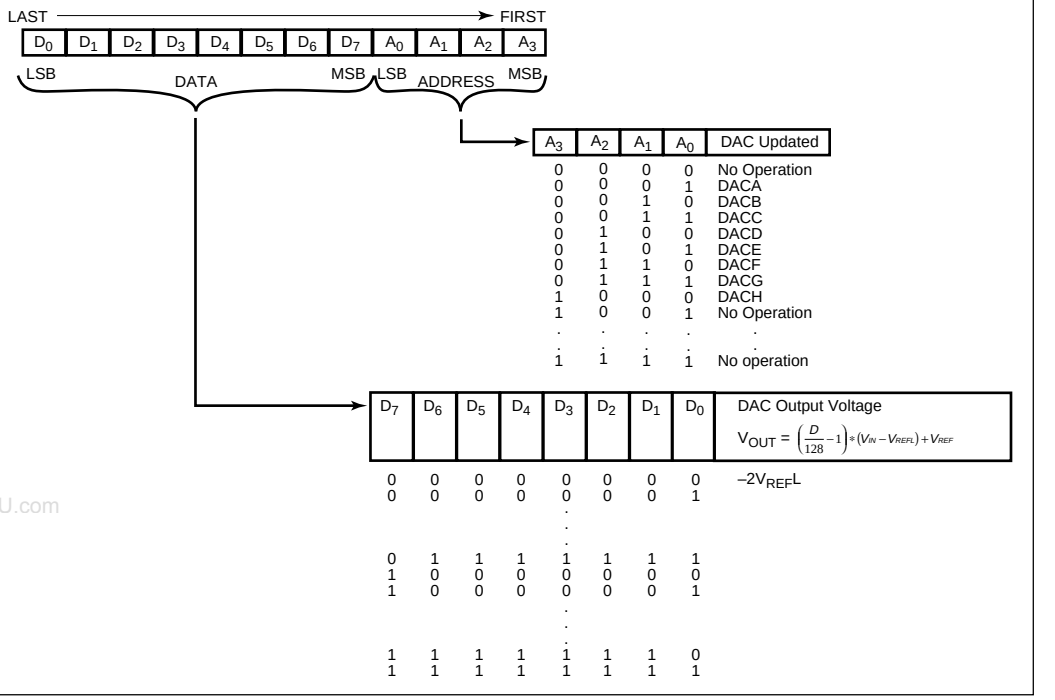


Table 1. Serial Input Decoded Truth Table

very precise when describing a system which runs from a single positive supply. Traditionally, the quadrants have been defined with respect to 0V. A two–quadrant multiplying DAC could produce negative output voltages only if a negative voltage reference were applied. A four–quadrant device could also produce a code–controlled negative output from a positive reference, or a code–controlled positive output from a negative reference. If ground is used to delineate the quadrants, then the **SP9840/SP9843** should be considered single–quadrant multiplying devices, as their output op amps cannot produce voltages below ground.

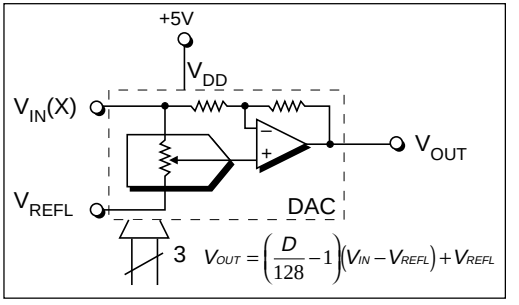


Figure 1. DAC and Output Amplifier Circuit

In reality, it is possible to define a DC voltage as a signal ground in a single supply system. If the DAC's V_{REFL} pin is driven to the voltage chosen as pseudo–ground, then each voltage output will exhibit 4–quadrant behavior with respect to pseudoground. For codes greater than 128, the output voltage will enter the quadrant below the pseudoground voltage when the input voltage goes below pseudoground. For codes less than 128, the output voltage will be below pseudoground when the input is above pseudoground.

When V_{REFL} is driven to some positive voltage and $V_{IN}(X)$ is grounded, the device performs as if it were a buffered trimpot tied between ground and a voltage equal to two times V_{REFL}. This mode of operation can be used as an "inverted single–quadrant" source with an approximate range of 0 to (V_{REFL}*2)Volts. Because the output voltage will decrease as the code is increased, this mode is considered to be inverted with respect to normal single–quadrant operation. Note that the minimum output voltage will be 1LSB above $V_{IN}(X)$.

Figure 2a and *2b* show "inverted single–quadrant" and 4–quadrant performance of the **SP9840/9843**.

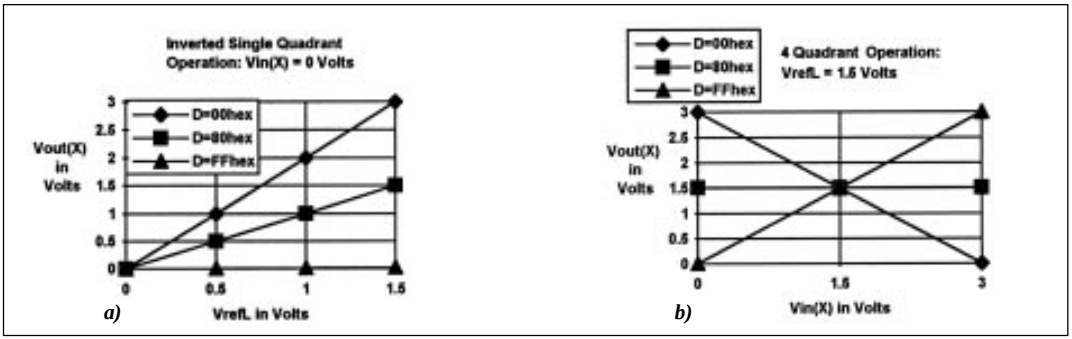


Figure 2. a) Inverted Single–Quadrant Operation; b) 4–Quadrant Operation

Applications which require two–quadrant operation with respect to pseudoground should use the **SIPEX SP9841** or **SP9842** two–quadrant multiplying DACs.

The choice of voltage to use for the pseudoground is limited by the legal voltage swing at the op amp output. The op amp exhibits excellent linearity for output voltages between, conservatively, 100mV and V_{DD} – 1.5V. The op amp BiCMOS output stage consists of an npn follower loaded by an NMOS common sourced to ground. This circuit exhibits wide bandwidth and can source large currents, while retaining the capability of driving the output to voltages close to ground.

At output voltages below 25mV, feedback forces some op amp internal nodes toward the supply rails. The NMOS pull–down device gets driven hard and the NMOS device enters the linear region — it begins to function in the same manner as a 50 ohm resistor. In reality, the wideband amplifier output stage sinks some internal quiescent current even when driving the output towards ground. This sunk current drops across the output stage NMOS transistor ON–resistance and internal routing resistance to provide a minimum output voltage below which the amplifier cannot drive. This minimum voltage is in the 15 to 25mV range. It varies within a package with each op amp's offset voltage and biasing variations. If an input voltage lower than this minimum, such as code 255 when $V_{IN}(X)$ is grounded, is requested, feedback within the op amp circuit will force internal nodes to the rails, while the output will remain saturated near this minimum value. Non–saturated monotonic behavior returns between 25mV and 100mV at the output, but full open loop gain and linearity are not apparent until the output voltage is nearly 100mV above the negative supply. Four–quadrant (programmable signed attenuator) applications usually bias V_{REFL} up at system pseudoground, well above this saturation region, and therefore maintain linearity even at high attenuations (i.e. near code 80_{HEX}).

Driving the Reference Inputs

The eight independent V_{IN} inputs of the **SP9840**, and the four–pair of inputs in the **SP9843**, exhibit a code–dependent input resistance, as shown in the specifications, and as a typical graph. In general, these inputs should be driven by an amplifier capable of handling

SDI	CLK	LOADH	PRESETL	LOGIC OPERATION
X	L	L	H	No Change
Data	↑	L	H	Shift In One Bit from SDI Shift Out 12–clock delayed data at SDO
X	X	X	L	All DAC Registers Preset to 80_H (Note 1)
X	L	H	H	Load Serial Register Data into DAC(X) Register
Note 1: "Preset" may not persist at all DACs if LOADH is high when PRESETL returns high.				

Table 2. Logic Control Input Truth Table.

the specified load resistance and capacitance. The reference inputs are useful for both AC and DC input sources. However, series resistance into these pins will degrade the linearity of the DAC — 50 Ohms of series resistance can cause up to 0.5LSB of additional integral linearity degradation for codes near zero, due to the code–dependent input current dropping across this error resistance. AC–coupled applications should use the largest capacitor value (lowest series impedance) which is practical, or use an external buffer to drive the inputs.

The DAC switches function in a break–before–make manner in order to minimize current spikes at the reference inputs. The reference inputs can withstand driving voltages slightly beyond the power rails without harm; the gain of ±1 at the op amps limits the choice of V_{IN}/V_{REFL} combinations if clipping is to be avoided at very high or very low codes. Note that rail–to–rail inputs can always be attenuated by choosing a code nearer midscale, if clipping of the output is undesirable.

Output Considerations

Each DAC output amplifier can easily drive 1Kohm loads in parallel with 15pF at its rated slew rate. The unique BiCMOS amplifier design also ensures stability into heavily capacitive loads — up to 47,000pF. Under these conditions, the slew rate will be limited by the instantaneous current available for charging the capacitance — the slew rate will be severely degraded, and some damped ringing will occur. Especially under heavy capacitive loading, a large, low impedance local bypass capacitor will be required. A 0.047µF ceramic in parallel with a low–ESR 2.2 to 10µF tantalum are recommended for worst–case loads.

The amplifier outputs can withstand momentary shorts to V_{DD} or ground. Continuous short circuit operation can result in thermally induced damage, and should be avoided.

If the input reference voltage is reduced to 0.6V, then both the amplifier and DAC are functional at room temperature at supply voltages as low as 2.5V. At V_{DD} = 2.7V, power dissipation is 9.3mW typical, with the serial clock at 4MHz, or 7.0mW typical with the serial clock gated off.

Interfacing to the SP9840/SP9843

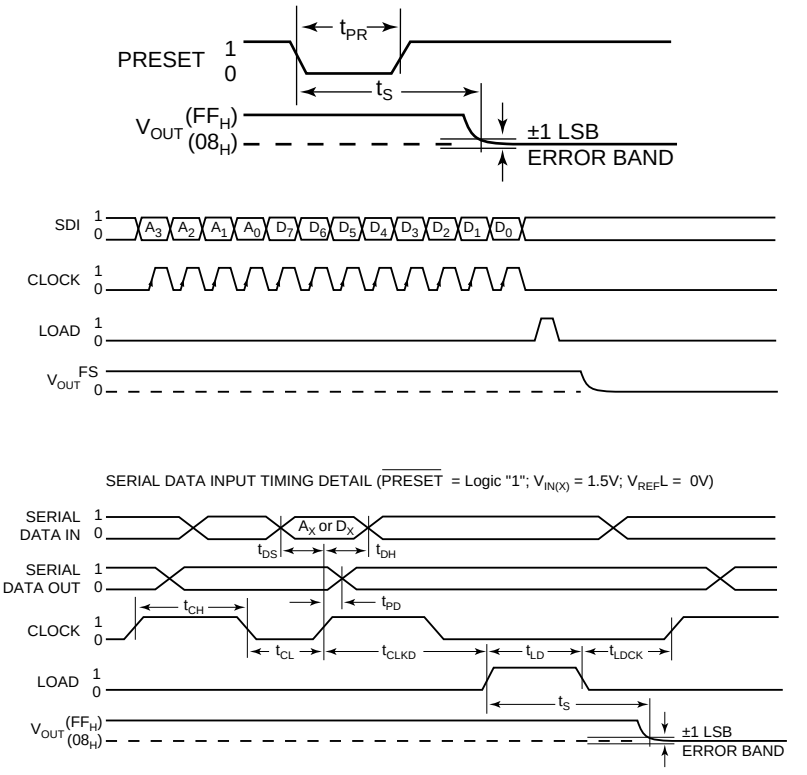
A simple serial interface, similar to that used in a 74HC594 shift–register with output latch, has been implemented in these products. A serial clock is used to strobe serial data into a 12–stage shift–register at each rising clock edge. The first four serial bits contain the address of the DAC to be updated, MSB first. The next 8 bits contain the binary value to be loaded into the desired DAC, again MSB first. After the 12th serial bit is clocked in, the LOADH line can be strobed to latch the 8 bits of data into the data holding register for the desired DAC. The address bits feed a decoding network which steers the LOADH pulse to the clock input of the desired DAC data holding register. The output of the 12th shift–register is also buffered and brought out as the SERIAL DATA OUT (SDO), which can be used to cascade multiple devices, or for data verification purposes.

The address field is set up such that DACA is addressed at 0001 (binary) and the others consecutively through DACH at 1000(binary). Address 0000(binary) will not affect the operation of any channel, as this combination is easily generated inadvertently at power–up. Other no–operation addresses exist at 1001(binary) through 1111(binary). Another use for no–operation addresses is to mask off updates of any DAC channel in a multiple–part system with cascaded serial inputs and outputs. By sending a valid address and data only to the desired channel, it is possible to simplify the system hardware by driving the LOADH pin at each part in parallel from a single source. *Table 1* shows a register–level diagram of the addresses, data, and the resulting operation.

A fourth control pin, PRESETL, can be used to simultaneously preset all DAC data holding registers to their mid–scale (80_H) values. This will asynchronously force all DAC outputs to buffer the voltages at their respective inputs to their outputs with unity gain. This feature is useful at power–up, as a simple resistor to the supply and capacitor to ground can insure that all DAC outputs start at a known voltage. For four–channel multiplying applications, this sets the default start–up gain to zero; only –70dB of feedthrough from the V_{IN}(X) inputs will be present at the outputs. *Table 2* summarizes the operation of the four digital inputs.

The four digital control input pins have been designed to accept TTL (0.8V to 2.0V minimum) or full 5V CMOS input levels. The serial data output can drive either TTL or CMOS inputs. Timing information is shown in *Figure 3*. Serial data is fully clocked into the shift–register after 12 clock rising edges, subject to the described setup and hold times. After the shift–register data is valid, the LOADH line can be pulsed high to load data into the desired DAC data register, which switches the DAC to the new input code. The serial clock input should not see a rising edge while the LOADH pulse is high in order to prevent shift–register data from corruption during data register loading.

The serial clock and data input pins are designed to be compatible as slaves under **National Semiconductor**'s Microwire™ and MicrowirePlus™ protocols and under **Motorola**'s SPI™ and QSPI™ protocols. In some micro–controllers, the interface is completed by programming a bit in a general–purpose I/O port as a level, used to strobe the LOADH line at the DACs. This is done in a manner similar to that used for generating a Chip Select signal, which is necessary when driving some other Microwire™ peripherals.



CHARACTERISTICS

(Typical @ 25°C with V_{DD} = +5V unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Clock Pulse Width (t_{CH}, t_{CL})	50			ns	
Data Setup Time (t_{DS})	30			ns	
Data Hold Time (t_{DH})	20			ns	
CLK to SDO Propagation Delay (t_{PD})			100	ns	
DAC Register Load Pulse Width (t_{LD})	50			ns	
Preset Pulse Width (t_{PR})	50			ns	
Clock Edge to Load Time (t_{CKLD})	30			ns	
Load Edge to Next Clock Edge (tLDCK)		60		ns	

Figure 3. Timing

ORDERING INFORMATION

Model	Reference Inputs	Temperature Range	Package
SP9840KN	Eight, independent	0° to + 70°C	24–pin, 0.3" Plastic DIP
SP9840BN	Eight, independent	–40° to + 85°C	24–pin, 0.3" Plastic DIP
SP9840KS	Eight, independent	0° to + 70°C	24–pin, 0.3" SOIC
SP9840BS	Eight, independent	–40° to + 85°C	24–pin, 0.3" SOIC
SP9843KS	Four pair	0° to + 70°C	20–pin, 0.3" SOIC
SP9843BS	Four pair	–40° to + 85°C	20–pin, 0.3" SOIC