PCI 9030 Data Book

PCI 9030 Data Book

Version 1.4

May 2002

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PREFACE

The information contained in this document is subject to change without notice. Although an effort has been made to keep the information accurate, there may be misleading or even incorrect statements made herein.

SUPPLEMENTAL DOCUMENTATION

The following is a list of additional documentation to provide the reader with further information regarding the PCI 9030 and related subjects:

- *PCI Local Bus Specification, Revision 2.1*, June 1, 1995
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com

- *PCI Local Bus Specification, Revision 2.2*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com

- *PCI Hot-Plug Specification, Revision 1.1*, June 20, 2001
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com

- *PCI Bus Power Management Interface Specification, Revision 1.1*, December 18, 1998
  PCI Special Interest Group (PCI SIG)
  5440 SW Westgate Drive #217, Portland, OR 97221 USA
  Tel: 503 291-2569, Fax: 503 297-1090, http://www.pcisig.com

- *PICMG 2.1, R2.0, CompactPCI Hot Swap Specification*, January 17, 2001
  PCI Industrial Computer Manufacturers Group (PICMG)
  c/o Virtual Inc., 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA
  Tel: 781 246-9318, Fax: 781 224-1239, http://www.picmg.org

- IEEE Standard 1149.1-1990, *IEEE Standard Test Access Port and Boundary-Scan Architecture*, 1990
  The Institute of Electrical and Electronics Engineers, Inc.
  445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA
  Tel: 800 678-4333 (domestic) or 732 981-0060, Fax: 732 981-1721, http://www.ieee.org

Note: *In this data book, shortened titles are given to the works listed above. The following table lists these abbreviations.*

Supplemental Documentation Abbreviations

Abbreviation	Document
PCI r2.1	PCI Local Bus Specification, Revision 2.1
PCI r2.2	PCI Local Bus Specification, Revision 2.2
Hot-Plug r1.1	PCI Hot-Plug Specification, Revision 1.1
PCI Power Mgmt. r1.1	PCI Bus Power Management Interface Specification, Revision 1.1
PICMG 2.1, R2.0	PICMG 2.1, R2.0, CompactPCI Hot Swap Specification
IEEE Standard 1149.1-1990	IEEE Standard Test Access Port and Boundary-Scan Architecture

TERMS AND DEFINITIONS

- PCI Target (Direct Slave)

  External PCI Bus Initiator initiates Data write/read to/from the Local Bus

Data Assignment Conventions

Data Width	PCI 9030 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	Lword

REVISION HISTORY

Date	Version	Comment
3/1999	0.90	New Release PCI 9030 Preliminary Data Book, Version 0.9.
8/1999	0.90	Update.
10/1999	0.90	Initial Release Red Book.
10/1999	0.91	Update.
11/1999	0.92	Update.
12/1999	0.93	Initial Release Blue Book.
4/2000	1.0	Production Release.
1/31/2001	1.1	Incorporated 1/31/2001 Addendum changes, including past design notes.
12/2001	1.2	Released version 1.2. Updated Hot-Plug support from Revision 1.0 to Revision 1.1. Updated PICMG 2.1 Hot Swap support from Revision 1.0 to Revision 2.0. Corrected Table 2-1 for PCI Command Code response. Renamed Section 2.2.2 from "Local Signals" to "Local Bus Signals Used in Timing Diagrams." Revised Section 2.2.4.2.1 Local Bus Wait State content and added Figures 2-1 and 2-2 to illustrate wait state definitions. Revised Sections 2.2.4.3.1 through 2.2.4.3.2.1 to clarify Local Bus bursting, Bterm mode, and BTERM# input. Corrected LINT[1:2] polarity in Timing Diagram 4-8. Updated Section 10 PCIBAR*x*, EROMRR, LAS*x*RR, EROMBRD, and LAS*x*BRD register bit descriptions. Replaced the PMDATASEL register description (missing in version 1.1). Corrected LAS*x*BRD[25] descriptions for Big Endian Byte Lane mode to indicate this bit is functional only in Big Endian mode. Updated the PMC register description to match *PCI Power Mgmt. r1.0*. (Refer to *PCI 9030 Design Notes #1* for a revised PMC register description compliant with *PCI Power Mgmt. r1.1*). Added pull-down recommendation to TRST# pin description and changed READY# wait state generator-related information in Section 11. Documented additional reset behavior in Section 11.1. Updated ALE Timing illustration, Figure 12-3. Figure 13-2 modified to remove non-metric measurements. Replaced Figure 13-6, "180-Pin µBGA Package Layout—Underside View" and Table 13-3, "180-Pin µBGA PCI 9030 Pinout" with new Figure 13-6, "180-Pin µBGA Physical Layout with Pinout." Updated package mechanical drawings for changed marking content, which affects inspection, pattern recognition, and tray and board loading equipment.
01/2002	1.3	Revised and clarified Figures 13-4 and 13-6. Updated Section 10 EROMBRD[19:15] and LAS*x*BRD[19:15] register bit descriptions, and associated text that appears elsewhere in the data book, to include LD signal. Corrected Section 10 EROMBRD[5] and LAS*x*BRD[5] register bit descriptions regarding "when set to 0".
05/2002	1.4	Corrected Fiducial locations and Pad Pitch measurement in Figure 13-2. Only affected pages list the revision and date change.

PCI 9030

PCI SMARTarget I/O Accelerator

May 2002
Version 1.4

CompactPCI Hot Swap Ready
for Adapters and Embedded Systems

FEATURE SUMMARY

- *PCI Local Bus Specification r2.2*-compliant 32-bit, 33 MHz Bus Target Interface Device enabling PCI Burst Transfers up to 132 MB/s
- *PCI Bus Power Management Interface Specification r1.1* compliant
- *PCI Local Bus Specification r2.2* Vital Product Data (VPD) configuration support
- *PICMG 2.1, R2.0, CompactPCI Hot Swap Specification*, Hot Swap Silicon
    - Programming Interface 0 (PI = 0)
    - Precharge Bias Voltage Support
    - Early Power Support
- PCI Target Programmable Burst Management
- PCI Target Read Ahead mode
- PCI Target Delayed Read mode
- PCI Target Delayed Write mode
- Programmable Interrupt Generator/Controller
- Two programmable FIFOs for zero wait state burst operation

- Flexible Local Bus runs up to 60 MHz
- 3.3/5V tolerant PCI and Local signaling supports Universal PCI Adapter designs
- Flexible Local Bus provides 32-bit Multiplexed or Non-Multiplexed Protocol for 8-, 16-, or 32-bit Peripheral and Memory devices
- Serial EEPROM interface
- Nine programmable General Purpose I/O (GPIOs)
- Five programmable Local Address spaces
- Four programmable independent Chip Selects
- Programmable Local Bus wait states
- Programmable Local Read prefetch mechanism
- Local Bus can run asynchronously to the PCI Bus
- Two programmable Local-to-PCI interrupts
- Endian Byte Swapping
- 3.3V Core, Low-Power CMOS in 176-pin PQFP or 180-pin µBGA
- Industrial Temp Range operation
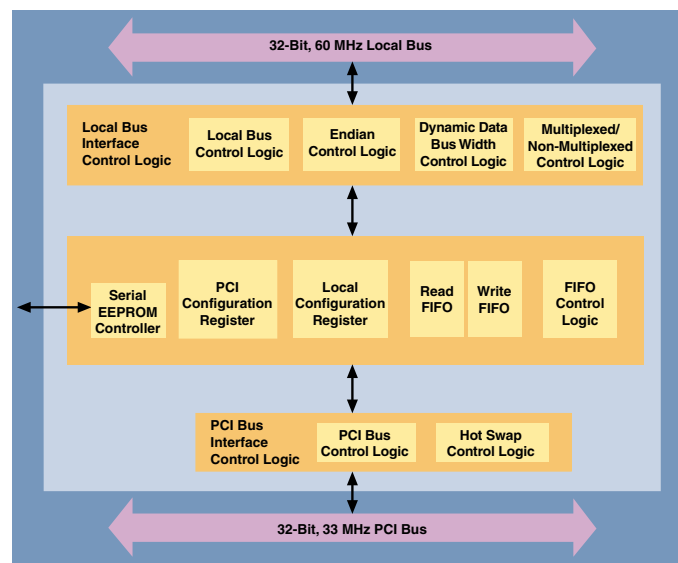
PCI 9030 Internal Block Diagram

1 INTRODUCTION

1.1 COMPANY AND PRODUCT BACKGROUND

PLX Technology, Inc., is the leading supplier of high-speed, interconnect silicon and software solutions for the networking and communications industry. These include high-speed silicon, reference design tools that minimize design risk, and software for managing data throughout the PCI Bus, as well as third-party development tool support through the PLX Partner Program, further extending our complete solution.

The PLX solution enables hardware designers and software developers to maximize system input/output (I/O), lower development costs, minimize system design risk, and accelerate time to market.

PLX PCI I/O Accelerator chips and I/O Processor devices are designed in a wide variety of embedded PCI communication systems, including switches, routers, media gateways, base stations, access multiplexors, and remote access concentrators. PLX customers include many of the leading communications equipment companies—3Com, Cisco Systems, Compaq Computer, Ericsson, Hewlett-Packard, Intel, IBM, Lucent Technologies, Marconi, Nortel Networks, and Siemens.

Founded in 1986, PLX has developed products based on the PCI industry standard since 1994. PLX is publicly traded (NASDAQ: PLXT) and headquartered in Sunnyvale, California, USA, with operations in the United Kingdom, Japan, and China.

1.1.1 PCI 9030 SMARTarget I/O Accelerator

The PCI 9030, a 32-bit, 33-MHz PCI Bus Target Interface chip with SMARTarget™ Technology, is the most advanced general-purpose PCI Target device available. It offers complete *PCI r2.2* implementation, enabling Burst transfers up to 132 MB/s, and is the industry's first CompactPCI Hot Swap *PICMG 2.1, R1.0*-compatible *Ready* Target device. The PCI 9030 is the perfect solution for migrating legacy designs to PCI while adding new features that enhance next generation Target designs. The PCI 9030 SMARTarget I/O Accelerator brings PLX's industry-leading experience in the PCI design world to the customer in a way that is simple and convenient to use.

1.1.2 SMARTarget Technology

Many PCI chip and core designs implement only basic *PCI r2.2* bus interface signaling, leaving the difficult performance and compatibility issues to the designer. The PCI 9030, with SMARTarget Technology, incorporates features which simplify design implementation. These features go far beyond the minimum to provide the highest possible design performance and flexibility.

SMARTarget Technology performance features:

- *PCI r2.2* compliant, 32-bit, 33 MHz Target Interface, enabling PCI Burst transfers up to 132 MB/s
- Up to 60 MHz Local Bus operation, enabling Burst transfers up to 240 MB/s
- PCI Target Read Ahead mode
- PCI Target Programmable Burst
- PCI Target Delayed Write mode
- Posted Memory Writes

SMARTarget Technology flexibility features:

- Programmable 32-bit Local Bus operates up to 60 MHz
- Supports five PCI-to-Local Address spaces
- Nine programmable General Purpose I/Os (GPIOs)
- Four programmable Chip Selects
- *PICMG 2.1, R2.0*, Hot Swap Silicon, including support for
  - Programming Interface 0 (PI = 0)
  - Precharge Bias Voltage
  - Early Power
- Big/Little Endian byte conversion
- Interrupt Generator/Controller
- *PCI r2.2* Vital Product Data (VPD)
- *PCI Power Mgmt. r1.1*
- 3.3/5V tolerant PCI signaling
- 3.3V CMOS device in 176-PQFP or 180-pin μBGA
- Programmable Read and Write strobe timing on the Local Bus

1.1.3   PCI 9030 Applications

The PCI 9030 can be used in a wide variety of networking, telecom, imaging, industrial and storage applications. The PCI 9030 simplifies legacy design migration to PCI by providing a convenient off-the-shelf solution that enables prototypes to be operational in a short time period.

1.1.3.1   High-Performance PCI Target Interface

The PCI 9030's built-in SMARTarget performance features (*such as* 3.3/5V tolerant I/O buffers and Local Bus operation up to 60 MHz), enable designers to connect a wide variety of memory and I/O devices. With SMARTarget in action, PCI Target Adapter designs have never been simpler to implement. Figure 1-1 illustrates a typical PCI Target adapter card.
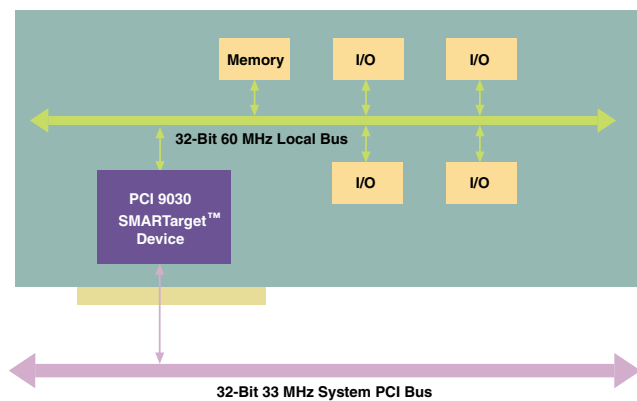
Figure 1-1. Typical PCI Target Adapter Card

1.1.3.2   High-Performance CompactPCI Adapter Card

The PCI 9030 has integrated key features to enable live insertion of Hot Swap CompactPCI adapters. The PCI 9030 Hot Swap Silicon includes the following features:

- Compliant with *PCI r2.2*
- Tolerant of V_{CC} from early power, including support for pin bounce, I/O cell stability within 4 ms, and low current drain during insertion
- Tolerant of asynchronous reset
- Tolerant of precharge bias voltage

- I/O buffers meet modified V/I requirements in *PICMG 2.1, R2.0*
- Limited I/O pin leakage at precharge bias voltage
- Incorporates the Hot Swap Control/Status register (HS_CSR)
- Incorporates an Extended Capability Pointer (ECP) to the Hot Swap Control/Status register
- Incorporates added resources for software control of the ejector switch, ENUM#, and the blue "Status" LED which indicates insertion and removal to the user
- Precharge Bias Voltage Support with integrated 10K-Ohm precharge resistors eliminates the need for an external resistor network
- Early Power Support allows transition between the operating and powered down states without external circuitry
- Programming Interface 0 (PI = 0)

Figure 1-2 illustrates a typical CompactPCI adapter card.
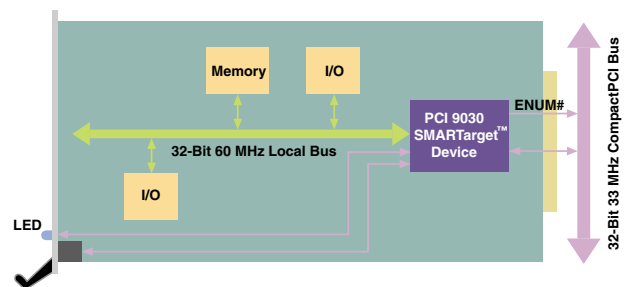
Figure 1-2. High-Performance CompactPCI Adapter Card

1.1.3.3   PMC Adapter Cards

In the real estate-conscious world of PMC cards, the PCI 9030 offers an attractive packaging option with the dime-size 180-pin μBGA. SMARTarget flexibility features, *such as* GPIOs and programmable chip selects, save additional valuable board space. The PCI 9030 enables a new generation of mini form factor PCI cards.

Figure 1-3 illustrates a typical PMC adapter card.
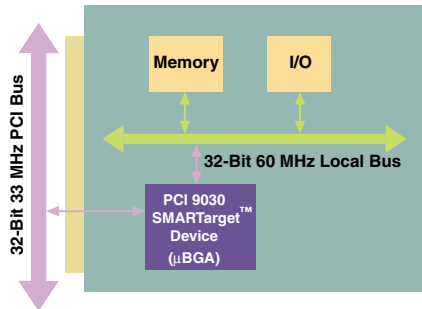
Figure 1-3. Typical PMC Adapter Card

1.1.4   PCI 9030 SMARTarget Features

1.1.4.1   Performance Features

PCI r2.2 **Compliant.** This 32-bit, 33 MHz Target Interface Chip enables PCI Burst Transfers up to 132 MB/s.

Up to 60 MHz Local Bus Operation. Enables burst transfers up to 240 MB/s.

PCI Target Read Ahead Mode. Prefetches a programmable amount of data from the Local Bus. This data can then be burst-transferred onto the PCI bus from the PCI 9030 internal PCI Target Read FIFO. The prefetch size can be programmed to match the PCI master burst length or can be used in the PCI Target Read Ahead mode data. This feature also allows for increased bandwidth and reduced read latency.

PCI Target Programmable Burst. The PCI 9030 may be programmed for several burst lengths, including unlimited burst. This allows for maximum transfer rates on both the PCI and Local Buses.

PCI Target Delayed Write Mode. The PCI Target Write data accumulates in the PCI Target Write FIFO to allow uninterrupted burst transactions on the Local Bus. This allows for a higher throughput for conditions in which the PCI Clock frequency is slower than the Local Clock frequency.

Posted Memory Writes. A PCI Memory write is posted to the PCI 9030 for later transfer to the Local Bus. This allows for maximum PCI performance and avoids potential deadlock situations.

1.1.4.2   Flexibility Features

Programmable Local Bus. Operates up to 60 MHz and supports both Multiplexed and Non-Multiplexed 32-bit address/data protocol, and dynamic Local Bus width control allowing Slave accesses to 8-, 16- or 32-bit devices.

PCI-to-Local Address Spaces. Supports five PCI-to-Local Address spaces. Spaces 0, 1, 2, 3, and the Expansion ROM all allow a PCI Bus Master to access the Local Memory spaces with individually programmable wait states, bus width, and burst capabilities.

GPIOs. The PCI 9030 has nine programmable general purpose I/O pins, which may be used for generic interface purposes.

Four Programmable Chip Selects. Eliminates decode logic, which improves performance.

PICMG 2.1, R2.0 **Hot Swap Silicon.** Compliant with *PICMG 2.1, R2.0*, including support for Programming Interface 0 (PI = 0), Precharge Bias Voltage, and Early Power.

Big/Little Endian Conversion. Supports automatic on-the-fly Big Endian and Little Endian conversion for all operations and bus widths.

Interrupt Generator/Controller. Can assert PCI interrupts from external and internal sources.

VPD Support. Fully supports the *PCI r2.2* Vital Product Data (VPD) extension, including the New Capabilities Structure. Provides an alternate access method for user- or system-defined parameters or configuration data.

PCI Power Management. Supports D_0 and D_{3hot} power states.

Two Programmable FIFOs for Zero Wait State Burst Operation. The following table describes the FIFO depth.

Table 1-1. FIFO Depth

FIFO	Depth
PCI Target Read	16 Lwords
PCI Target Write	32 Lwords

3.3/5V Tolerant PCI Signaling. Enables Universal PCI Adapters.

3.3V CMOS Device in 176-pin PQFP or 180-pin µBGA.

1.1.4.3   Additional Features

5V Tolerant Operation. The PCI 9030 requires a 3.3V supply. It provides 3.3V signaling with 5V I/O tolerance on both the PCI and Local Buses.

Serial EEPROM Interface. The PCI 9030 contains a three-wire serial EEPROM interface that provides the option of loading configuration information from a serial EEPROM device.

Clocks. The Local Bus interface runs from a Local Bus clock, which runs asynchronously to the PCI clock. In addition, the PCI 9030 provides a buffered PCI clock output, which can be used as a Local Bus clock input.

RST# Timing. Supports response to first configuration accesses after de-assertion of PCI RST# in less than 2^{25} clocks.

Subsystem and Subsystem Vendor IDs. Contains Subsystem ID and Subsystem Vendor ID in the PCI Configuration register space, in addition to Device and Vendor IDs.

Silicon Revision ID. Contains the PCI 9030 Silicon Revision ID, which is programmable by way of the serial EEPROM.

1.1.5   PLX Chip Compatibility

1.1.5.1   Pin Compatibility

The PCI 9030 is *not* pin compatible with the PCI 9050, PCI 9052, PCI 9054, *nor* the PCI 9080.

1.1.5.2   Register Compatibility

All registers implemented in the PCI 9050 and 9052 are implemented in the PCI 9030. The PCI 9030 includes many new bit definitions and several new registers. Refer to Table 1-2 for details.

The PCI 9030 is *not* register-compatible with the PCI 9080 nor the PCI 9054.

1.1.6 PCI 9030 COMPARISON WITH OTHER PLX CHIPS

Table 1-2. PCI 9030, PCI 9050, and PCI 9052 Comparison

Feature	PCI 9030	PCI 9050	PCI 9052
Pin Count and Type	176 PQFP/180 µBGA	160 PQFP	160 PQFP
Package Size	27 x 27 mm	31 x 31 mm	31 x 31 mm
Local Address Spaces	5	5	5
PCI Initiator Mode	No	No	No
Number of FIFOs	2	2	2
FIFO Depth—PCI Target Write	32 Lwords (128 bytes)	16 Lwords (64 bytes)	16 Lwords (64 bytes)
FIFO Depth—PCI Target Read	16 Lwords (64 bytes)	8 Lwords (32 bytes)	8 Lwords (32 bytes)
LLOCKo# Pin for Lock Cycles	Yes	Yes	Yes
WAITo# Pin for Wait State Generation	Yes	Yes	Yes
BCLKo (BCLKO) Pin; Buffered PCI Clock	Yes	Yes	Yes
ISA Bus Interface	No	No	Yes
Register Addresses	Identical to the PCI 9050 and PCI 9052, but contains additional registers for increased functionality	—	—
Big Endian ⇔ Little Endian Conversion	Yes	Yes	Yes
PCI Target Delayed Read Transactions	Yes	Yes	Yes
PCI Target Delayed Write Transactions	Yes	No	No
PCI Bus Power Management Interface r1.1	Yes	No	No
PCI r2.2 VPD Support	Yes	No	No
Programmable Prefetch Counter	Yes	Yes	Yes
Programmable Wait States	Yes	Yes	Yes
Programmable Local Bus READY# Timeout	Yes	No	No
Programmable GPIOs	9	4	4
Additional Device and Vendor ID Registers	Yes	Yes	Yes
Core and Local Bus V_{CC}	3.3V	5V	5V
PCI Bus V_{CC}	3.3V	5V	5V
3.3V PCI Bus and Local Bus Signaling	Yes	No	No
5V Tolerant PCI Bus and Local Bus Signaling	Yes	Yes	Yes
Serial EEPROM Support	2K, 4K bit devices	1K bit devices	1K bit devices
Serial EEPROM Read Control	Reads allowed via VPD function (refer to Section 9) and Serial EEPROM Control register (CNTRL)	Reads allowed via Serial EEPROM Control register (CNTRL)	Reads allowed via Serial EEPROM Control register (CNTRL)
PCI Target Read Ahead Mode	Yes	Yes	Yes
CompactPCI Hot Swap Capability	*Ready*	*Capable*	*Capable*

1—Introduction

2   PCI AND LOCAL BUS

This section discusses PCI and Local Bus operation.

2.1   PCI BUS

2.1.1   PCI Bus Interface and Bus Cycles

The PCI 9030 is *PCI r2.2*-compliant. Refer to *PCI r2.2* for specific PCI Bus functions as a PCI Target Interface chip.

2.1.1.1   PCI Target Command Codes

As a Target, the PCI 9030 allows access to the PCI 9030 internal registers and the Local Bus, using the commands listed in Table 2-1.

All Read or Write accesses to the PCI 9030 can be Byte, Word, or Lword (32-bit data). All memory commands are aliased to basic memory commands. All PCI 9030 I/O accesses are decoded to an Lword boundary. Byte enables are used to determine which bytes are read or written. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

Table 2-1. PCI Target Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

2.1.1.2   Wait States—PCI Bus

The PCI Bus Master throttles IRDY# and the PCI Bus Slave throttles TRDY# to assert PCI Bus wait state(s).

2.1.1.3   PCI Bus Little Endian Mode

The PCI Bus is a Little Endian bus (*that is*, the address is invariant and data is Lword-aligned to the lowermost byte lane).

Table 2-2. PCI Bus Little Endian Byte Lanes

Byte Number	Byte Lane
0	AD[7:0]
1	AD[15:8]
2	AD[23:16]
3	AD[31:24]

2.1.1.4   PCI Prefetchable Memory Mapping

PCI Memory Address spaces assigned to the PCI 9030 for its Local Address spaces can be mapped as either prefetchable or non-prefetchable memory within the system. Configuration software (PCI BIOS) checks the PCI 9030 Configuration register Prefetchable bit(s) (PCIBARx[3], where x is the PCI Base Address register number) to determine whether the Target memory is prefetchable. The value of the PCIBARx[3] bit(s) is set according to Local Configuration register settings (as configured by serial EEPROM values) at boot time.

When set to 1, the PCIBARx[3] bit(s) signals that the Memory space can operate under a prefetching protocol, for improved performance. If a PCI Master initiates a Read to a location that is mapped in the prefetchable address range, a Host-to-PCI or PCI-to-PCI bridge is permitted to extend the Read Transaction burst length in anticipation of the Master consuming the additional data. PCIBARx[3] should normally be set if all the following conditions are met:

- Multiple Memory reads of an Lword result in the same data
- If Read data is discarded by the PCI Master, no negative side effects occur
- Address space is not mapped as I/O
- Local Target must be able to operate with byte merging

Byte merging is an optional function of a Host-to-PCI or PCI-to-PCI bridge in which bytes or combinations of bytes written in any order by multiple individual Memory Write cycles to one Lword address can be merged within the bridge's Posted Memory Write buffer into a single Lword Write cycle. Byte merging is possible when any of the bytes to be merged are written only once, and the Prefetchable bit(s) is set to 1 (PCIBAR*x*[3]=1).

The Prefetchable bit(s) setting has no effect on prefetching initiated by the PCI 9030. PCI 9030 prefetching is disabled, by default, in the Local Configuration registers, and should be enabled to support highest performance with PCI Target Burst reads and PCI Target Read Ahead mode. (Refer to Section 4.2.1.4.)

2.1.1.5 PCI Target Accesses to an 8-or 16-Bit Local Bus Device

Direct PCI access to an 8- or 16-bit Local Bus device results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each 8-bit transfer, byte enables are encoded to provide Local Address bits LA[1:0]. For each 16-bit transfer, byte enables are encoded to provide BLE#, BHE#, and LA1.

2.2 LOCAL BUS

2.2.1 Introduction

The Local Bus provides a data path between the PCI Bus and non-PCI devices, including memory devices and peripherals. The Local Bus is a 32-bit multiplexed or non-multiplexed bus, with bus memory regions that can be programmed for 8-, 16-, or 32-bit widths. The PCI 9030 Local Bus is signal-compatible with popular RISC and Bridge architecture, including the i960Cx, i960Jx, and PPC401 GF. In addition, the Local Bus can directly connect to Texas Instruments DSP devices (*such as* the TMS320C6202 and TMS320C54x).

The PCI 9030 is the Local Bus Master. The PCI 9030 can transfer data between the Local Bus, internal registers and FIFOs. Burst lengths are not limited. The bus width depends upon the Local Address Space register setting. There are four address spaces and one default space (the Expansion ROM that can be used as another address space). Each space contains a set of configuration registers that determine all Local Bus characteristics when that space is accessed.
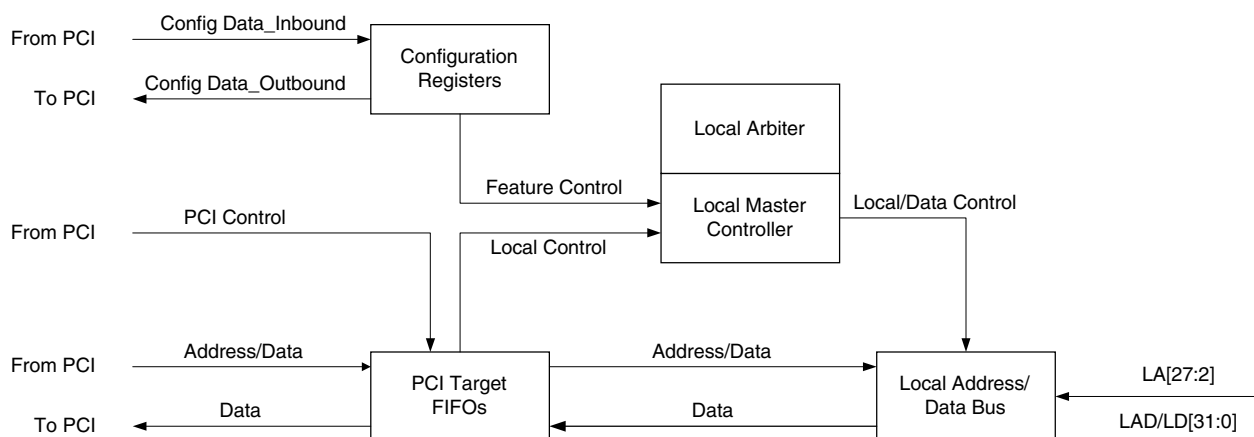
Figure 2-1. Local Bus Block Diagram

2.2.1.1 Transactions

Four types of transactions can occur on a Local Bus:

- Read
- Write
- Read Burst
- Write Burst

A Bus access is a transaction which is bounded by the assertion of ADS# at the beginning and de-assertion of BLAST# at the end. A Bus access consists of an Address cycle followed by one or more Data transfers. During each Clock cycle of an access, the Local Bus is in one of four basic states defined in Section 2.2.1.2. A Clock cycle consists of one Local Bus clock period.

2.2.1.2 Basic Bus States

The four basic bus states are idle, address, data/wait, and recovery. Once the Local Bus Master owns the bus and needs to start a bus access, the address state is entered, ADS# or ALE is asserted, and a valid address is presented on the address/data bus. Data is then transferred while in a data/wait state. READY# or the internal wait state generator is used to insert wait states. BLAST# is asserted during the last data/wait state to signify the last transfer of the access.

After all data is transferred, the bus enters the recovery state to allow the bus devices to recover. The bus then enters the idle state and waits for another access.

2.2.2 Local Bus Signals Used in Timing Diagrams

The key Local Bus control signals listed in most timing diagram examples are as follows:

- ADS# or ALE indicates the start of an access
- READY#, WAITo#, and BTERM# are used to insert wait states and terminate Burst cycles during Data transfers
- LW/R# indicates the Data transfer direction
- BLAST# and BTERM# indicate the end of an access

The key data signals are:

- LA Address Bus
- LAD Address, Data Bus
- LBE[3:0]# Local Byte Enables, indicating valid byte lanes

2.2.3 Local Bus Signals

There are four groups of Local Bus signals:

- Clock
- Address/Data
- Control/Status
- Arbitration

Signal usage varies upon application.

2.2.3.1 Clock

LCLK, the Local Bus clock, operates at frequencies up to 60 MHz, and is asynchronous to the PCI Bus clock. Most Local Bus signals are driven and sampled on the rising edge of LCLK. Setup and hold times, with respect to LCLK, must be observed. (Refer to Section 12.2, "Local Inputs," on page 12-3 for setup and hold timing requirements.)

2.2.3.2 Address/Data

2.2.3.2.1 Multiplexed Mode (MODE=1)

2.2.3.2.1.1 LA[27:2]

LA[27:2] contains the transfer address. The address remains valid during the transfer, and increments with successive data during Burst cycles.

2.2.3.2.1.2 LAD[31:0]

The LAD[31:0] Bus is a 32-bit Multiplexed Address/Data Bus. During an Address phase, LAD[27:0] contains the transfer address, with LAD[1:0] having the same state as LBE[1:0]# pins.

During Data phases, LAD[31:0], LAD[15:0], or LAD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8 or 16 bits wide, the data supplied by the PCI 9030 is replicated across the entire 32-bit-wide bus.

2.2.3.2.2 Non-Multiplexed Mode (MODE=0)

2.2.3.2.2.1 LA[27:2]

LA[27:2] contains the transfer address. The address remains valid during the transfer, and increments with successive data during Burst cycles.

2.2.3.2.2.2 LD[31:0]

The LD[31:0] bus is a 32-bit Non-Multiplexed Data Bus. During Data phases, LD[31:0], LD[15:0], or LD[7:0] contain transfer data for a 32-, 16-, or 8-bit bus, respectively. If the bus is 8 or 16 bits wide, the data supplied by the PCI 9030 is replicated across the entire 32-bit-wide bus.

2.2.3.3 Control/Status

The control/status signals control the address latches and flow of data across the Local Bus.

2.2.3.3.1 ADS#, ALE

A Local Bus access starts when ADS# (address strobe) is asserted during an address state by the PCI 9030 as the Local Bus Master. ALE is used to strobe the LA/LAD Bus into an external address latch. When BTERM# input is enabled for a Local Address space in the corresponding Bus Region Descriptor register, BTERM# can be used to complete an access in place of LRDYi#. When BTERM# is enabled and asserted, LRDYi# is ignored. (Refer to Figure 12-3 on page 12-5 for ALE timing specifications, and to Section 2.2.4.3 for further information regarding BTERM#.)

2.2.3.3.2 LBE[3:0]#

During an Address phase, the LBE[3:0]# Local Byte Enables denote which byte lanes are being used during access of a 32-bit bus. They remain asserted until the end of the data transfer.

2.2.3.3.3 LLOCKo#

When the PCI 9030 owns the Local Bus, LLOCKo# is asserted to indicate that an atomic operation for a PCI Target access may require multiple transactions to complete. LLOCKo# is asserted during the Address phase of the first transaction of the atomic operation, and de-asserted one clock after the last transaction of the atomic operation completes. If enabled, the Local Bus arbiter does not grant the Bus to another Master until the atomic operation completes.

2.2.3.3.4 LW/R#

During an Address phase, LW/R# is driven to a valid state, and signifies direction of the data transfer. Since the PCI 9030 is the Local Bus Master, LW/R# is driven high when the PCI 9030 is writing data to a Local Bus, and low when it is reading the bus.

2.2.3.3.5 RD#

RD# is a general purpose read output strobe. The timing is controlled by the current Bus Region Descriptor register. The RD# strobe is asserted during the entire data transfer.

Normally, RD# is also asserted during NRAD wait states, unless Read Strobe Delay clocks are programmed the Bus Region Descriptor register(s) (LAS*x*BRD[27:26] and/or EROMBRD[27:26], where *x* is the Local Address Space number). (Refer to Table 2-5 and Figure 2-3.) RD# remains asserted throughout Burst and NRDD wait states.

Table 2-3. READY# Data Transfers

Slave Device	READY#		Description
	Input Enable	Signal	
Address Spaces	0	Ignored	READY# is not sampled by the PCI 9030. Data transfers determined by the internal wait state generator. READY# is ignored and the Data transfer takes place after the internal wait state counter expires.
	1	Sampled	READY# is sampled by the PCI 9030. Data transfers are determined by an external device, which asserts READY# to indicate a Data transfer is taking place.

2.2.3.3.6   READY#

The READY# input pin has a corresponding Enable bit in the Bus Region Descriptor register(s) (LAS*x*BRD[1] and/or EROMBRD[1]). If READY# is enabled, this indicates that Write data is being accepted or Read data is being provided by the Bus Slave. If a Bus Slave needs to insert wait states, it can de-assert READY# until it is ready to accept or provide data. If READY# is disabled, then the Local Bus transfer length can be determined by internal wait state generators. (Refer to Table 2-3.)

2.2.3.3.7   WAITo#

WAITo# is an output that provides status of the internal wait state generators. It is asserted while internal wait states are being inserted. READY# input is not sampled until WAITo# is de-asserted.

2.2.3.3.8   WR#

WR# is a general purpose write output strobe. The timing is controlled by the current Bus Region Descriptor register. The WR# strobe is asserted during the entire data transfer.

WR# is normally asserted during address-to-data wait states (NWAD), unless Write Strobe Delay clocks are programmed in the Bus Region Descriptor register(s) (LAS*x*BRD[29:28] and/or EROMBRD[29:28]). WR# remains asserted throughout Burst and data-to-data wait states (NWDD). The LAD/LD Data Bus valid time can be extended beyond WR# de-assertion if Write Cycle Hold clocks are programmed in the Bus Region Descriptor register(s) (LAS*x*BRD[31:30] and/or EROMBRD[31:30]).

2.2.3.4   Local Bus Arbitration

The PCI 9030 is the Local Bus Master. When the PCI Bus initiates a new transfer request, the PCI 9030 takes Local Bus control. Another device can gain Local Bus control by asserting LREQ. If the PCI 9030 has no cycles to run, it asserts LGNT, transferring control to the external Master.

If the PCI 9030 requires the Local Bus for a pending PCI Target transaction before the external Master completes, and the PCI 9030 Local Bus Arbiter is configured to give priority to PCI Target accesses over external master ownership of the Local Bus (CNTRL[7]=0), the Local Bus Arbiter de-asserts LGNT regardless of LREQ pin state (default preempt condition). If instead, priority is given to the external Master (CNTRL[7]=1), the Local Bus Arbiter continues to assert LGNT output until the Local Bus Master releases the bus by de-asserting LREQ.

LREQ can be pulled low or grounded to provide permanent Local Bus ownership to the PCI 9030.

2.2.3.4.1   LGNT

LGNT is asserted by the PCI 9030 to grant Local Bus control to a Local Bus Master. When the PCI 9030 requires the Local Bus, it can signal a preempt by de-asserting LGNT, if configured to do so in the Local Arbiter LGNT Signal Select Enable bit (CNTRL[7]=0).

2.2.3.4.2   LREQ

LREQ is asserted by a Local Bus Master to request Local Bus use. The PCI 9030 can be made master of the Local Bus by pulling LREQ low (or by grounding LREQ).

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2.2.3.4.3 Arbitration Timing Diagram
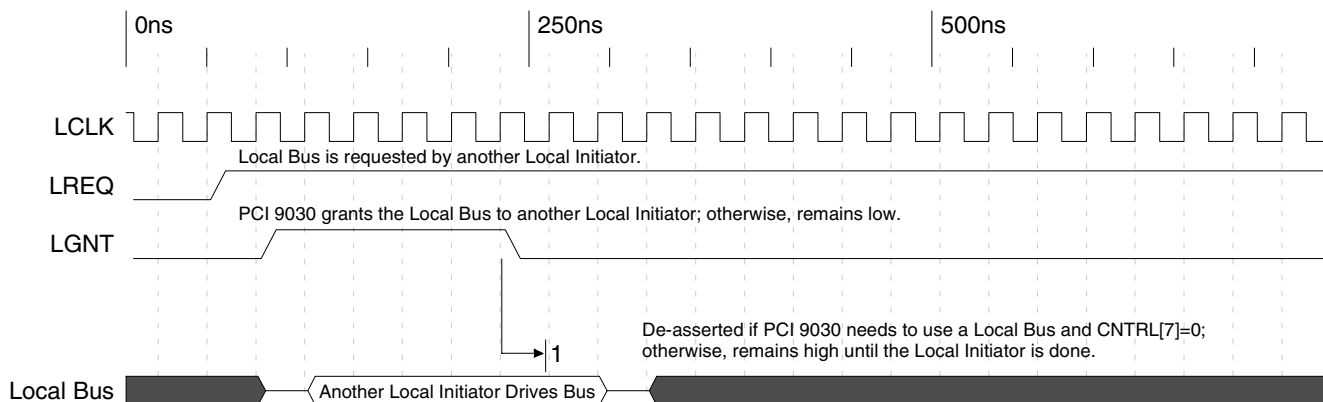
Timing Diagram 2-1. Local Bus Arbitration from the PCI 9030 by Another Local Bus Initiator (LREQ and LGNT)

2.2.4 Local Bus Interface and Bus Cycles

The PCI 9030 is the Local Bus Master. The PCI 9030 interfaces a PCI Host Bus to a Multiplexed or Non-Multiplexed Local Bus, selected by the MODE[1:0] pins, as listed in Table 2-4.

Notes: *No PCI Initiator capability.*
Internal registers are not readable/writable from the Local Bus. The internal registers are accessible from the Host CPU on the PCI Bus or from the serial EEPROM.

Table 2-4. MODE Pin-to-Bus Mode Cross-Reference

MODE Pin	Mode	Bus Width
1	Multiplexed	32-, 16, or 8-Bit
0	Non-Multiplexed	

2.2.4.1 Bus Cycles

In both Non-Multiplexed and Multiplexed modes, the LA[27:2] Address Bus drives an access address valid beginning one clock prior to ADS# assertion (which signals the start of the Bus cycle) and continues until the cycle ends (signaled by BLAST# de-assertion). In Multiplexed mode (MODE=1), the LAD/LD[31:0] Multiplexed Address/Data Bus also drives the access address valid onto LAD/LD[27:0], beginning one clock prior to ADS# assertion and continuing until ADS# de-assertion one clock later, after which data is driven. The LAD/LD[31:0] Data Bus drives Write data valid one clock after ADS# assertion when ADS# de-asserts, and continues until the cycle ends or until data-to-address wait states (or data-to-data wait states

if burst is enabled) begin, if programmed. BLAST# assertion indicates the last Data cycle of an access. (Refer to Figure 2-2 and Figure 2-3.)

Write cycle data valid time and Read cycle data time can be extended with internally generated address-to-data wait states and/or by delaying READY# ready input assertion if READY# input is enabled for the Space. When enabled, READY# input assertion indicates to the PCI 9030 that Read data on the bus is valid to accept or a Write Data transfer has completed. READY# input is not sampled until address-to-data wait states (and/or data-to-data wait states with burst), which are signaled by WAITo# assertion, expire (WAITo# de-asserted). READY# is ignored during the Address cycle (ADS# assertion), internally generated data-to-address wait states, and idle cycles between transfers. BTERM# input, if enabled, is used to break up a Burst access and also serves as a ready input. (Refer to Section 2.2.4.3.)

RD# and WR# strobes can be independently programmed for each Local Address Space. RD# and/or WR# strobe assertion can be optionally delayed during address-to-data wait states. Write Cycle Hold clocks can be selectively programmed to extend data valid time and BLAST# assertion, beyond WR# strobe de-assertion.

Recovery (idle) cycles can be optionally programmed for each Space, using data-to-address wait states (NXDA) to extend time between Local Bus accesses to allow sufficient time for an external device to float its data pins after a Read request.
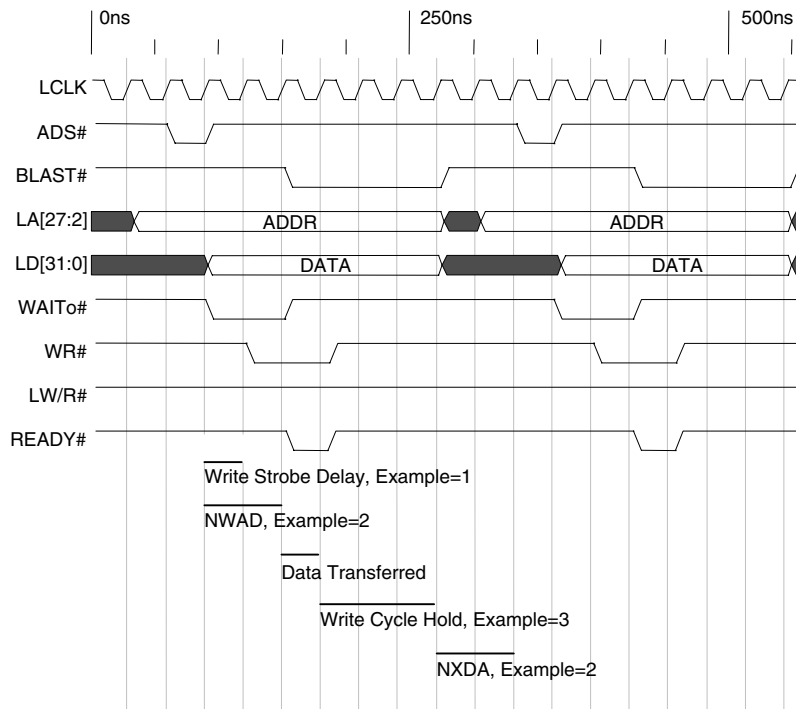
Figure 2-2. PCI 9030 Single Cycle Write

Note: *NWDD is relevant only in a Burst cycle, where it determines the wait state between successive Data cycles.*
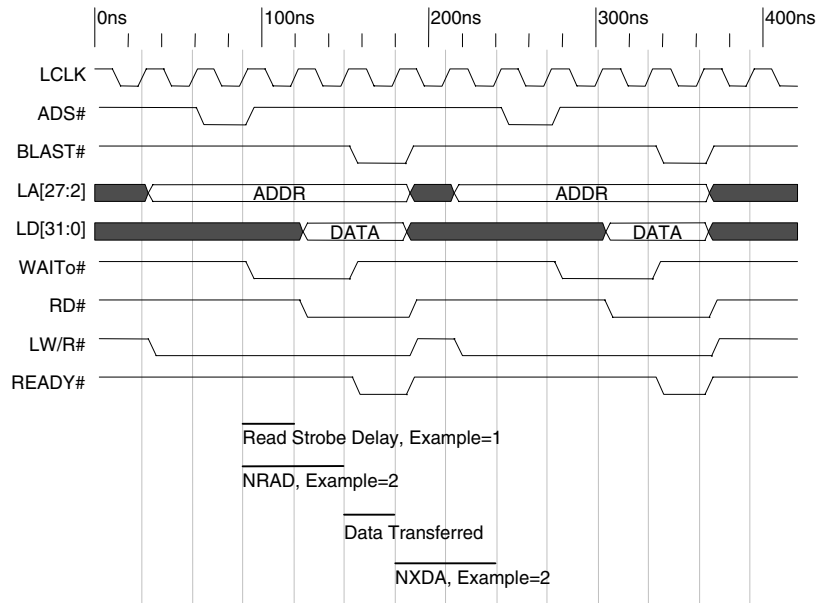
Figure 2-3. PCI 9030 Single Cycle Read

Note: *NRDD is relevant only in a Burst cycle, where it determines the wait state between successive Data cycles.*

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2.2.4.2   Wait State Control

The PCI 9030 as a Local Bus Master signals internal wait states with the WAITo# signal. Local Bus devices can insert external wait states by delaying READY# assertion. (Refer to Figure 2-2 and Figure 2-3.) The following figure illustrates wait state control.
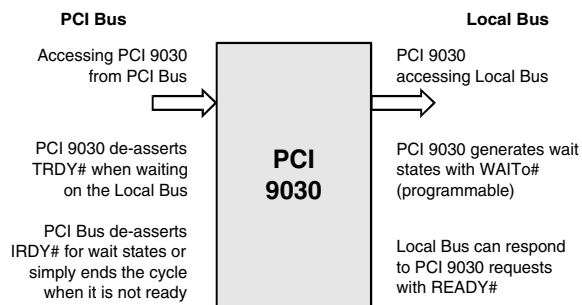
Figure 2-4. Wait States

Note: *The figure represents a sequence of Bus cycles.*

2.2.4.2.1   Internal Wait State Generator

The Local Address Space Bus Region Descriptor can be used to program the number of wait states (if any) generated by the internal wait state generator. (Refer to Table 2-5.)

NXDA wait states are inserted only after the last Data transfer of a Bus request. *For example*, for a PCI Target single Cycle access to an 8-bit burst Local Bus, NXDA wait states are inserted only after the fourth byte, rather than after every byte.

2.2.4.2.2   Ready Signaling

If READY# mode is disabled, the external READY# input signal has no effect on wait states for a Local access. Wait states between Data cycles are inserted internally by a wait state counter. The wait state counter is initialized with its Configuration register value at the start of each Data access.

If READY# mode is enabled and the internal wait state counter is zero (default value), the READY# input controls the number of additional wait states.

If READY# mode is enabled and the internal wait state counter is programmed to a non-zero value, READY# has no effect until the wait state counter reaches 0. When it reaches 0, the READY# input controls the number of additional wait states.

BTERM# input can also be used as a ready input. (Refer to Section 2.2.4.3.) If the internal wait state counter is programmed to a non-zero value and BTERM# is enabled, BTERM# input is not sampled until the wait state counter reaches 0.

Table 2-5. Local Address Space Bus Region Descriptor Internal Wait States

Wait State	Bits	Description
NRAD	LAS*x*BRD[10:6] EROMBRD[10:6]	**N**umber of **R**ead **A**ddress-to-**D**ata wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)
NRDD	LAS*x*BRD[12:11] EROMBRD[12:11]	**N**umber of **R**ead **D**ata-to-**D**ata wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)
NXDA	LAS*x*BRD[14:13] EROMBRD[14:13]	**N**umber of **R**ead/**W**rite **D**ata-to-**A**ddress wait states (0-3). LAD/LD Bus Write data is not valid during NXDA wait states. (Wait states between consecutive bus requests. NXDA wait states are inserted only after the last Data transfer of a PCI Target access.)
NWAD	LAS*x*BRD[19:15] EROMBRD[19:15]	**N**umber of **W**rite **A**ddress-to-**D**ata wait states (0-31). LAD/LD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)
NWDD	LAS*x*BRD[21:20] EROMBRD[21:20]	**N**umber of **W**rite **D**ata-to-**D**ata wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)

Note: *x is the Local Address Space number.*

2.2.4.3 Burst Mode and Continuous Burst Mode (Bterm "Burst Terminate" Mode)

Note: *In the following sections, Bterm refers to the PCI 9030 internal register bit and BTERM# refers to the PCI 9030 external signal.*

2.2.4.3.1 Burst and Bterm Modes

As an input, BTERM# is asserted by external logic. It instructs the PCI 9030 to break up a Burst cycle.

Table 2-6. Burst and Bterm on the Local Bus

Mode	Burst	Bterm	Result
Single Cycle	0	0	One ADS# per data (default)
	0	1	One ADS# per data
Burst-4	1	0	One ADS# per four data
Continuous Burst	1	1	One ADS# per BTERM# (refer to Section 2.2.4.3.3)

On the Local Bus, BLAST# and BTERM# perform the following:

- If Local Bus bursting is enabled for a Local Address space (LAS*x*BRD[0]=1 and/or EROMBRD[0]=1), but Bterm mode (continuous burst) and BTERM# input are disabled (LAS*x*BRD[2]=0 and/or EROMBRD[2]=0), the PCI 9030 bursts up to four Data phases or to the next 16-byte boundary, whichever occurs first. BLAST# is asserted at the beginning of the last Data phase and a new ADS# is asserted at the first Lword-aligned address (LA[3:2]=00) for the next burst.
- If Bterm mode and BTERM# input are enabled (LAS*x*BRD[2]=1 and/or EROMBRD[2]=1) and asserted, the PCI 9030 terminates the Burst cycle at the end of the current Data phase without generating BLAST#. The PCI 9030 generates a new Burst transfer, starting with a new ADS#, and terminating it normally using BLAST#.
- BTERM# input is valid only when the PCI 9030 is performing a PCI Target transaction.
- BTERM# is used to indicate a Memory access is crossing a page boundary or requires a new Address cycle.
- If the internal wait state counter is programmed to a non-zero value and Bterm mode and the BTERM# input are enabled (LAS*x*BRD[2]=1 and/or EROMBRD[2]=1), BTERM# input is not sampled until the wait state counter reaches 0.

- BTERM# always overrides READY#, even if both signals are asserted. BTERM# executes the ongoing transaction and causes the PCI 9030 to initiate a new Address/Data cycle for Burst transactions.

Note: *If Bterm mode (continuous burst) and BTERM# input are disabled (LASxBRD[2]=0 and/or EROMBRD[2]=0), the PCI 9030 performs the following:*

- *32-bit Local Bus—Bursts up to four Lwords*
- *16-bit Local Bus—Bursts up to two Lwords*
- *8-bit Local Bus—Bursts up to one Lword*

In every case, it performs four data beats.

2.2.4.3.2 Burst-4 Mode

If Bterm mode (continuous burst) and BTERM# input are disabled, and Local Bus bursting is enabled for a Local Address space (LASxBRD[2, 0]=01 and/or EROMBRD[2, 0]=01, respectively), bursting can start on any Lword boundary and continue up to a 16-byte address boundary. After data up to the boundary is transferred, the PCI 9030 asserts a new Address cycle (ADS#).

Table 2-7. Burst-4 Mode

Bus Width	Burst
32 bit	Four Lwords or up to a quad Lword boundary (LA[3:2]=11)
16 bit	Four words or up to a quad word boundary (LA[2:1]=11)
8 bit	Four bytes or up to a quad byte boundary (LA[1:0]=11)

2.2.4.3.3 Continuous Burst Mode (Bterm "Burst Terminate" Mode)

If Bterm mode and BTERM# input are enabled, and Local Bus bursting for a Local Address space is enabled (LASxBRD[2, 0]=11 and/or EROMBRD[2, 0]=11, respectively), the PCI 9030 can operate beyond Burst-4 mode.

Bterm mode enables the PCI 9030 to perform long bursts to devices that can accept bursts of longer than four data. The PCI 9030 asserts one Address cycle and continues to burst data. If a device requires a new Address cycle (ADS#), it can assert BTERM# input to cause the PCI 9030 to assert a new Address cycle. The BTERM# input acknowledges the current Data transfer (replacing READY#) and requests that a new Address cycle be asserted (ADS#). The new address is for the next Data transfer. If Bterm mode and

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the BTERM# input are enabled (LAS*x*BRD[2]=1 and/ or EROMBRD[2]=1) and the BTERM# signal is asserted, the PCI 9030 asserts BLAST# only if its Read FIFO is full, its Write FIFO is empty, or a transfer completes.

2.2.4.3.4 Partial Lword Accesses

Partial Lword accesses are Lword accesses in which not all byte enables are asserted.

PCI Target writes always pass the PCI Byte Enables (C/BE[3:0]#) to the Local Byte Enables (LBE[3:0]#). PCI Target Single reads always pass the Byte Enables. PCI Target Burst reads ignore the Byte Enables and return all 32-bit data. (Refer to Table 2-8.)

Local Bus Burst Start addresses can be any Lword boundary. If the Burst Start address in a PCI Target transfer is not aligned to an Lword boundary, the PCI 9030 first performs a single cycle. It then starts to burst on the Lword boundary.

Table 2-8. PCI Target Single and Burst Reads

Bus	PCI Target Single Reads	PCI Target Burst Reads
32-, 16-, or 8-bit Local Bus	Passes the byte enables	Ignores the byte enables and all 32-bit data is passed

2.2.4.4 Recovery States

In Multiplexed mode, the PCI 9030 inserts a minimum of one recovery state between the last Data transfer and the next Address cycle. Add recovery states by programming values greater than 1 into the NXDA bits of the Bus Region Descriptor register(s) (LAS*x*BRD[14:13] and/or EROMBRD[14:13]).

In Non-Multiplexed mode, the PCI 9030 uses the NXDA (data-to-address wait states) value in the Bus Region Descriptor register(s) (LAS*x*BRD[14:13] and/or EROMBRD[14:13]) to determine the number of recovery states to insert between the last Data transfer and next Address cycle. This value can be programmed between 0 and 3 clock cycles (default value is 0).

Note: *The PCI 9030 does not support the i960J function that uses the READY# input to add recovery states. No additional recovery states are added if the READY# input remains asserted during the last Data cycle.*

2.2.4.5 Local Bus Read Accesses

For all single cycle Local Bus Read accesses, the PCI 9030 reads only bytes corresponding to byte enables requested by a PCI Initiator. For all Burst Read cycles, the PCI 9030 can be programmed to:

• Perform PCI Target Delayed Reads
• Perform PCI Target Read Ahead
• Generate internal wait states
• Enable external wait control (READY# input)
• Enable type of Burst mode to perform

2.2.4.6 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Bus Master are written.

For all Burst Write cycles, the PCI 9030 can be programmed to:

• Perform PCI Target delayed writes
• Generate internal wait states
• Enable external wait control (READY# input)

2.2.5 Local Bus Big/Little Endian Mode

For each of the following transfer types, the PCI 9030 Local Bus can be independently programmed to operate in Little Endian or Big Endian mode for PCI Target accesses to Local Address Spaces 0, 1, 2, and 3, and Expansion ROM.

Notes: *The PCI Bus is always Little Endian.*
Only byte lanes are swapped, not individual bits.

The PCI 9030 Local Bus can be programmed to operate in Big or Little Endian mode, as listed in Table 2-9.

Big/Little Endian Control bits are as follows:

• LAS0BRD[24]—Space 0
• LAS1BRD[24]—Space 1
• LAS2BRD[24]—Space 2
• LAS3BRD[24]—Space 3
• EROMBRD[24]—Expansion ROM

In Big Endian mode, the PCI 9030 transposes data byte lanes. Data is transferred as listed in Table 2-10 through Table 2-14.

Table 2-9. Byte Number and Lane Cross-Reference

Byte Number		Byte Lane	
Big Endian	Little Endian	Multiplexed Mode	Non-Multiplexed Mode
3	0	LAD[7:0]	LD[7:0]
2	1	LAD[15:8]	LD[15:8]
1	2	LAD[23:16]	LD[23:16]
0	3	LAD[31:24]	LD[31:24]

2.2.5.1   32-Bit Local Bus— Big Endian Mode

Data is Lword aligned to the uppermost byte lane (Address Invariance).

Table 2-10. Lword Lane Transfer—32-Bit Local Bus

Burst Order	Byte Lane
First Transfer	PCI Byte 0 appears on Local Data [31:24]
	PCI Byte 1 appears on Local Data [23:16]
	PCI Byte 2 appears on Local Data [15:8]
	PCI Byte 3 appears on Local Data [7:0]
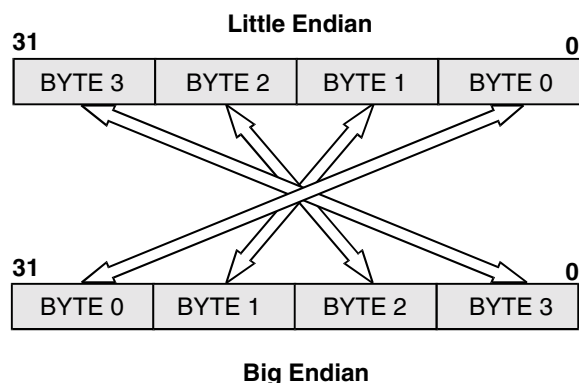
Figure 2-5. Big/Little Endian—32-Bit Local Bus

2.2.5.2   16-Bit Local Bus— Big Endian Mode

For a 16-bit Local Bus, the PCI 9030 can be programmed to use upper or lower word lanes.

Table 2-11. Upper Word Lane Transfer— 16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 2-12. Lower Word Lane Transfer— 16-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]
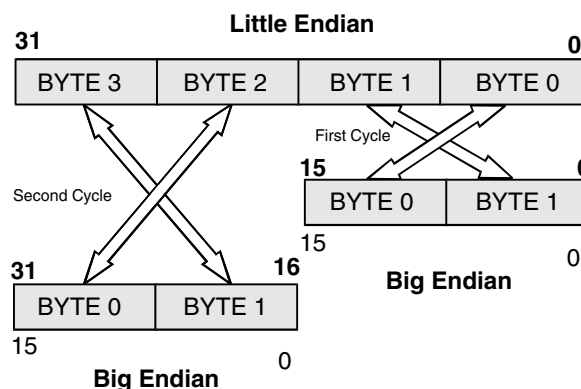
Figure 2-6. Big/Little Endian—16-Bit Local Bus

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2.2.5.3 8-Bit Local Bus—Big Endian Mode

For an 8-bit Local Bus, the PCI 9030 can be programmed to use upper or lower byte lanes.

Table 2-13. Upper Byte Lane Transfer—8-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
Second Transfer	Byte 1 appears on Local Data [31:24]
Third Transfer	Byte 2 appears on Local Data [31:24]
Fourth Transfer	Byte 3 appears on Local Data [31:24]

Table 2-14. Lower Byte Lane Transfer—8-Bit Local Bus

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]
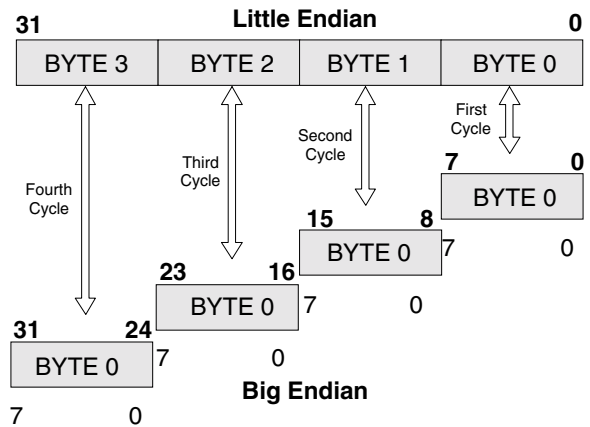
Figure 2-7. Big/Little Endian—8-Bit Local Bus

3   SERIAL EEPROM RESET AND INITIALIZATION

3.1   INITIALIZATION

During power-on, the PCI RST# signal resets the default values of the PCI 9030 internal registers. In return, the PCI 9030 outputs the local LRESETo# signal and checks for a serial EEPROM. If a serial EEPROM exists, and the first 33 bits are not all ones (1), the PCI 9030 loads the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9030 Configuration registers can be written only by the optional serial EEPROM or PCI Host processor. During serial EEPROM initialization, the PCI 9030 response to Direct Slave accesses is Retrys.

3.2   RESET

3.2.1   PCI Bus RST# Input

PCI Bus RST# input assertion causes all PCI Bus outputs to float, asserts both Local reset outputs LRESETo# and LEDon#, and floats all other Local Bus output and I/O pins, except BCLKo, EECS, EEDI, EESK, ENUM#, LGNT, LPMINT#, multiplexed I/O pins LA[27:24]/GPIO[4:7], and the Local Data Bus signals. The LA[27:24]/GPIO[4:7] multiplexed I/O pins, and the Non-multiplexed mode LD[31:0] data or Multiplexed mode LAD[31:0] address/data I/O pins, are driven low during PCI reset. (Refer to *PCI 9030 Errata #4.*)

3.2.2   Software Reset

A PCI host can set the PCI Adapter Software Reset bit (CNTRL[30]=1) to reset the PCI 9030 and assert LRESETo#. The PCI and Local Configuration register contents are not reset as a result. When the Software Reset bit is set, the PCI 9030 responds only to Configuration register accesses, and not to Local Bus accesses. The PCI 9030 remains in this reset condition until the PCI Host clears the bit (CNTRL[30]=0). The PCI Interface is not reset.

Note: If PCI Target Read Ahead mode is enabled (CNTRL[16]=1), disable it prior to a software reset, or if following a software reset, perform a PCI Target read of any valid Local Bus address, except the next sequential Lword referenced from the last PCI Target read, to flush the PCI Target Read FIFO.

3.2.3   Local Bus Output LRESETo#

LRESETo# is asserted when the PCI Bus RST# input is asserted or the PCI Adapter Software Reset bit is set (CNTRL[30]=1).

3.3   SERIAL EEPROM

After reset, the PCI 9030 attempts to read the serial EEPROM to determine its presence. An active start bit set to 0 indicates a serial EEPROM is present. The PCI 9030 supports 93CS56L (2K bit) or 93CS66L (4K bit). (Refer to manufacturer's data sheet for the particular serial EEPROM being used.) The first 33 bits are then checked to verify that the serial EEPROM is programmed. If the first 33 bits are all ones (1), a blank serial EEPROM is present.

For blank serial EEPROM conditions, the PCI 9030 reverts to the default values. (Refer to Table 3-1.) When the Serial EEPROM Valid bit is set to 1 (CNTRL[28]=1), if programmed, real or random data is detected in the serial EEPROM.

An active Start bit set to 1 indicates that a serial EEPROM is not present. For missing serial EEPROM conditions, the PCI 9030 stops the serial EEPROM load and reverts to the default values within 13 serial EEPROM clocks (EESK).

The 3.3V serial EEPROM clock is derived from the PCI clock, generated by the PCI 9030 by internally dividing the PCI clock by 132.

The serial EEPROM can be read or written from the PCI Bus. The Serial EEPROM Control Register bits (CNTRL[28:24]) control the PCI 9030 pins that enable reading or writing of serial EEPROM data bits. (Refer to manufacturer's data sheet for the particular serial EEPROM being used.)

To reload serial EEPROM data into the PCI 9030 internal registers, write 1 to the Reload Configuration Registers bit (CNTRL[29]=1).

The serial EEPROM can also be read or written, using the VPD function. (Refer to Section 9.) The PCI 9030 loads 34 Lwords from the serial EEPROM.

Table 3-1. Serial EEPROM Guidelines

Serial EEPROM	PCI 9030 System Boot Condition
None	Uses default values (Start bit is 1).
Programmed	Boots with serial EEPROM values (Start bit is 0).
Blank	Detects a blank device and reverts to default values (Start bit is 0).

3.3.1 Serial EEPROM Load Sequence

The serial EEPROM load sequence, listed in Table 3-2, uses the following abbreviations:

- **MSW** = Most Significant Word bits [31:16]
- **LSW** = Least Significant Word bits [15:0]

3.3.1.1 Serial EEPROM Load

The registers listed in Table 3-2 are loaded from the serial EEPROM after a PCI reset is de-asserted. The serial EEPROM is organized in words (16 bit). The PCI 9030 first loads the Most Significant Word bits (MSW[31:16]), starting from the most significant bit ([31]). The PCI 9030 then loads the Least Significant Word bits (LSW[15:0]), starting again from the most significant bit ([15]). Therefore, the PCI 9030 loads the Device ID, Vendor ID, Class Code, and so forth.

The serial EEPROM values can be programmed using a serial EEPROM programmer or PLXMon™ software. The values can be programmed using the PCI 9030 VPD function (refer to Section 9) or through the Serial EEPROM Control register (CNTRL).

The CNTRL register allows programming of the serial EEPROM, one bit at a time. To read back the value from the serial EEPROM, the Vital Product Data (VPD) function can be utilized. With full utilization of VPD, the designer can perform reads and writes from/to the serial EEPROM, 32 bits at a time. Values should be programmed in the order listed in Table 3-2. The 68, 16-bit words listed in the table are stored sequentially in the serial EEPROM.

3.3.1.2 Recommended Serial EEPROMs

The PCI 9030 is designed to use serial EEPROMs with a three-wire serial interface, powered at 3.3V, and that support 250 kHz clocking and sequential reads.

For specific EEPROM recommendations, refer to the EEPROM Guidelines posted on the PLX website, http://www.plxtech.com/products/default.htm.
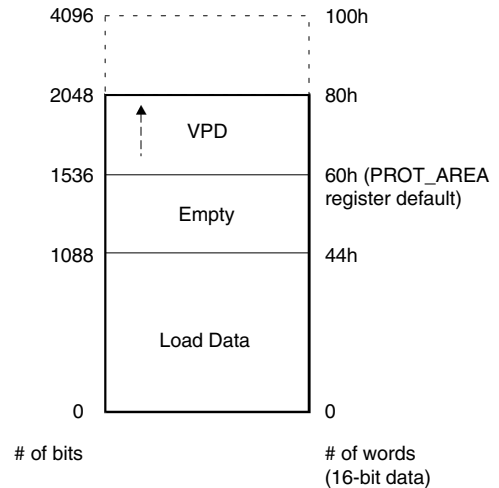
Figure 3-1. Serial EEPROM Memory Map

Table 3-2. Serial EEPROM Register Load Sequence

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected
00h	PCI 02h	Device ID	PCIIDR[31:16]
02h	PCI 00h	Vendor ID	PCIIDR[15:0]
04h	PCI 06h	PCI Status	PCISR[15:0]
06h	PCI 04h	PCI Command	*Reserved*
08h	PCI 0Ah	Class Code	PCICCR[15:0]
0Ah	PCI 08h	Class Code / Revision	PCICCR[7:0] / PCIREV[7:0]
0Ch	PCI 2Eh	Subsystem ID	PCISID[15:0]
0Eh	PCI 2Ch	Subsystem Vendor ID	PCISVID[15:0]
10h	PCI 36h	MSB New Capability Pointer	*Reserved*
12h	PCI 34h	LSB New Capability Pointer	CAP_PTR[7:0]
14h	PCI 3Eh	(Maximum Latency and Minimum Grant are not loadable)	*Reserved*
16h	PCI 3Ch	Interrupt Pin (Interrupt Line Routing is not loadable)	PCIIPR[7:0] / PCIILR [7:0]
18h	PCI 42h	MSW of Power Management Capabilities	PMC[15:11, 5, 3:0]
1Ah	PCI 40h	LSW of Power Management Next Capability Pointer / Power Management Capability ID	PMNEXT[7:0] / PMCAPID[7:0]
1Ch	PCI 46h	MSW of Power Management Data / PMCSR Bridge Support Extension	*Reserved*
1Eh	PCI 44h	LSW of Power Management Control/Status	PMCSR[14:8]
20h	PCI 4Ah	MSW of Hot Swap Control/Status	*Reserved*
22h	PCI 48h	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]
24h	PCI 4Eh	PCI Vital Product Data Address	*Reserved*
26h	PCI 4Ch	PCI Vital Product Data Next Capability Pointer / PCI Vital Product Data Control	PVPD_NEXT[7:0] / PVPDCNTL[7:0]
28h	Local 02h	MSW of Local Address Space 0 Range	LAS0RR[31:16]
2Ah	Local 00h	LSW of Local Address Space 0 Range	LAS0RR[15:0]
2Ch	Local 06h	MSW of Local Address Space 1 Range	LAS1RR[31:16]
2Eh	Local 04h	LSW of Local Address Space 1 Range	LAS1RR[15:0]
30h	Local 0Ah	MSW of Local Address Space 2 Range	LAS2RR[31:16]
32h	Local 08h	LSW of Local Address Space 2 Range	LAS2RR[15:0]
34h	Local 0Eh	MSW of Local Address Space 3 Range	LAS3RR[31:16]
36h	Local 0Ch	LSW of Local Address Space 3 Range	LAS3RR[15:0]
38h	Local 12h	MSW of Expansion ROM Range	EROMRR[31:16]
3Ah	Local 10h	LSW of Expansion ROM Range	EROMRR[15:0]
3Ch	Local 16h	MSW of Local Address Space 0 Local Base Address (Remap)	LAS0BA[31:16]
3Eh	Local 14h	LSW of Local Address Space 0 Local Base Address (Remap)	LAS0BA[15:0]

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Table 3-2. Serial EEPROM Register Load Sequence (Continued)

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected
40h	Local 1Ah	MSW of Local Address Space 1 Local Base Address (Remap)	LAS1BA[31:16]
42h	Local 18h	LSW of Local Address Space 1 Local Base Address (Remap)	LAS1BA[15:0]
44h	Local 1Eh	MSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[31:16]
46h	Local 1Ch	LSW of Local Address Space 2 Local Base Address (Remap)	LAS2BA[15:0]
48h	Local 22h	MSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[31:16]
4Ah	Local 20h	LSW of Local Address Space 3 Local Base Address (Remap)	LAS3BA[15:0]
4Ch	Local 26h	MSW of Expansion ROM Local Base Address (Remap)	EROMBA[31:16]
4Eh	Local 24h	LSW of Expansion ROM Local Base Address (Remap)	EROMBA[15:0]
50h	Local 2Ah	MSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[31:16]
52h	Local 28h	LSW of Local Address Space 0 Bus Region Descriptor	LAS0BRD[15:0]
54h	Local 2Eh	MSW of Local Address Space 1 Bus Region Descriptor	LAS1BRD[31:16]
56h	Local 2Ch	LSW of Local Address Space 1 Bus Region Descriptor	LAS1BRD[15:0]
58h	Local 32h	MSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[31:16]
5Ah	Local 30h	LSW of Local Address Space 2 Bus Region Descriptor	LAS2BRD[15:0]
5Ch	Local 36h	MSW of Local Address Space 3 Bus Region Descriptor	LAS3BRD[31:16]
5Eh	Local 34h	LSW of Local Address Space 3 Bus Region Descriptor	LAS3BRD[15:0]
60h	Local 3Ah	MSW of Expansion ROM Bus Region Descriptor	EROMBRD[31:16]
62h	Local 38h	LSW of Expansion ROM Bus Region Descriptor	EROMBRD[15:0]
64h	Local 3Eh	MSW of Chip Select 0 Base Address	CS0BASE[31:16]
66h	Local 3Ch	LSW of Chip Select 0 Base Address	CS0BASE[15:0]
68h	Local 42h	MSW of Chip Select 1 Base Address	CS1BASE[31:16]
6Ah	Local 40h	LSW of Chip Select 1 Base Address	CS1BASE[15:0]
6Ch	Local 46h	MSW of Chip Select 2 Base Address	CS2BASE[31:16]
6Eh	Local 44h	LSW of Chip Select 2 Base Address	CS2BASE[15:0]
70h	Local 4Ah	MSW of Chip Select 3 Base Address	CS3BASE[31:16]
72h	Local 48h	LSW of Chip Select 3 Base Address	CS3BASE[15:0]
74h	Local 4Eh	Serial EEPROM Write-Protected Address Boundary	PROT_AREA[7:0]
76h	Local 4Ch	LSW of Interrupt Control/Status	INTCSR[15:0]
78h	Local 52h	MSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[31:16]
7Ah	Local 50h	LSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[15:0]
7Ch	Local 56h	MSW of General Purpose I/O Control	GPIOC[31:16]
7Eh	Local 54h	LSW of General Purpose I/O Control	GPIOC[15:0]

Table 3-2. Serial EEPROM Register Load Sequence (Continued)

Serial EEPROM Offset	Register Offset	Register Description	Register Bits Affected
80h	Local 72h	MSW of Hidden 1 Power Management Data Select (refer to Section 7.2.1)	PMDATA[7:0] hidden, D_0 and D_{3hot} Power Dissipated
82h	Local 70h	LSW of Hidden 1 Power Management Data Select (refer to Section 7.2.1)	PMDATA[7:0] hidden, D_0 and D_{3hot} Power Consumed
84h	Local 76h	MSW of Hidden 2 Power Management Data Scale (refer to Section 7.2.1)	*Reserved*
86h	Local 74h	LSW of Hidden 2 Power Management Data Scale (refer to Section 7.2.1)	PMCSR[14:13] hidden, Bits [7:0] are used as follows: [7:6] D_{3hot} Power Dissipated, [5:4] D_0 Power Dissipated, [3:2] D_{3hot} Power Consumed, [1:0] D_0 Power Consumed

<div style="text-align: right">3—Serial EEPROM</div>

3.4   INTERNAL REGISTER ACCESS

The PCI 9030 provides several internal registers, which allow for maximum flexibility in the bus-interface design and performance. These registers are accessible from the PCI and Local Buses (refer to Figure 3-2) and include the following:

• PCI Configuration
• Local Configuration
• Power Management
• Hot Swap
• VPD
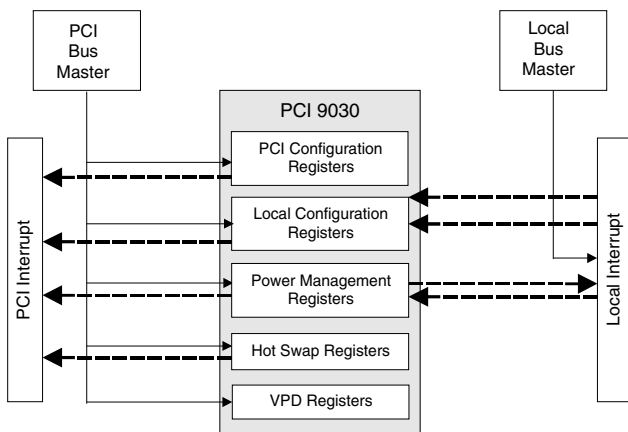
Figure 3-2. PCI 9030 Internal Register Access

Note: *Local Configuration register access can be limited to Memory- or I/O-Mapped. Access can be disabled by way of the PCIBAR1 and PCIBAR0 Enable bits (CNTRL[13:12]). These bits should not be disabled for the PC platform.*

3.4.1   PCI Configuration Registers

Device and Vendor IDs. There are two sets of Device and Vendor IDs. The Device ID and Vendor ID are located at offset 00h of the PCI Configuration registers (PCIIDR[31:16] and PCIIDR[15:0], respectively). The Subsystem ID and Subsystem Vendor ID are located at offsets 2Eh and 2Ch, respectively, of the PCI Configuration registers (PCISID[15:0] and PCISVID [15:0], respectively). The Device ID and Vendor ID identify the particular device and its manufacturer. The Subsystem Vendor ID and Subsystem ID provide a way to distinguish between PCI interface chip vendors and add-in board manufacturers, using a PCI chip.

Status. This register contains PCI Bus-related events information.

Command. This register controls the ability of a device to respond to PCI accesses. It controls whether the device responds to I/O or Memory Space accesses.

Class Code. This register identifies the general function of the device. (Refer to *PCI r2.2* for further details.)

Revision ID. The value read from this register represents the PCI 9030 current silicon revision.

Header Type. This register defines the device configuration header format and whether the device is single function or multi-function.

Note: Multiple functions are not supported.

Cache Line Size. This register defines the system cache line size in units of 32-bit Lwords.

PCI Base Address for Memory Accesses to Local Configuration Registers. The system BIOS uses this register to assign a PCI Address space segment for Memory accesses to the PCI 9030 Local Configuration registers. The PCI Address Range occupied by these Configuration registers is fixed at 128 bytes. During initialization, the Host writes FFFFFFFF to this register, then reads back FFFFFF80, determining the required Memory space of 128 bytes. The Host then writes the base address to PCIBAR0[31:7].

PCI Base Address for I/O Accesses to Local Configuration Registers. The system BIOS uses this register to assign a PCI address space segment for I/O accesses to the PCI 9030 Local Configuration registers. The PCI address range occupied by these Configuration registers is fixed at 128 bytes. During initialization, the host writes FFFFFFFF to this register, then reads back FFFFFF81, determining a required 128 bytes of I/O space. The Host then writes the base address to PCIBAR1[31:7].

PCI Base Address for Accesses to Local Address Spaces 0, 1, 2, and 3. The system BIOS uses these registers to assign a PCI address space segment for accesses to Local Address Space 0, 1, 2, and 3. The PCI address range occupied by this space is determined by the Local Address Space Range registers. During initialization, the host writes FFFFFFFF to these registers, then reads back a value determined by the range. The Host then writes the base address to the upper bits of these registers.

PCI Expansion ROM Base Address. The system BIOS uses this register to assign a PCI address space segment for accesses to the Expansion ROM. The PCI address range occupied by this space is determined by the Expansion ROM Range register. During initialization, the Host writes FFFFFFFF to this register, then reads back a value determined by the range. The Host then writes the base address to the upper bits of this register.

PCI Interrupt Line. Indicates to which system interrupt controller(s) input the interrupt line is connected. The PCI 9030 does not use this value, rather the value is used by device drivers and operating systems for priority and vector information. Values in this register are system-architecture specific.

PCI Interrupt Pin. This register specifies the interrupt request pin (if any) to be used. The PCI 9030 supports INTA#, but not INTB#, INTC#, nor INTD#.

3.4.2 PCI Bus Access to Internal Registers

The PCI 9030 PCI Configuration registers can be accessed from the PCI Bus with a Type 0 Configuration cycle.

All other PCI 9030 internal registers can be accessed by a Memory cycle, with the PCI Bus address that matches the base address specified in PCI Base Address 0 (PCIBAR0[31:4]) for the PCI 9030 Memory-Mapped Configuration register. These registers can also be accessed by an I/O cycle, with the PCI Bus address matching the base address specified in PCI Base Address 1 (PCIBAR1[31:2] for the PCI 9030 I/O-Mapped Configuration register.

All PCI Read or Write accesses to the PCI 9030 registers can be Byte, Word, or Lword accesses. All PCI Memory accesses to the PCI 9030 registers can be Burst or Non-Burst accesses. The PCI 9030 responds with a PCI Bus disconnect for all Burst I/O accesses (PCIBAR1[31:2]) to the PCI 9030 Internal registers.

3.5 NEW CAPABILITIES FUNCTION SUPPORT

The New Capabilities Function Support includes PCI Power Management, Hot Swap, and VPD features, as listed in the following table. [For further information on these features, refer to Section 7, "PCI Power Management," Section 8, "CompactPCI Hot Swap," and Section 9, "PCI Vital Product Data (VPD)."]

Table 3-3. New Capabilities Function Support Features

New Capability Function	PCI Register Offset Location
First (Power Management)	40h, which is pointed to, from CAP_PTR [7:0].
Second Hot Swap)	48h, which is pointed to, from PMNEXT[7:0].
Third (VPD)	4Ch, which is pointed to, from HS_NEXT[7:0]. Because PVPD_NEXT[7:0] defaults to zero (0), this indicates that VPD is the last PCI 9030 New Capability Function Support feature.

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3.6   SERIAL EEPROM AND CONFIGURATION INITIALIZATION TIMING DIAGRAMS
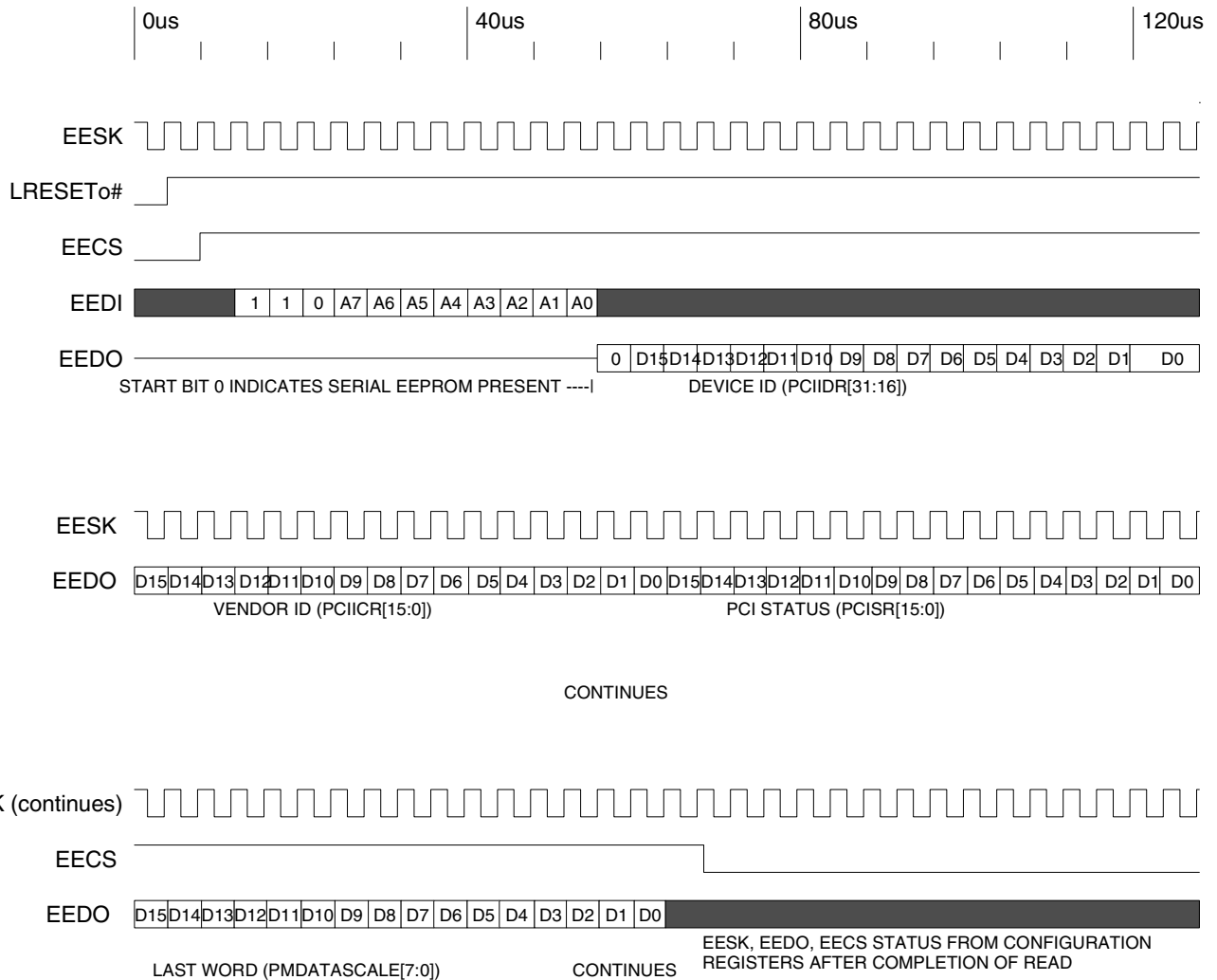
Note: Serial EEPROM initialization completes in approximately 4.35 ms with a 33.3 MHz PCI clock.

Timing Diagram 3-1. Initialization from Serial EEPROM (2K or 4K Bit)
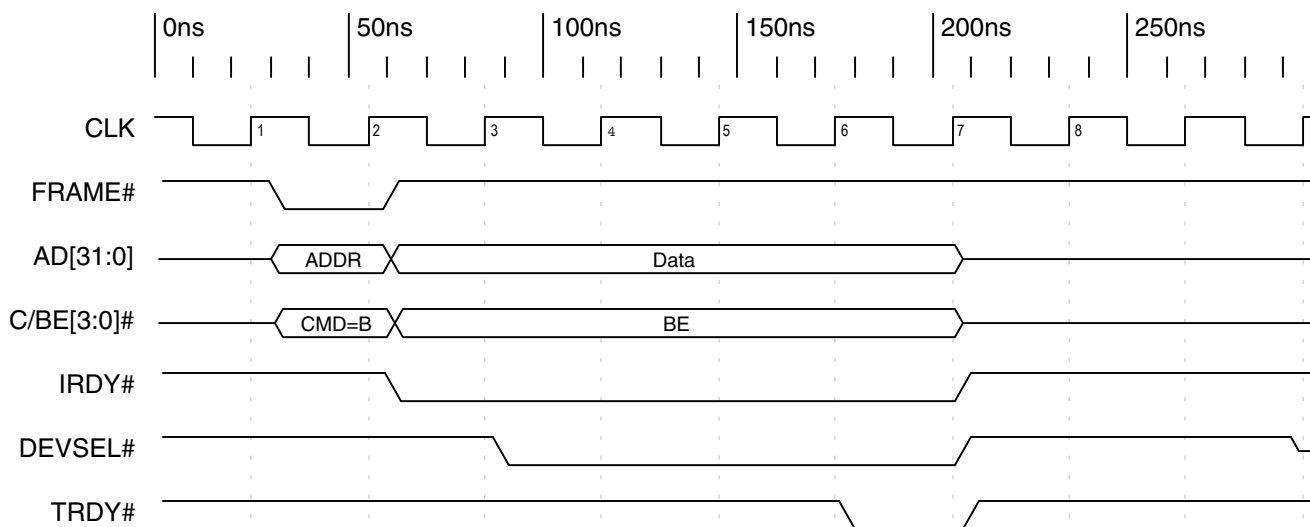
Timing Diagram 3-2. PCI Configuration Write to PCI Configuration Register
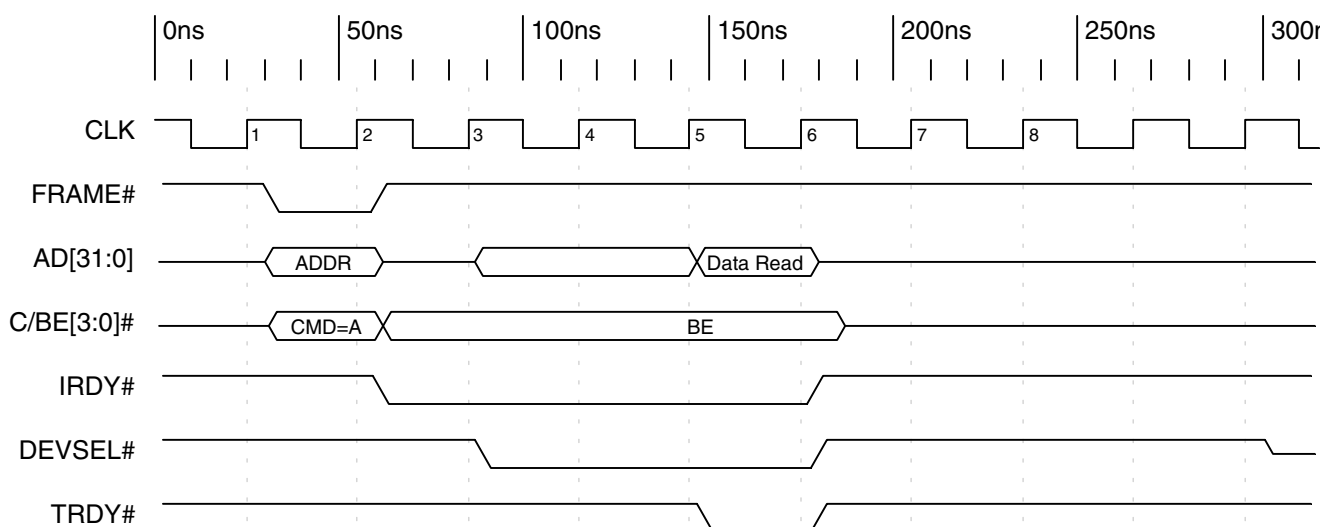
Timing Diagram 3-3. PCI Configuration Read from PCI Configuration Register
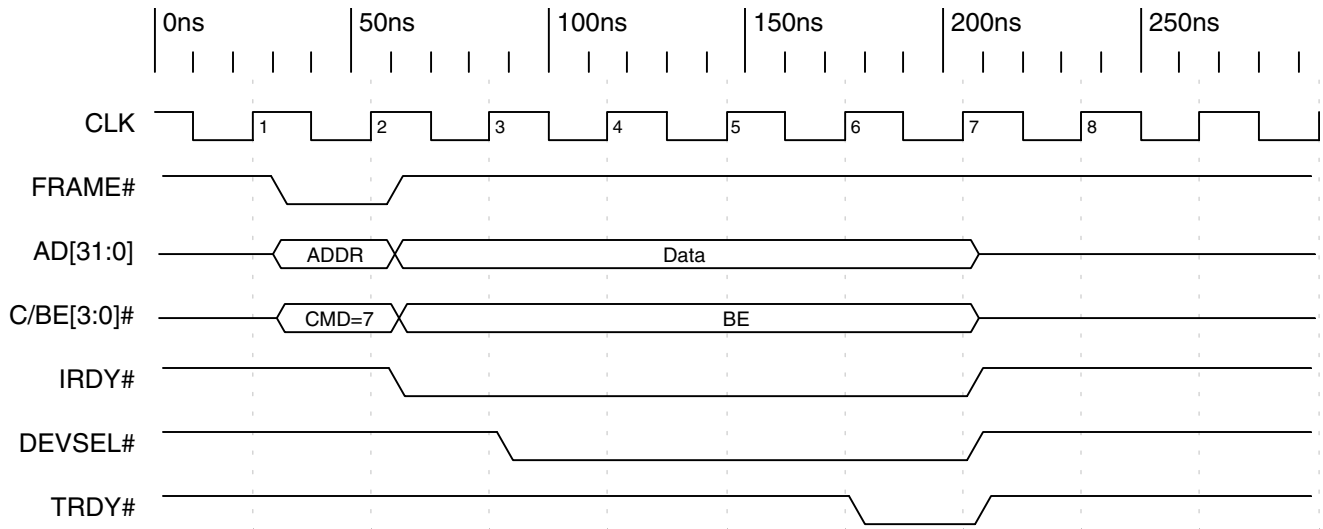
Timing Diagram 3-4. PCI Memory Write to Local Configuration Register
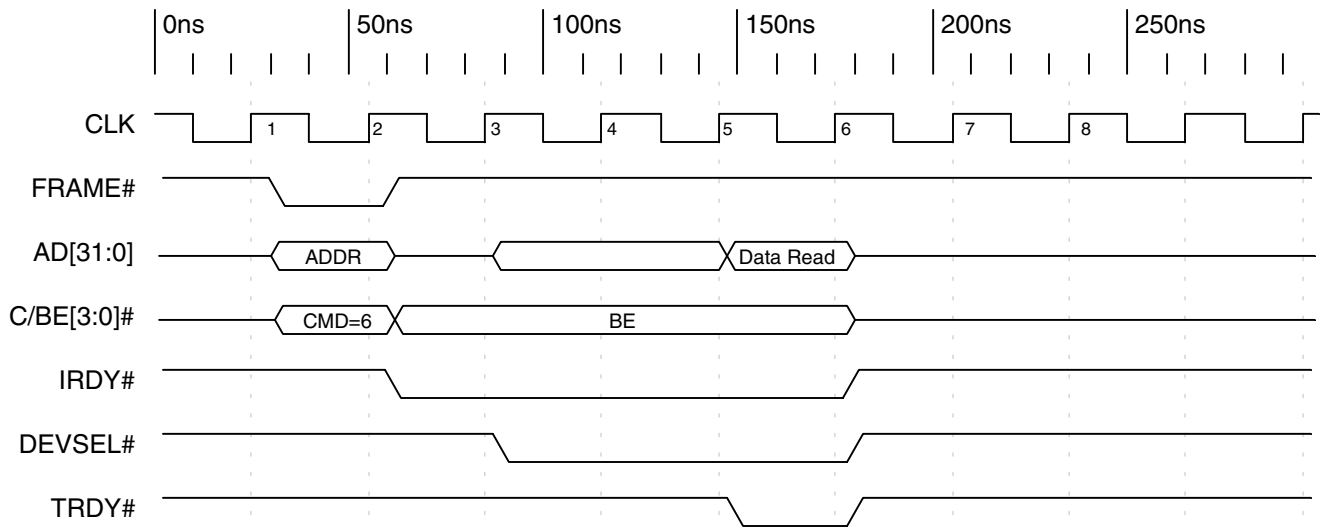
Timing Diagram 3-5. PCI Memory Read from Local Configuration Register

4   PCI TARGET (DIRECT SLAVE) OPERATION

Functional operation described can be modified through the PCI 9030 programmable internal registers.

4.1   OVERVIEW

PCI Target (Direct Slave) operations originate on the PCI Bus, go through the PCI 9030, and finally access the Local Bus. The PCI 9030 is a PCI Bus target and a Local Bus master.

4.2   DIRECT DATA TRANSFER MODE

The PCI 9030 supports PCI Target accesses to Local Memory or I/O Transfer mode.

4.2.1   PCI Target Operation (PCI Master-to-Local Bus Access)

The PCI 9030 supports Burst Memory-Mapped Transfer accesses and I/O-Mapped, Single-Transfer accesses to the Local Bus from the PCI Bus through a 16-Lword (64-byte) PCI Target Read FIFO and a 32-Lword (128-byte) PCI Target Write FIFO. The PCI Base Address registers are provided to set up the adapter location in the PCI memory and I/O space. In addition, Local Mapping registers allow address translation from the PCI Address Space to the Local Address Space. Five spaces are available:

- Space 0
- Space 1
- Space 2
- Space 3
- Expansion ROM

Expansion ROM is intended to support a bootable ROM device for the Host.

For single cycle PCI Target reads, the PCI 9030 reads a single Local Bus Lword or partial Lword. The PCI 9030 disconnects after one transfer for all PCI Target I/O accesses.

For highest data-transfer rates, the PCI 9030 supports posted writes. Memory-mapped address spaces can be selectively enabled to prefetch data to support PCI Burst reads. A Prefetch Counter for each Local address space controls whether prefetch is enabled and continuous, or limited to a finite number of accesses. (Refer to Section 4.2.1.3.)

If prefetch is enabled for a Local address space, the PCI 9030 can also be programmed to support PCI Target Read Ahead mode. (Refer to Section 4.2.1.4.)

Each Local space can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width. The PCI 9030 contains an internal wait state generator and external wait state input, READY#. READY# can be selectively enabled or disabled for each local address space in the corresponding LAS*x*BRD and/or EROMBRD registers.

With or without wait state(s), the Local Bus, independent of the PCI Bus, can:

- Burst as long as data is available (Continuous Burst mode)
- Burst four data at a time (Burst-4 mode)
- Perform continuous single cycles

4.2.1.1   PCI Target Lock

The PCI 9030 supports direct PCI-to-Local-Bus Exclusive accesses (locked atomic operations). A PCI-locked operation to the Local Bus results in the entire address Spaces 0, 1, 2, and 3, and Expansion ROM being locked until they are released by the PCI Bus Master. Locked operations are enabled or disabled with the PCI Target LOCK# Enable bit (CNTRL[23]) for PCI-to-Local accesses.

It is the responsibility of external arbitration logic to monitor the LLOCKo# pin and enforce the meaning for an atomic operation. *For example*, if a local master initiates a locked operation, the Local Bus Arbiter may choose to not grant use of the Local Bus to other masters until the locked operation completes.

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4.2.1.2 *PCI r2.2* Features Enable

The PCI 9030 can be programmed through the *PCI r2.2* Features Enable bit (CNTRL[14]) to perform all PCI Read/Write transactions in compliance with *PCI r2.2*. The following PCI 9030 behavior occurs when CNTRL[14]=1.

4.2.1.2.1 PCI Target Delayed Read Mode

PCI Bus single cycle aligned or unaligned PCI Target Read transactions always result in a one-Lword single cycle transfer on the Local Bus, with corresponding Local Byte Enables (LBE[3:0]#), asserted to reflect PCI Byte Enables (C/BE[3:0]#), unless the PCI Read No Flush Mode bit is enabled (CNTRL[16]=1). (Refer to Section 4.2.1.4.) This causes the PCI 9030 to Retry all PCI Bus Read requests that follow, until the original PCI Address and PCI Byte Enables (C/BE[3:0]#) are matched. (Refer to Figure 4-1.)
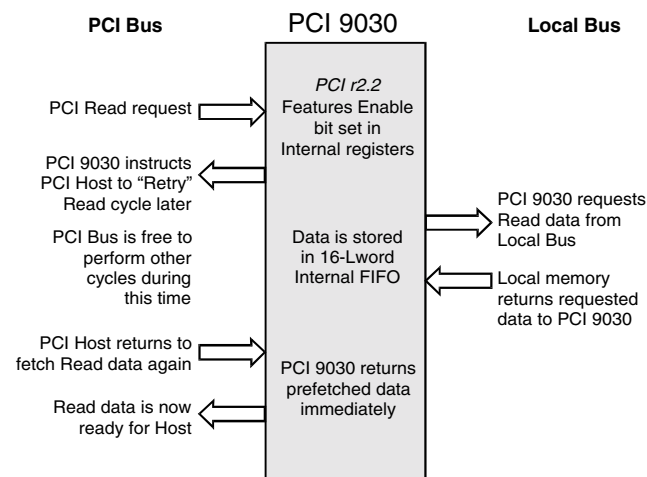
Figure 4-1. PCI Target Delayed Read Mode

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.2.2 2^{15} PCI Clock Timeout

If the PCI Master does not complete the originally requested PCI Target Delayed Read transfer, the PCI 9030 flushes the PCI Target Read FIFO after 2^{15} PCI clocks and grants an access to a new PCI Target Read access. The PCI 9030 Retries all other PCI Target Read accesses that occur before the 2^{15} PCI Clock timeout, provided the Disconnect with Flush Read FIFO bit is disabled (CNTRL[31]=0, default). If enabled (CNTRL[31]=1), a new PCI Target Read access flushes any pending delayed reads from the Read FIFO and the new Read request is granted.

4.2.1.2.3 *PCI r2.2* 16- and 8-Clock Rule

The PCI 9030 guarantees that if the first PCI Target Write data cannot be accepted by the PCI 9030 and/or the first PCI Target Read data cannot be returned by the PCI 9030 within 16 PCI clocks from the beginning of the PCI Target cycle (FRAME# asserted), the PCI 9030 issues a Retry (STOP# asserted) to the PCI Bus.

During successful PCI Target Read and/or Write accesses, the subsequent data after the first access is accepted for writes or returned for reads in eight PCI clocks (TRDY# asserted). Otherwise, the PCI 9030 issues a PCI disconnect (STOP# asserted) to the PCI Master.

In addition, setting the *PCI r2.2* Features Enable bit [CNTRL[14]=1) allows optional enabling of the following *PCI r2.2* functions:

- No write while a Delayed Read is pending (PCI Retries for writes) (CNTRL[17])
- Write and flush pending Delayed Read (CNTRL[15])

4.2.1.3   Local Bus Prefetch

Memory-Mapped PCI 9030 Local address spaces can be selectively programmed to enable a Local Bus prefetch (enabled by default in LAS*x*BRD[5:3]). A Prefetch Counter for each space controls the number of prefetches to perform in conjunction with each PCI Target read. When the Prefetch Counter is enabled (LAS*x*BRD[5]=1), the Prefetch Count (LAS*x*BRD[4:3]) can be set to 0 (disabling prefetch), or to 4, 8 or 16 Lwords (independent of Local Bus width). If the Prefetch Counter is disabled (LAS*x*BRD[5]=0), the PCI 9030 performs continuous prefetches.

When a PCI Target read is performed and a Local Bus prefetch is enabled for the Local Address space, the PCI 9030 fetches the requested data and continues to read data from sequential addresses (anticipating the PCI Master eventually consuming the additional data). When the PCI 9030 prefetches, if the Prefetch Counter is enabled, the PCI 9030 stops reading from the Local Bus read after reaching the Prefetch Count limit. In Continuous Prefetch mode, if PCI Target Read Ahead mode is disabled (CNTRL[16]=0) (refer to Section 4.2.1.4), the PCI 9030 prefetches as long as space is available in its FIFO, and stops prefetching a few PCI clocks after the PCI Master completes its read. If both Continuous Prefetch and PCI Target Read Ahead modes are enabled, the PCI 9030 continues to prefetch until the Read FIFO is full. If prefetch is disabled (LAS*x*BRD[5:3]=100), or the address space is mapped as I/O, the PCI 9030 stops after one Read transfer.

Local prefetch must be enabled if PCI Burst reads and Read Ahead mode are utilized.

Refer to Section 2.1.1.4 regarding mapping of PCI 9030 address spaces into an upstream bridge's Prefetchable Base and Limit registers.

4.2.1.4   PCI Target Read Ahead Mode

The PCI 9030 also supports PCI Target Read Ahead mode (CNTRL[16]), where prefetched data can be read from the PCI 9030 internal FIFO instead of the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). The PCI Target Read Ahead mode functions can be used with or without PCI Target Delayed Read mode. (Refer to Figure 4-2.)

Read Ahead mode requires that Prefetch be enabled in the LAS*x*BRD and/or EROMBRD registers for the Memory-Mapped spaces that use Read Ahead mode. The PCI 9030 flushes its Read FIFO for each I/O-Mapped access.
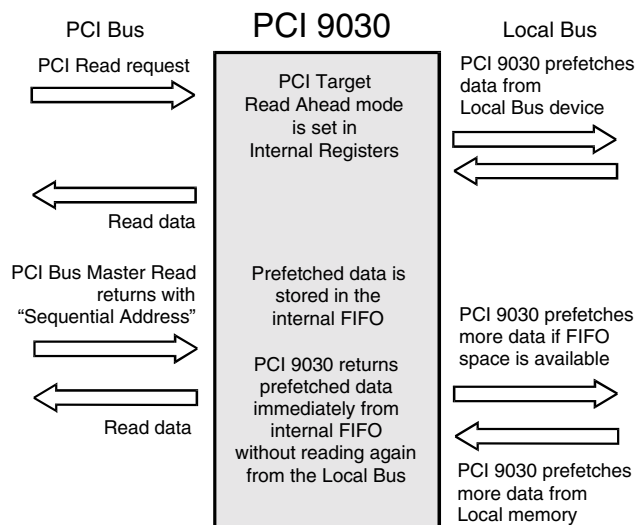
Figure 4-2. PCI Target Read Ahead Mode

Note: *The figure represents a sequence of Bus cycles.*

4.2.1.5   PCI Target Delayed Write Mode

The PCI 9030 supports PCI Target Delayed Write mode transactions, where posted Write data accumulates in the PCI Target Write FIFO before the PCI 9030 requests a Write transaction (ADS# and/or ALE assertion) to be performed on the Local Bus. PCI Target Delayed Write mode is programmable to delay the ADS# and ALE assertion for the amount of Local clocks selected in CNTRL[11:10]. This feature is useful for gaining higher throughput during PCI Target Write Burst transactions for conditions in which the PCI clock frequency is slower than the Local clock frequency.

4.2.1.6   PCI Target Local Bus READY# Timeout Mode

The PCI 9030 supports PCI Target Local Bus READY# Timeout mode transactions, where the PCI 9030 asserts an internal READY# signal to recover from stalling the Local and PCI Buses. The PCI Target Local Bus READY# Timeout mode transaction is programmable to select the amount of Local clocks before READY# times out (CNTRL[9:8]). If a Local Target stalls with a READY# assertion

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during PCI Target Write transactions, the PCI 9030 empties the Write FIFO by dumping the data into the Local Bus and does not pass an error condition to the PCI Bus Initiator. During PCI Target Read transactions, the PCI 9030 issues a PCI Target Abort to the PCI Bus Initiator every time the PCI Target Local Bus READY# Timeout is detected.

4.2.1.7   PCI Target Transfer

A PCI Bus Master addressing the Memory space decoded for the Local Bus initiates transactions. Upon a PCI Read/Write, the PCI 9030 being a Local Bus Master executes a transfer, at which time it reads data into the PCI Target Read FIFO or writes data to the Local Bus.

For a PCI Direct access to the Local Bus, the PCI 9030 has a 32-Lword (128-byte) Write FIFO and an 16-Lword (64-byte) Read FIFO. The FIFOs enable the Local Bus to operate independently of the PCI Bus.

For Write transfers, if the Write FIFO becomes full, the PCI 9030 is programmable to disconnect, or retain the PCI Bus while generating wait states (TRDY# de-asserted) (CNTRL[18]).

For PCI Read transactions from the Local Bus, the PCI 9030 holds off TRDY# while gathering data from the Local Bus. For Read accesses mapped to PCI Memory space, the PCI 9030 prefetches up to 16 Lwords (in Continuous Prefetch mode) from the Local Bus. Unused Read data is flushed from the FIFO. For Read accesses mapped to PCI I/O space, the PCI 9030 does not prefetch Read data. Rather, it breaks each read of a Burst cycle into a single Address/Data cycle on the Local Bus.

The PCI Target Retry Delay Clocks bits (CNTRL[22:19]) can be used to program the period of time in which the PCI 9030 holds off TRDY#. The PCI 9030 issues a Retry to the PCI Bus Transaction Master when the programmed time period expires. This occurs when the PCI 9030 cannot gain Local Bus control and return TRDY# within the programmed time period or the Local Bus is slowly emptying the Write FIFO, and filling the Read FIFO.

The PCI 9030 supports on-the-fly Endian conversion for Spaces 0, 1, 2, and 3, and Expansion ROM. The Local Bus can be Big/Little Endian by using the programmable internal register configuration.

Note: *The PCI Bus is always Little Endian.*
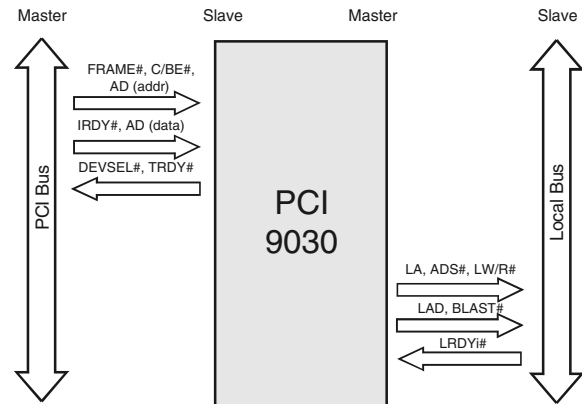
Figure 4-3. PCI Target Write
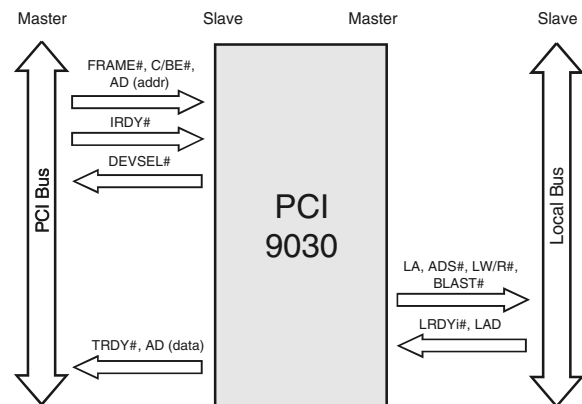
Figure 4-4. PCI Target Read

Note: *The figures represent a sequence of Bus cycles.*

4.2.1.8   PCI Target PCI-to-Local Address Mapping

Five Local Address spaces—Spaces 0, 1, 2, and 3, and Expansion ROM—are accessible from the PCI Bus. Each is defined by a set of three registers:

- Local Address Range (LAS*x*RR and/or EROMRR, where *x* is the Local Address Space number)
- Local Base Address (LAS*x*BA and/or EROMBA)
- PCI Base Address (PCIBAR2, PCIBAR3, PCIBAR4, PCIBAR5, and/or PCIERBAR)

A fourth register, the Bus Region Descriptor registers (LAS*x*BRD and/or EROMBRD), defines the Local Bus characteristics for the PCI Target regions. (Refer to Figure 4-5.)

Each PCI-to-Local Address space is defined as part of reset initialization. (Refer to Section 4.2.1.8.1.) These Local Bus characteristics can be modified at any time before actual data transactions.

4.2.1.8.1   PCI Target Local Bus Initialization

Range—Specifies the PCI Address bits to use for decoding a PCI access to Local Bus space. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits required to be included in decode, and 0 to all others.

Remap PCI-to-Local Addresses into a Local Address Space—Bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor—Specifies the Local Bus characteristics.

4.2.1.8.2   PCI Target Initialization

After a PCI reset and serial EEPROM load, the software determines the amount of required address space by writing all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9030 returns zeros (0) in the Don't Care Address bits, effectively specifying the address space required, at which time the PCI software maps the Local Address space into the PCI Address space by programming the PCI Base Address register. (Refer to Figure 4-5.)
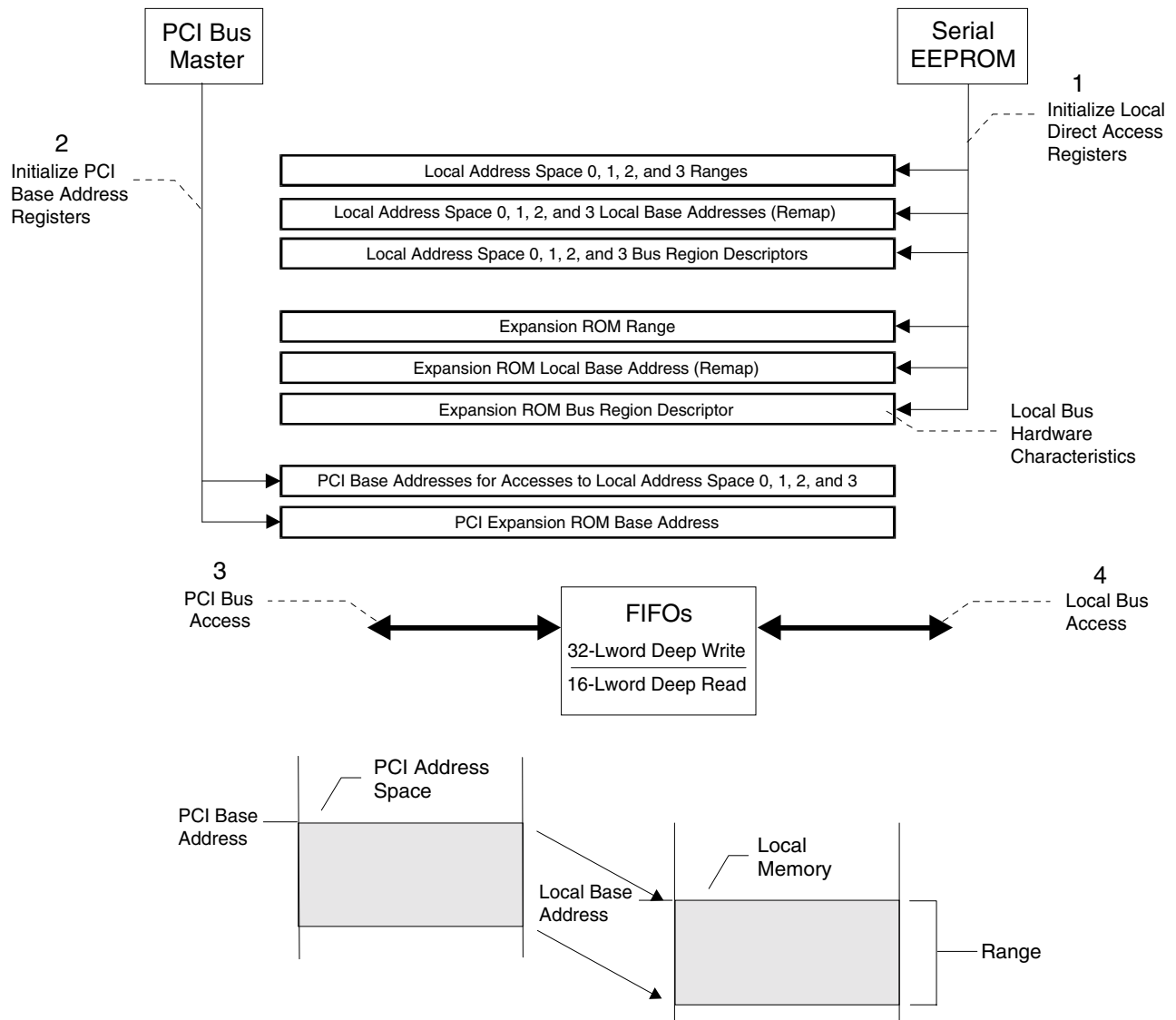
4—PCI Target

Figure 4-5. Local Bus PCI Target Access

4.2.1.8.3 PCI Target Example

A 1 MB prefetchable Local Address Space encompassing Local Bus Addresses 01200000h through 012FFFFFh is to be configured for Local Address Space 0. Assume the BIOS System Resource Manager allocates 1 MB with a PCI Base Address of 34500000h. The Local memory is then accessible at PCI Addresses 34500000h through 345FFFFFh.

a. Program the serial EEPROM as follows:
   - **Range**—FFF00008h [1 MB, decode the upper 12 PCI Address bits, and set the Prefetchable bit (LAS0RR[3]=1)].
   - **Local Base Address (Remap)**—01200001h (Local Base Address for PCI-to-Local accesses). Bit 0 must be set to enable address decoding (LAS0BA[0]=1).

b. PCI Initialization software writes all ones (1) to the PCI Base Address register, then reads it back.
   - The PCI 9030 returns a value of FFF00008h, after which the PCI software writes the base address it assigned into the PCI Base Address register(s).
   - **PCI Base Address**—34500008h (PCI Base Address for Access to Local Address Space 0 register, PCIBAR2). The PCI Base Address is always aligned on a boundary determined by address space size. The Prefetchable bit is set (PCIBAR2[3]=1).

4.2.1.8.4 PCI Target Byte Enables (Multiplexed Mode)

During a PCI Target transfer, each of five spaces—Spaces 0, 1, 2, and 3, and Expansion ROM—can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#). LBE[3:0]# (PQFP—pins 55, 58-60, respectively; µBGA—pins M5, P5, M6, N6, respectively) are encoded, based on the configured bus width, as follows.

32-Bit Bus—The four byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LAD[31:24]
- LBE2# Byte Enable 2—LAD[23:16]
- LBE1# Byte Enable 1—LAD[15:8]
- LBE0# Byte Enable 0—LAD[7:0]

16-Bit Bus—LBE[3, 1:0]# are encoded to provide BHE#, LAD1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LAD[15:8]
- LBE2# *not used*
- LBE1# Address bit 1 (LAD1)
- LBE0# Byte Low Enable (BLE#)—LAD[7:0]

8-Bit Bus—LBE[1:0]# are encoded to provide LAD[1:0], respectively:

- LBE3# *not used*
- LBE2# *not used*
- LBE1# Address bit 1 (LAD1)
- LBE0# Address bit 0 (LAD0)

During the Address phase, LAD[1:0] are valid address bits with the same value as LBE[1:0]#.

4.2.1.8.5 PCI Target Byte Enables (Non-Multiplexed Mode)

During a PCI Target transfer, each of five spaces—Spaces 0, 1, 2, and 3, and Expansion ROM—can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#). LBE[3:0]# (PQFP—pins 55, 58-60, respectively; µBGA—pins M5, P5, M6, N6, respectively) are encoded, based on the configured bus width, as follows.

32-Bit Bus—The four byte enables indicate which of the four bytes are active during a Data cycle:

- LBE3# Byte Enable 3—LD[31:24]
- LBE2# Byte Enable 2—LD[23:16]
- LBE1# Byte Enable 1—LD[15:8]
- LBE0# Byte Enable 0—LD[7:0]

16-Bit Bus—LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively:

- LBE3# Byte High Enable (BHE#)—LD[15:8]
- LBE2# *not used*
- LBE1# Address bit 1 (LA1)
- LBE0# Byte Low Enable (BLE#)—LD[7:0]

8-Bit Bus—LBE[1:0]# are encoded to provide LA[1:0], respectively:

- LBE3# *not used*
- LBE2# *not used*
- LBE1# Address bit 1 (LA1)
- LBE0# Address bit 0 (LA0)

4—PCI Target

4.3   RESPONSE TO FIFO FULL OR EMPTY

Table 4-1 lists the PCI 9030 response to full or empty
FIFOs.

Table 4-1. Response to FIFO Full or Empty

Mode	Direction	FIFO	PCI Bus	Local Bus
PCI Target Write	PCI-to-Local	Full	Disconnect or Throttle TRDY#[1]	If CNTRL[31]=0 (default preempt condition), de-assert LGNT if the Local Bus is busy. In either case, wait for LREQ to be de-asserted by the local bus master.
		Empty	Normal	Normal, assert BLAST#.
PCI Target Read	Local-to-PCI	Full	Normal	Normal, assert BLAST#.
		Empty	Disconnect or Throttle TRDY#[1]	Normal.

1. Throttle TRDY# depends on the PCI Target Retry Delay Clocks (CNTRL[22:19]).

4.4 PCI TARGET (DIRECT SLAVE) OPERATION TIMING DIAGRAMS
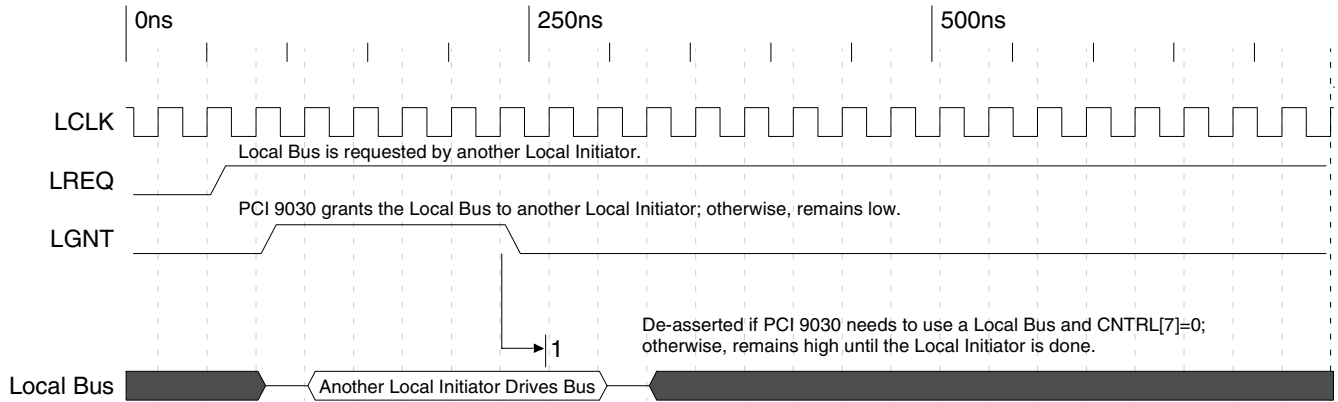
Timing Diagram 4-1. Local Bus Arbitration from the PCI 9030 by Another Local Bus Initiator (LREQ and LGNT)
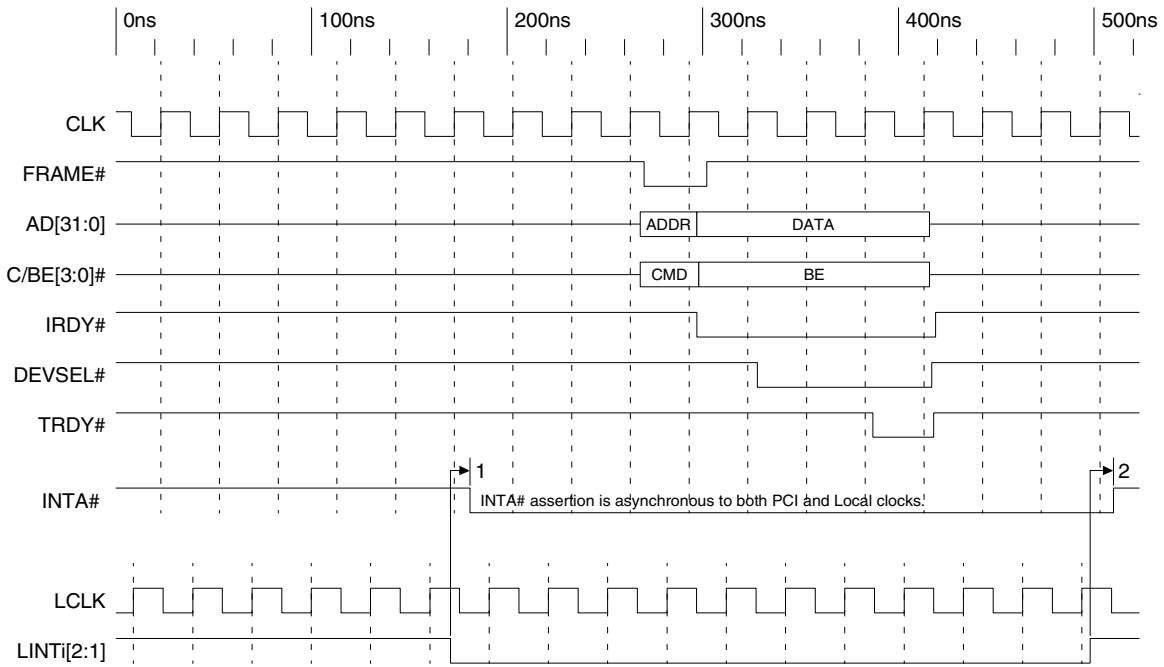
Timing Diagram 4-2. Local Level-Triggered Interrupt Asserting PCI Interrupt
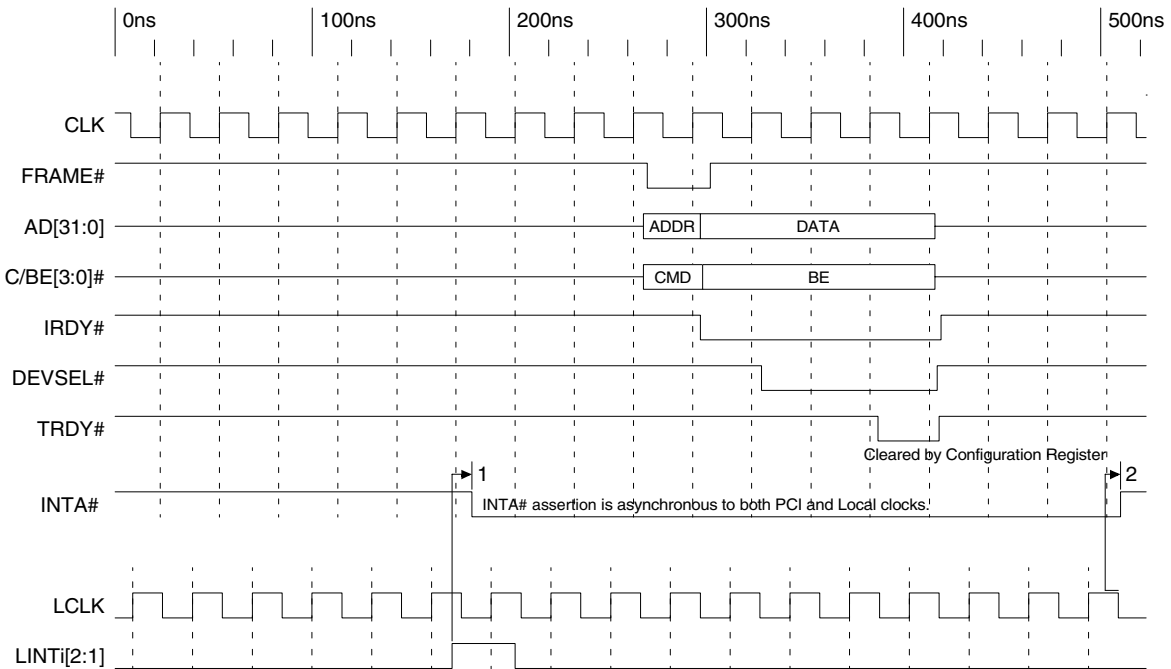
Timing Diagram 4-3. Local Edge-Triggered Interrupt Asserting PCI Interrupt
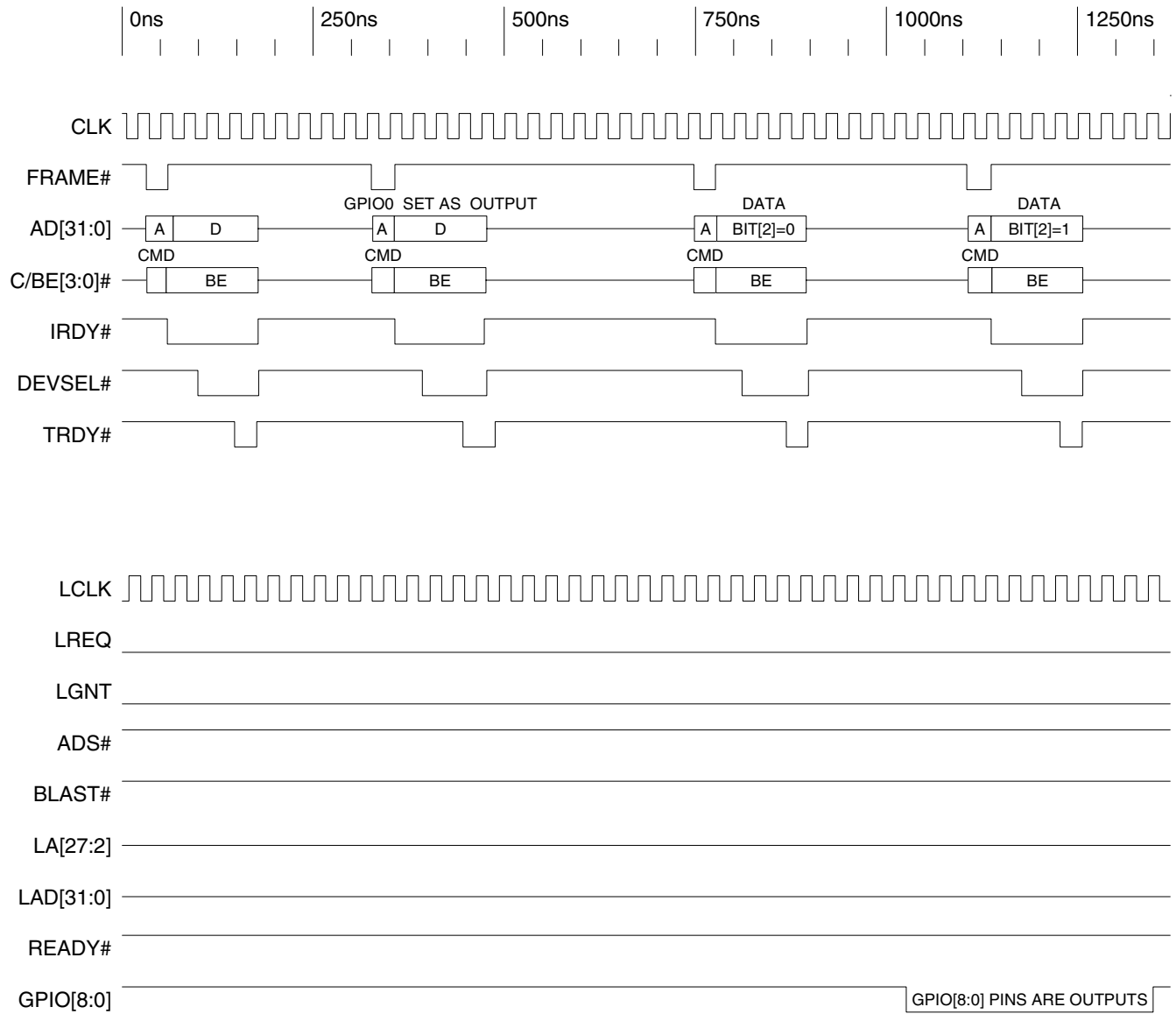
Note: GPIO pins configured as outputs are driven only when the PCI 9030 owns the Local Bus.
(Refer to *PCI 9030 Errata #2*.)

Timing Diagram 4-4. GPIO[8:0] as Outputs
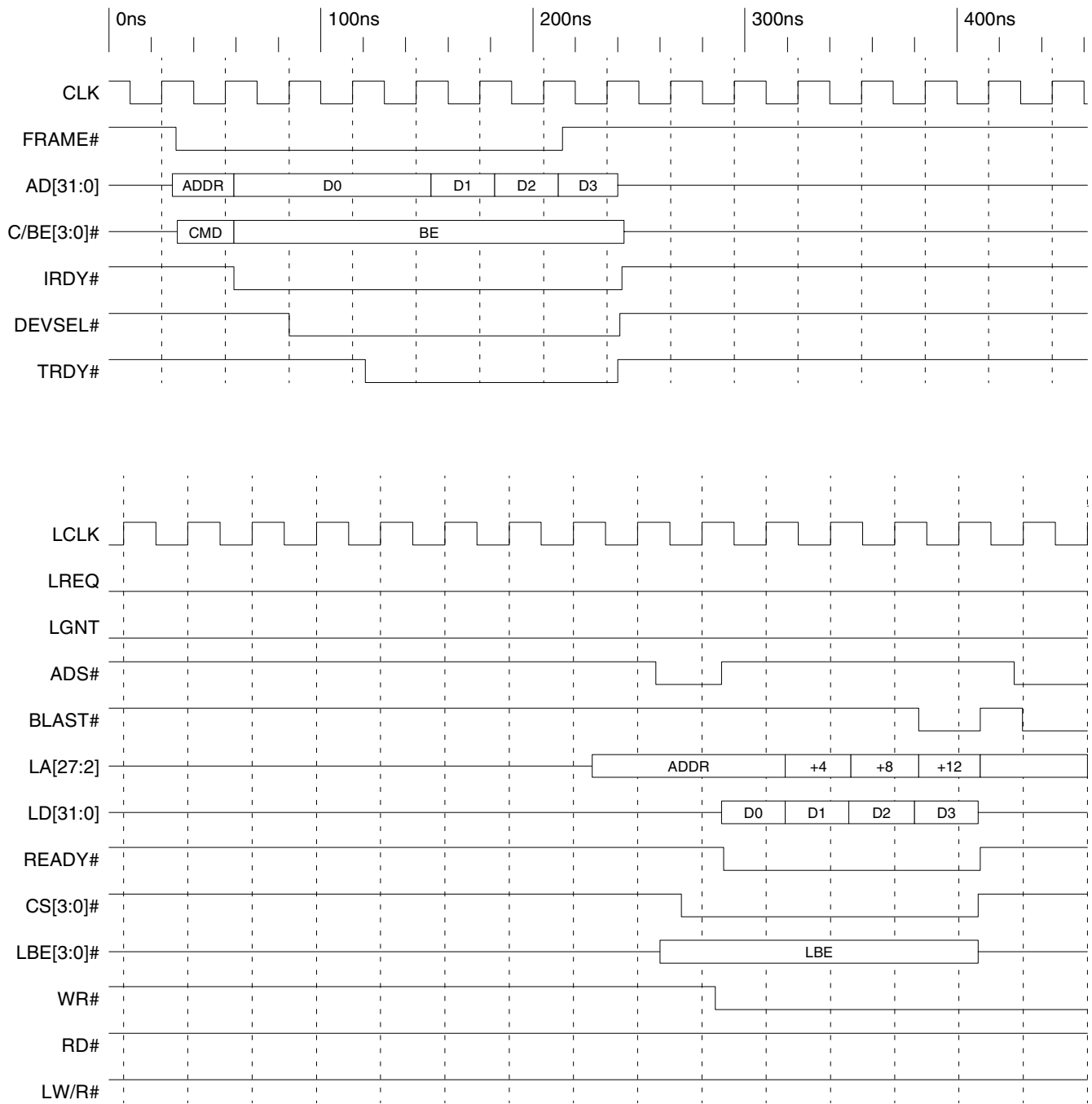
Note: CS[3:0]# Base Address is in the range of Local Address Spaces 3 through 0.

Timing Diagram 4-5. Chip Select [3:0]# (32-Bit Local Bus)

4.4.1 Serial EEPROM and Configuration Initialization Timing Diagrams

Note: Serial EEPROM initialization completes in approximately 4.35 ms with a 33.3 MHz PCI clock.

Timing Diagram 4-6. Initialization from Serial EEPROM (2K or 4K Bit)

4—PCI Target
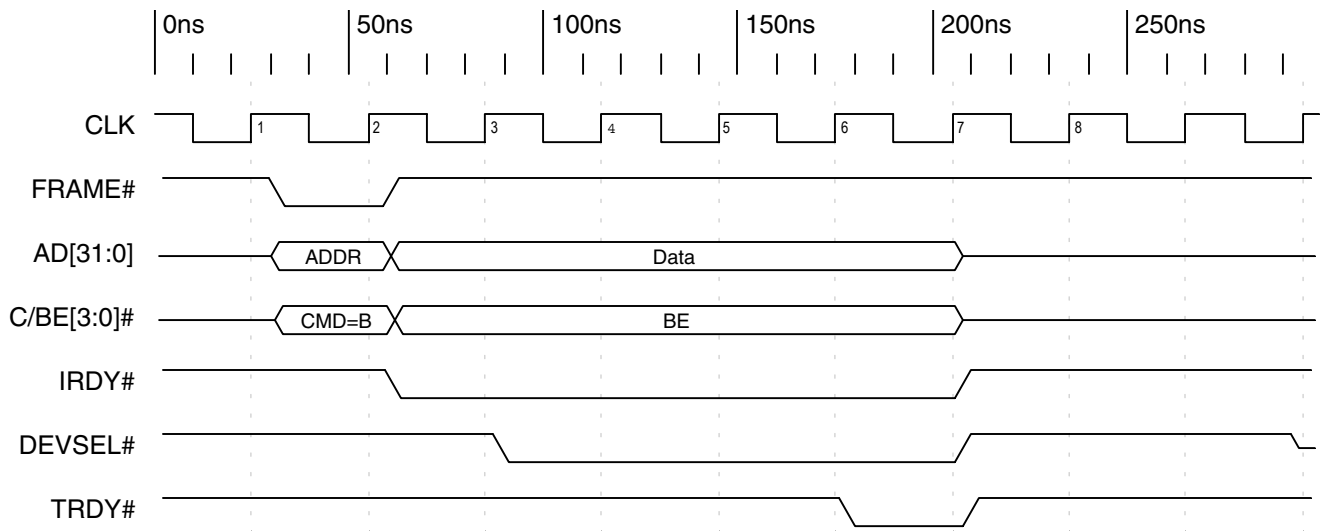
Timing Diagram 4-7. PCI Configuration Write to PCI Configuration Register
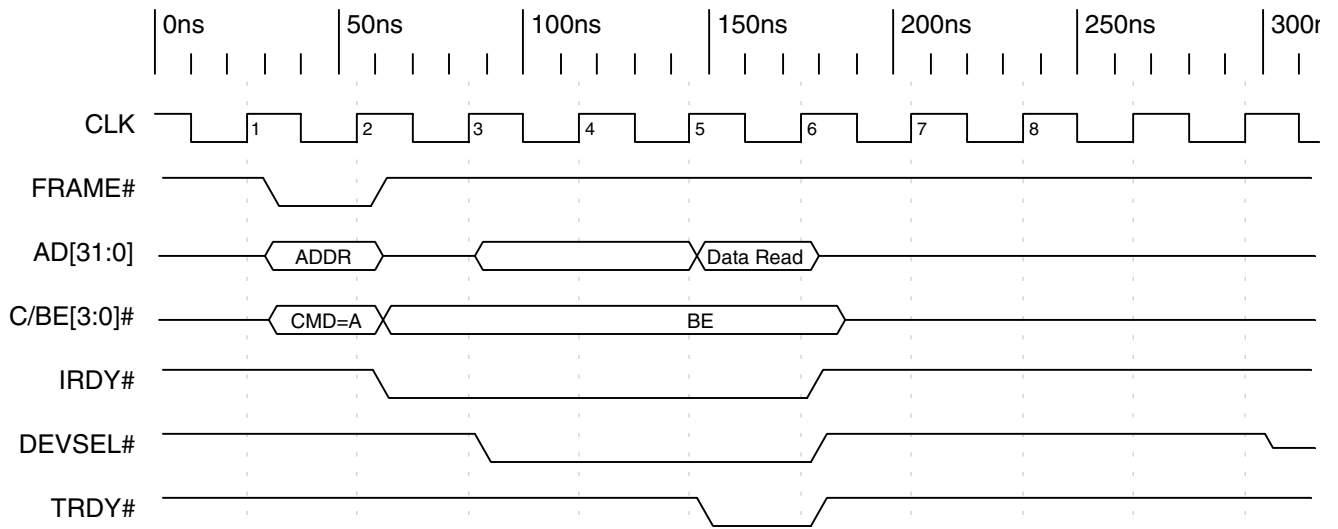
Timing Diagram 4-8. PCI Configuration Read from PCI Configuration Register
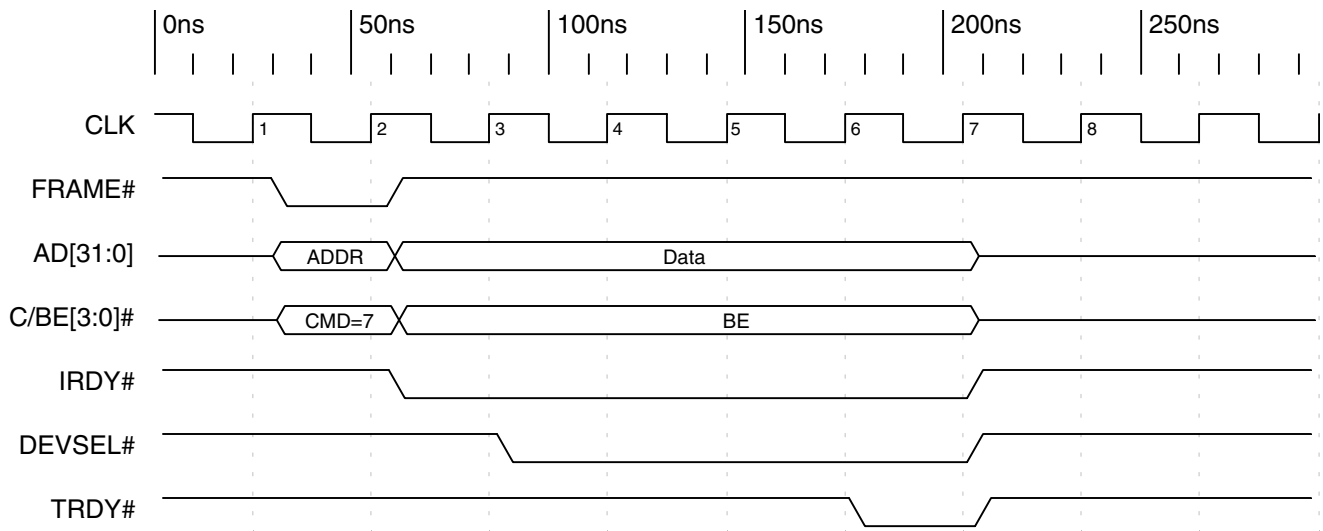
Timing Diagram 4-9. PCI Memory Write to Local Configuration Register
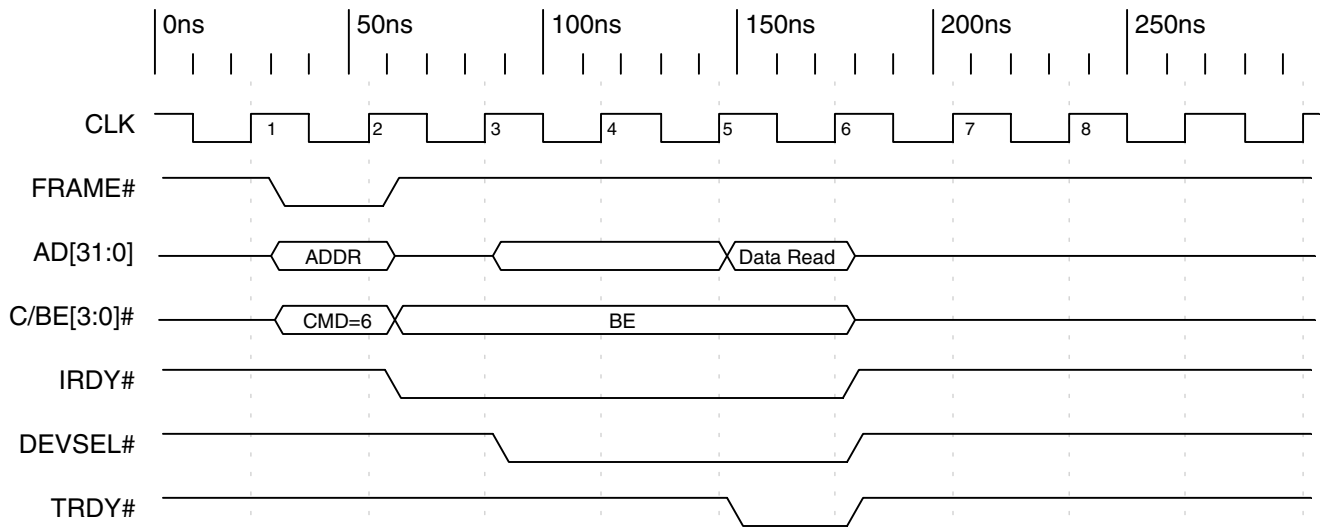
Timing Diagram 4-10. PCI Memory Read from Local Configuration Register

4—PCI Target

4.4.2   Multiplexed and Non-Multiplexed Modes Timing Diagrams
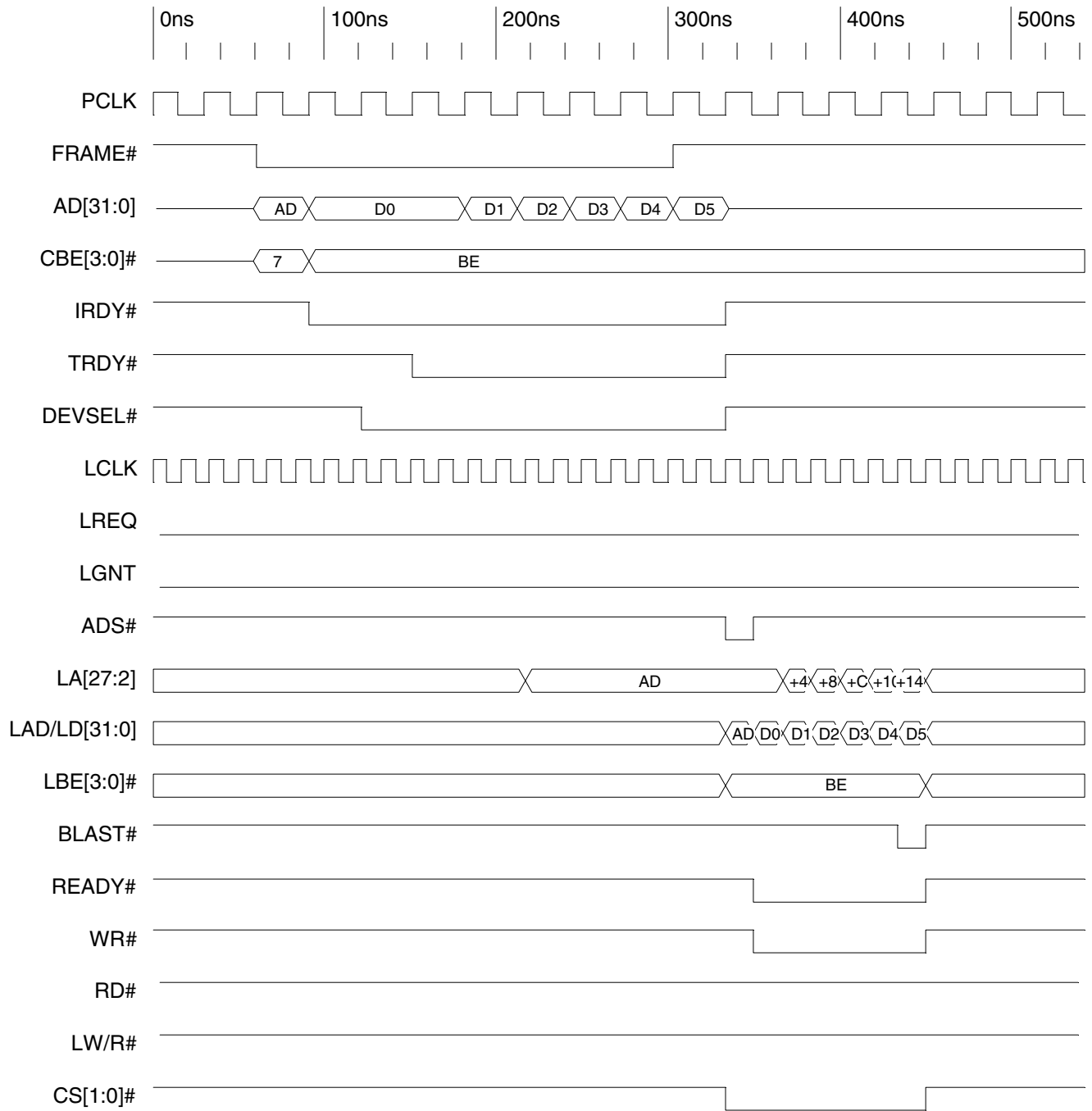
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-11. PCI Target Burst Write with Delayed Write and Chip Select Enabled (32-Bit Local Bus)
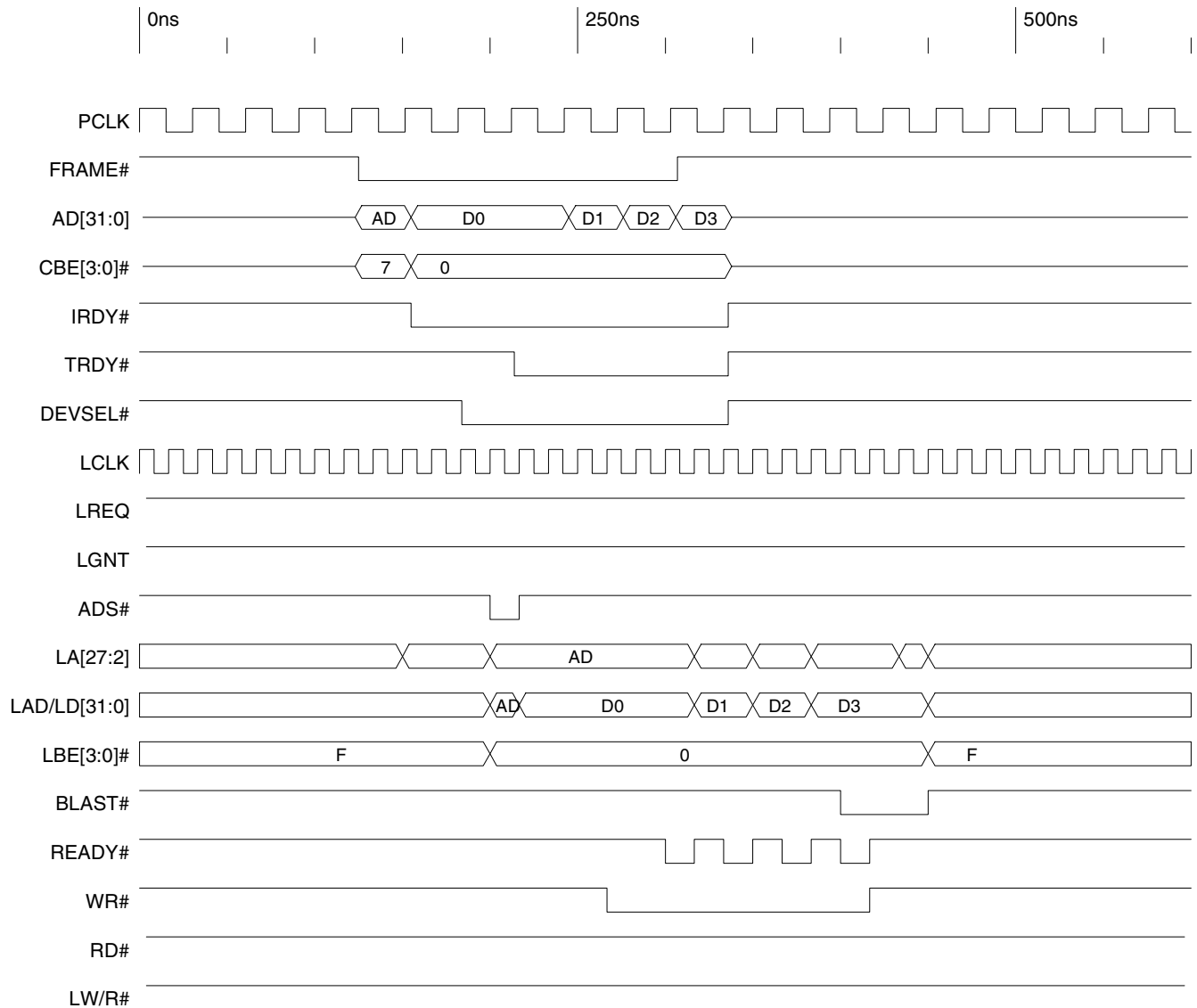
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Five Address-to-Data Wait States; One Data-to-Data Wait State;
Three Write Strobe Delay Clocks; Two Write Cycle Hold Clocks.

Timing Diagram 4-12. PCI Target Burst Write (32-Bit Local Bus)
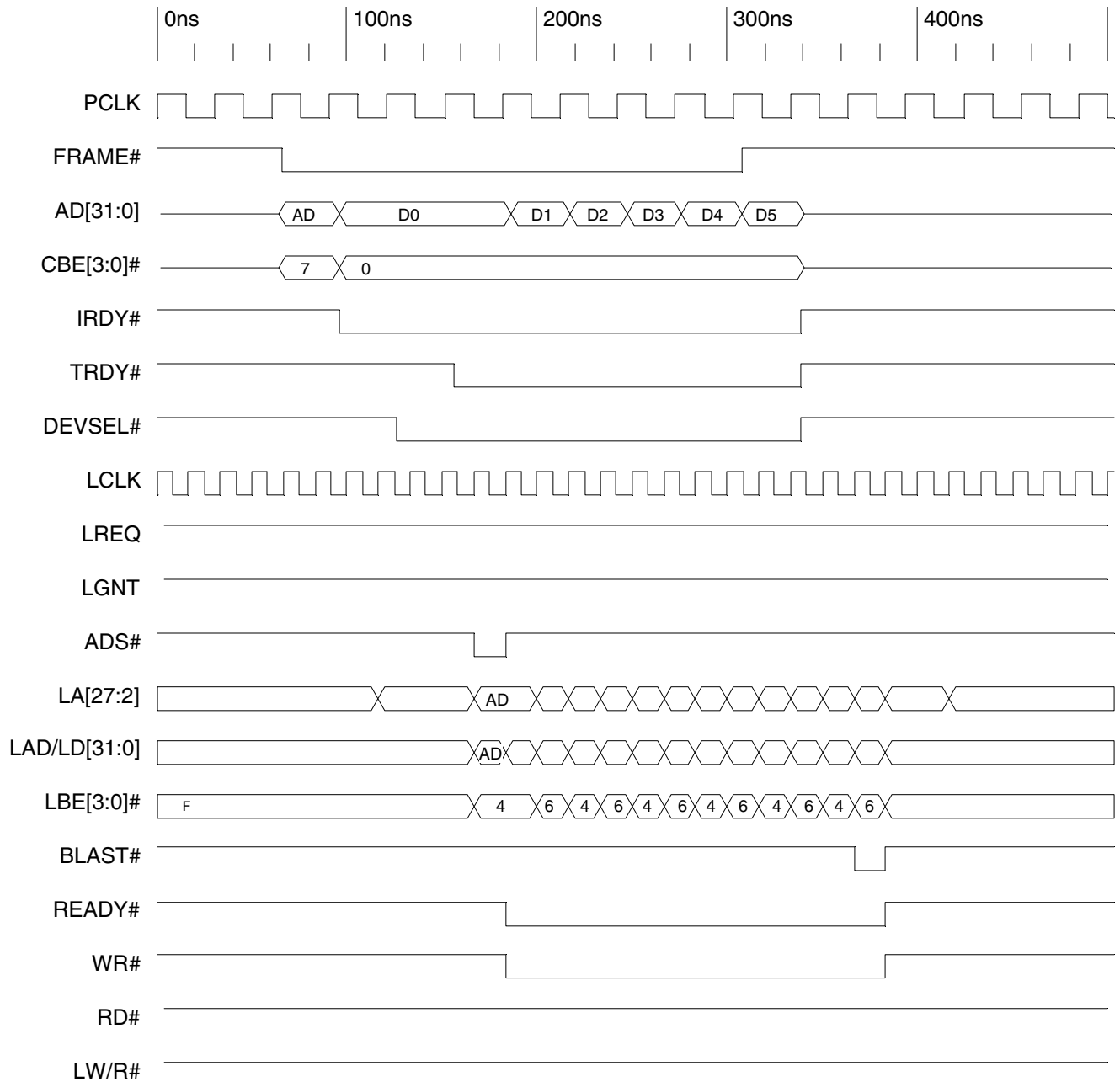
4—PCI Target

| 0ns | 100ns | 200ns | 300ns | 400ns |

PCLK

FRAME#

AD[31:0]   AD   D0   D1   D2   D3   D4   D5

CBE[3:0]#   7   0

IRDY#

TRDY#

DEVSEL#

LCLK

LREQ

LGNT

ADS#

LA[27:2]   AD

LAD/LD[31:0]   AD

LBE[3:0]#   F   4   6   4   6   4   6   4   6   4   6   4   6

BLAST#

READY#

WR#

RD#

LW/R#

Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-13. PCI Target Burst Write (16-Bit Local Bus), No Wait States
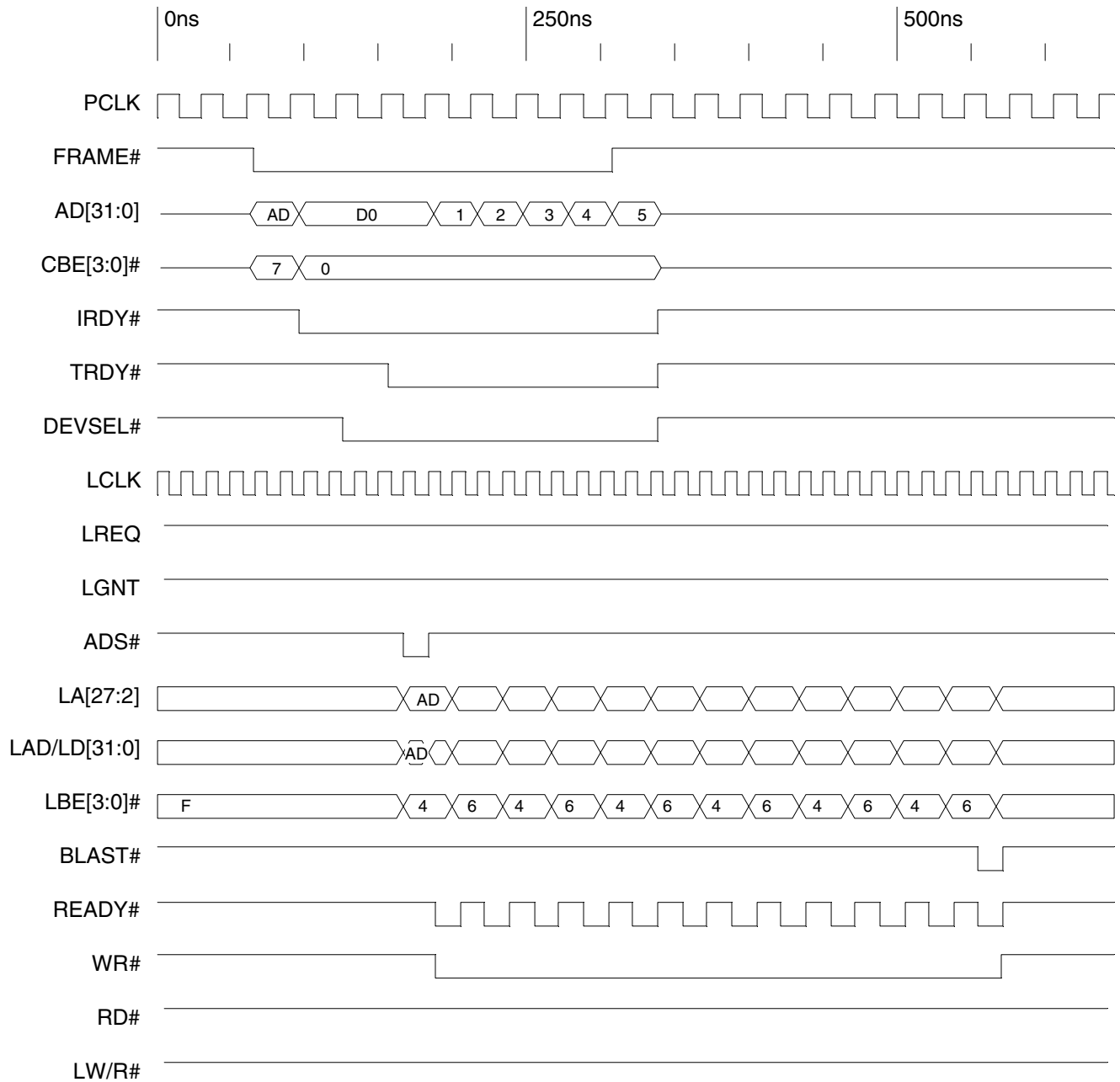
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-14. PCI Target Burst Write (16-Bit Local Bus), One Data-to-Data Wait State
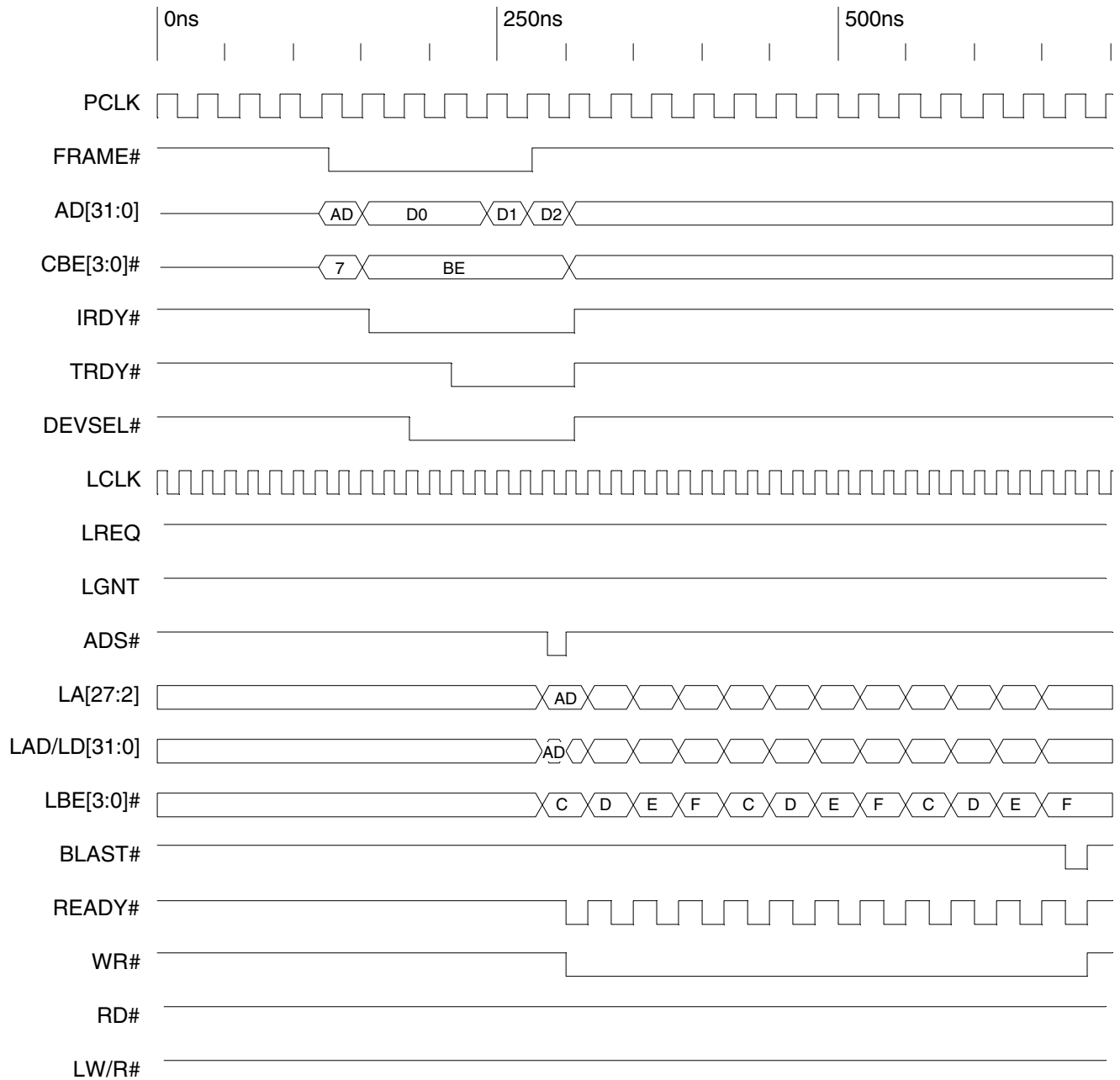
	0ns	250ns	500ns

PCLK

FRAME#

AD[31:0]   AD D0 D1 D2

CBE[3:0]#   7   BE

IRDY#

TRDY#

DEVSEL#

LCLK

LREQ

LGNT

ADS#

LA[27:2]   AD

LAD/LD[31:0]   AD

LBE[3:0]#   C D E F C D E F C D E F

BLAST#

READY#

WR#

RD#

LW/R#

Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-15. PCI Target Burst Writes (8-Bit Local Bus), One Data-to-Data Wait State
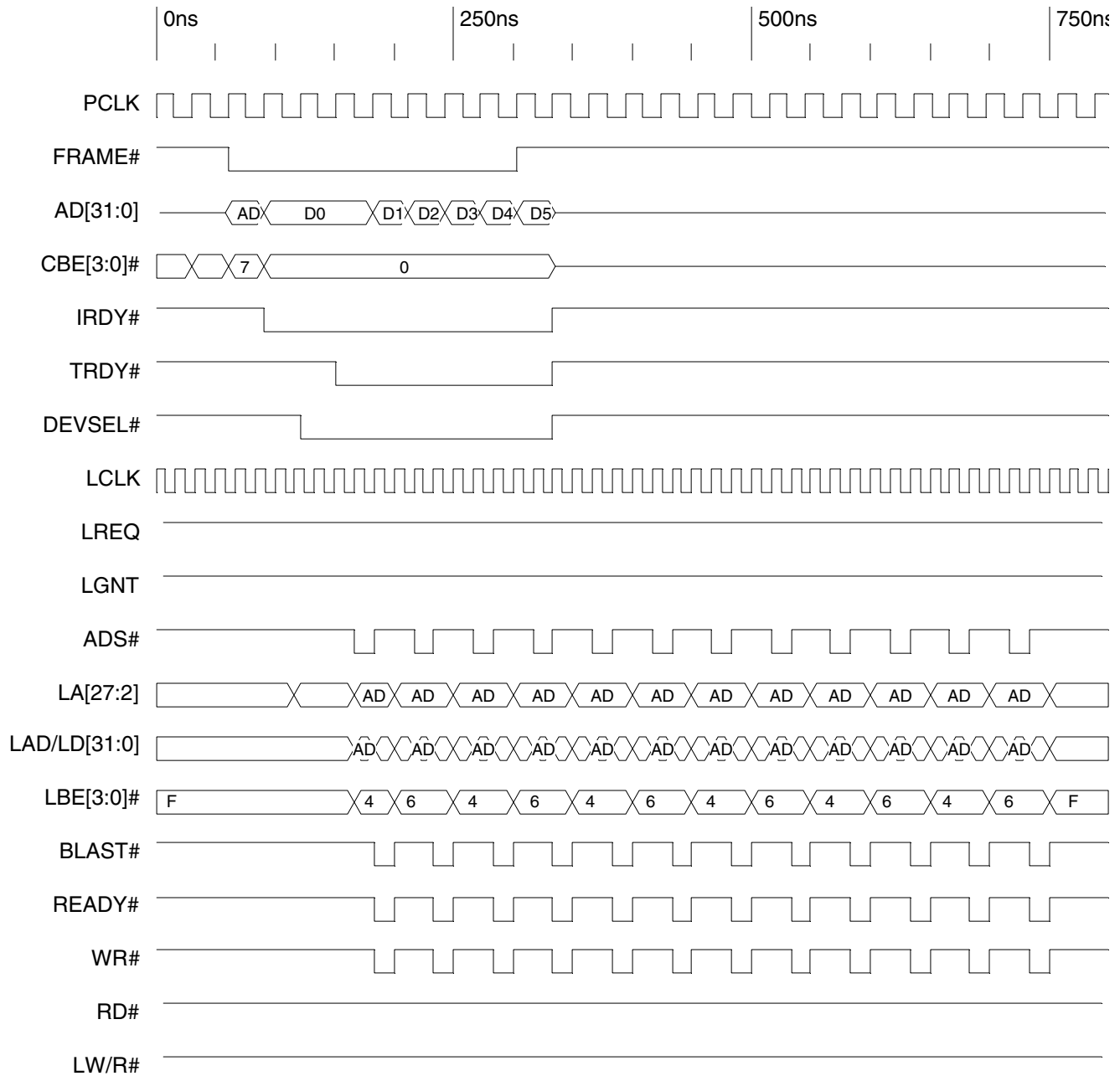
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-16. PCI Target Single Writes (16-Bit Local Bus)
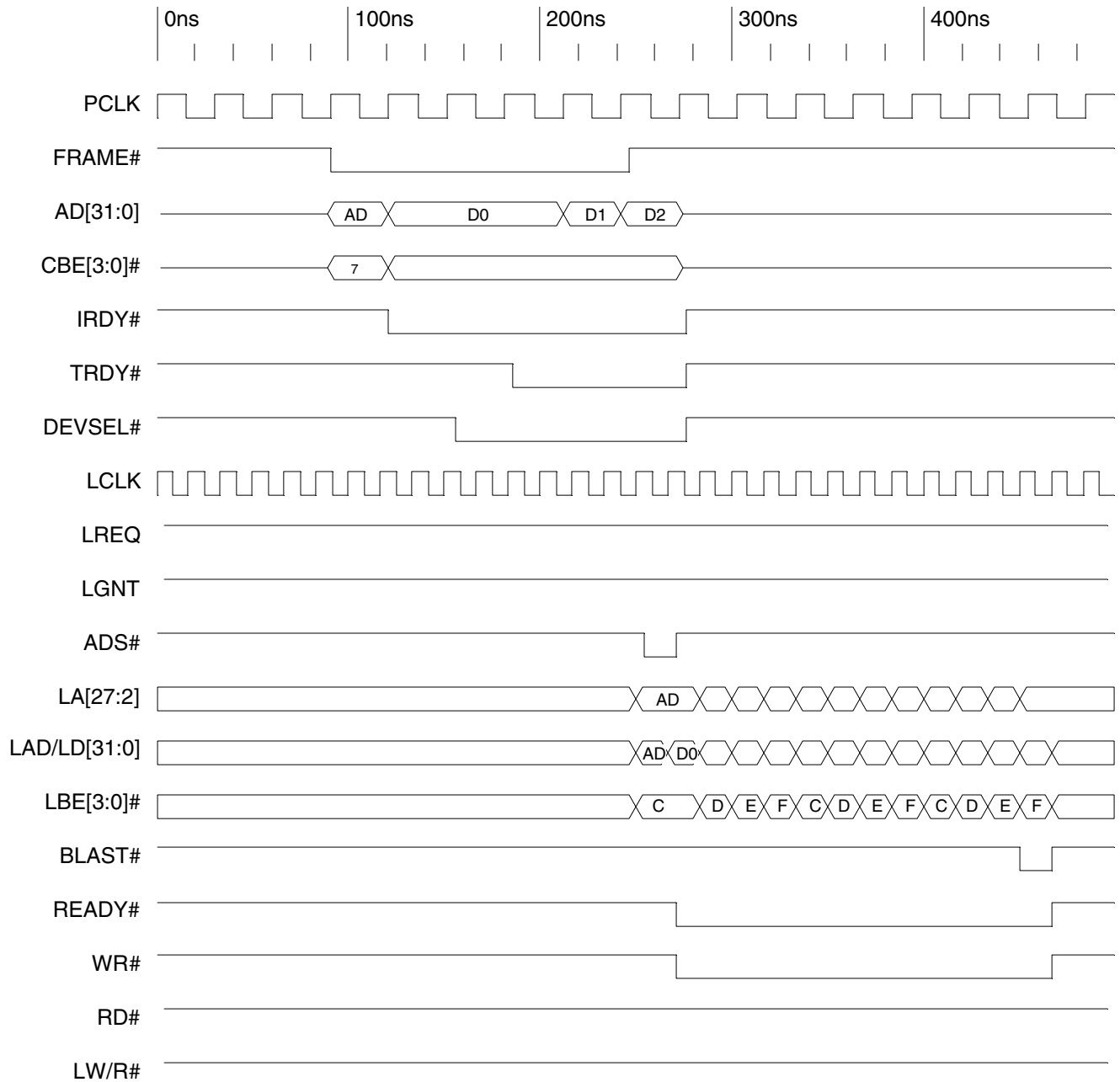
4—PCI Target

Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-17. PCI Target Burst Write (8-Bit Local Bus), No Wait States
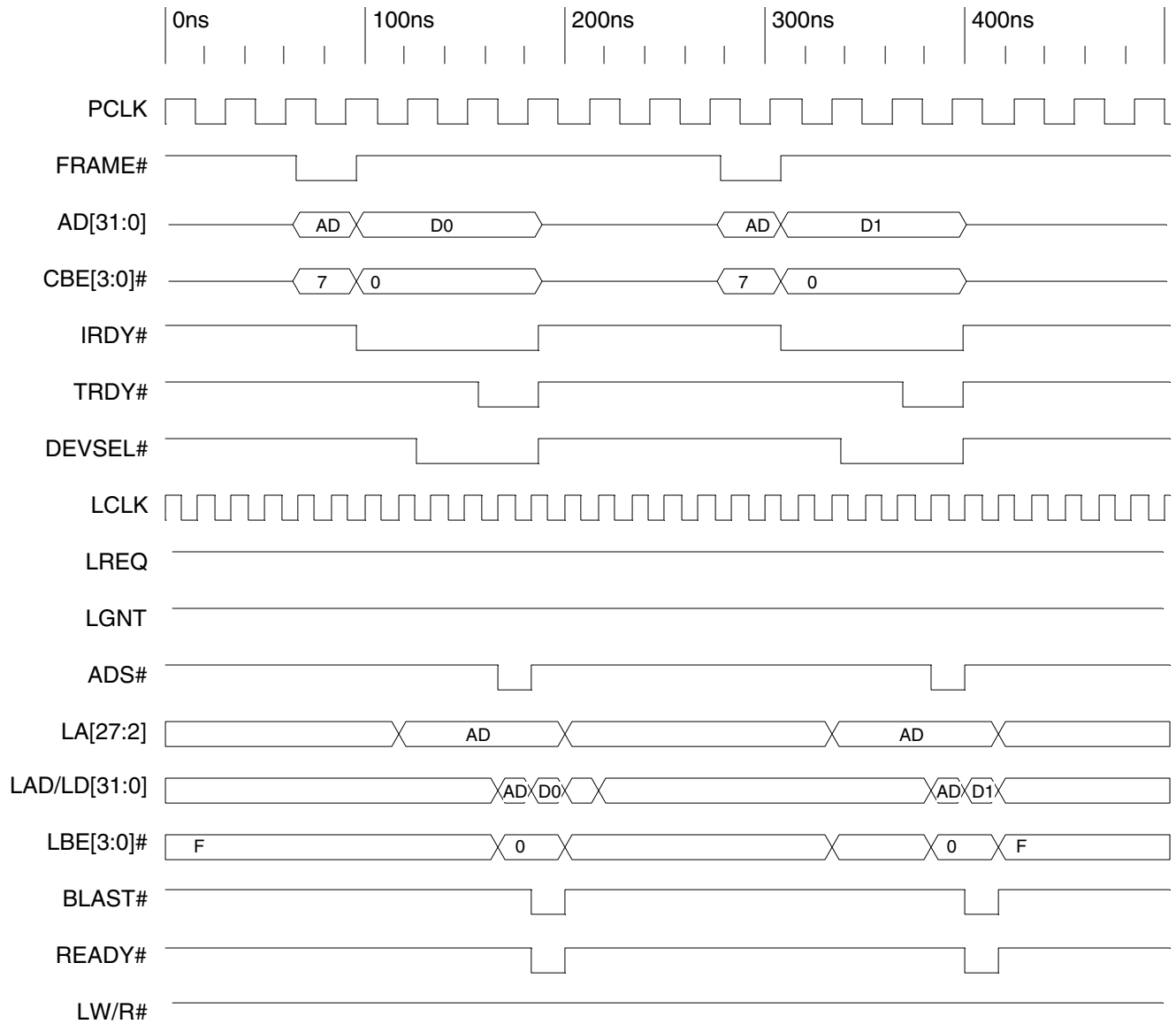
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-18. PCI Target Back-to-Back Single Writes (32-Bit Local Bus)
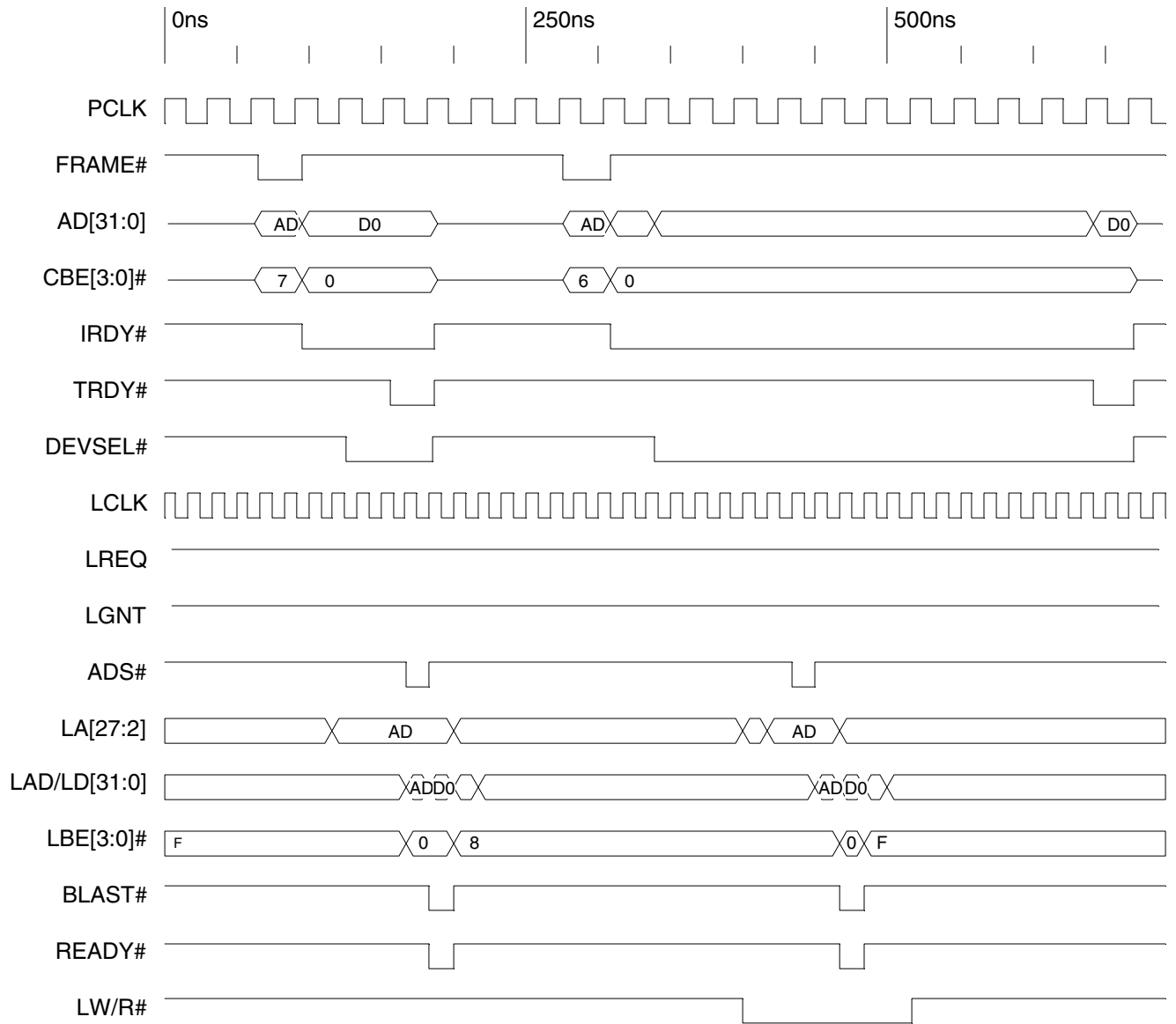
	0ns			250ns			500ns	

PCLK

FRAME#

AD[31:0] AD D0 AD D0

CBE[3:0]# 7 0 6 0

IRDY#

TRDY#

DEVSEL#

LCLK

LREQ

LGNT

ADS#

LA[27:2] AD AD

LAD/LD[31:0] ADD0 ADD0

LBE[3:0]# F 0 8 0 F

BLAST#

READY#

LW/R#

Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-19. PCI Target Back-to-Back Burst Write Followed by Read (16-Bit Local Bus)
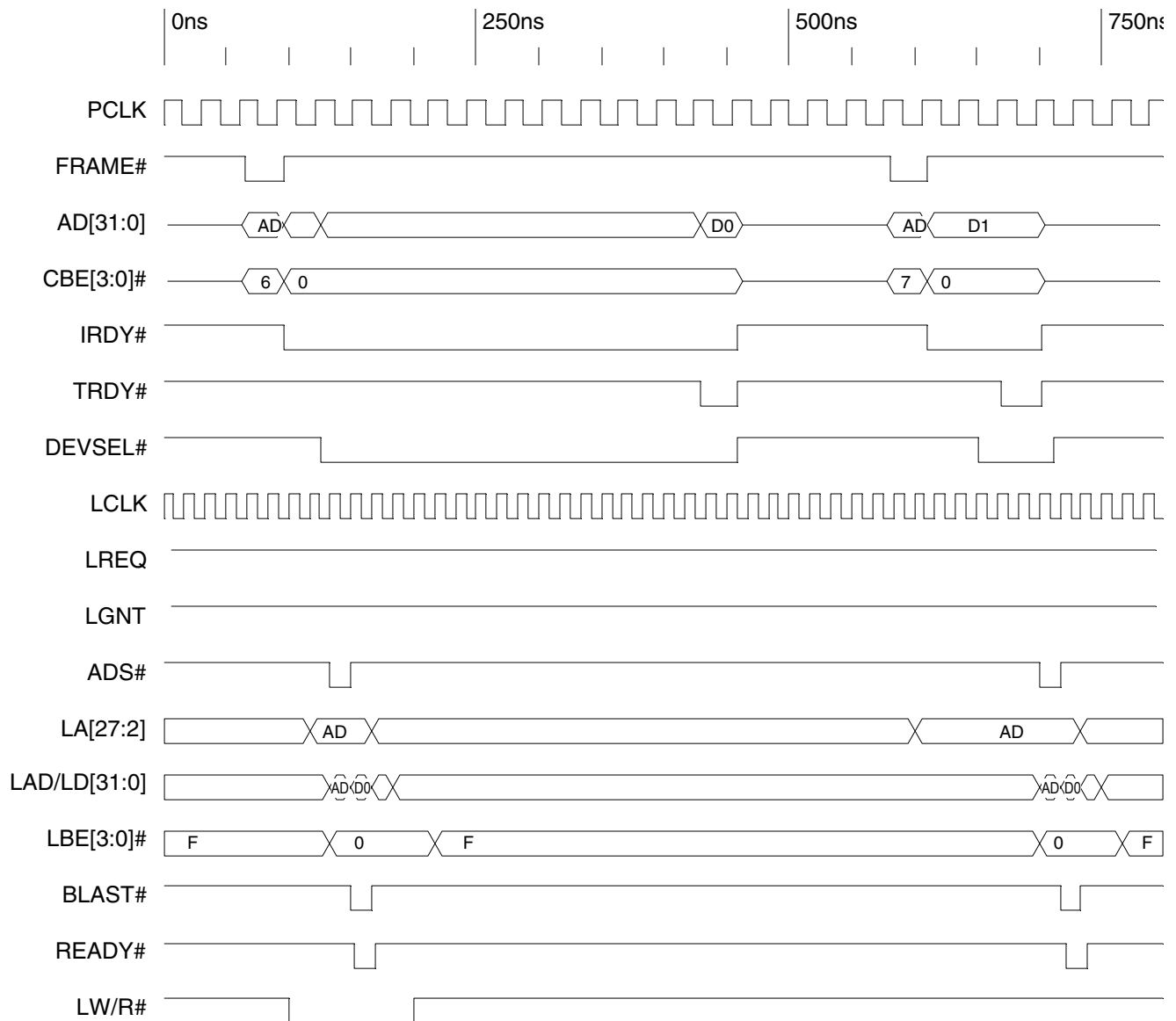
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-20. PCI Target Back-to-Back Burst Read Followed by Write (16-Bit Local Bus)

4—PCI Target

Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.

Timing Diagram 4-21. PCI Target Back-to-Back Burst Reads (16-Bit Local Bus)

4.4.2.1   Multiplexed Mode Only Timing Diagrams
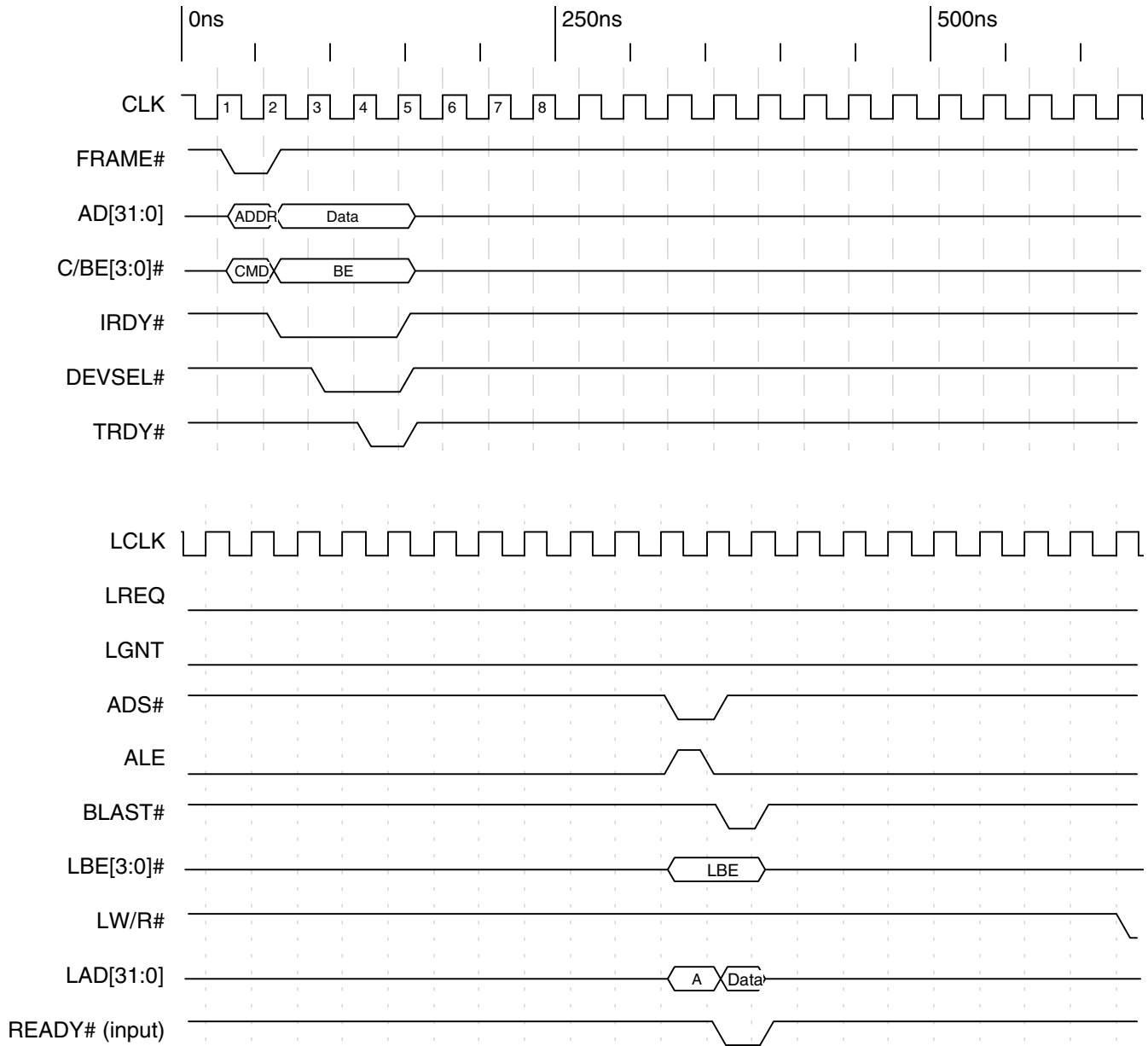
Timing Diagram 4-22. PCI Target Single Write (32-Bit Local Bus), Multiplexed Mode Only
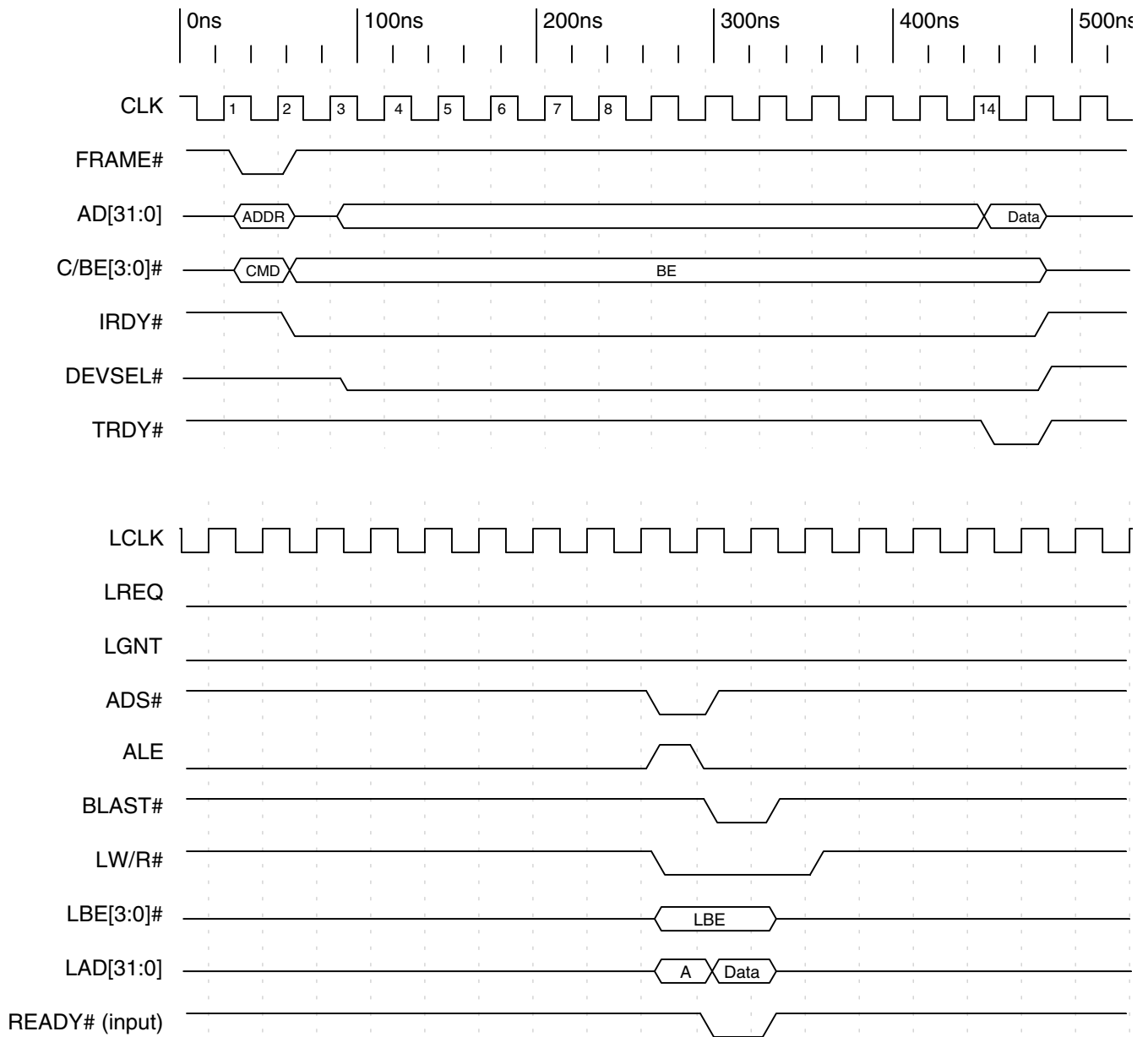
Timing Diagram 4-23. PCI Target Single Read (32-Bit Local Bus), Multiplexed Mode Only

Eight Lword Burst, no wait states, BTERM# (input) enabled, Burst enabled, 32-bit Local Bus.

Note: If BTERM# (input) is disabled, a new ADS# cycle starts every quad-Lword boundary.
BTERM# (input) replaces READY# (input) when asserted.

Timing Diagram 4-24. PCI Target Burst Write with Bterm Enabled (32-Bit Local Bus), Multiplexed Mode Only
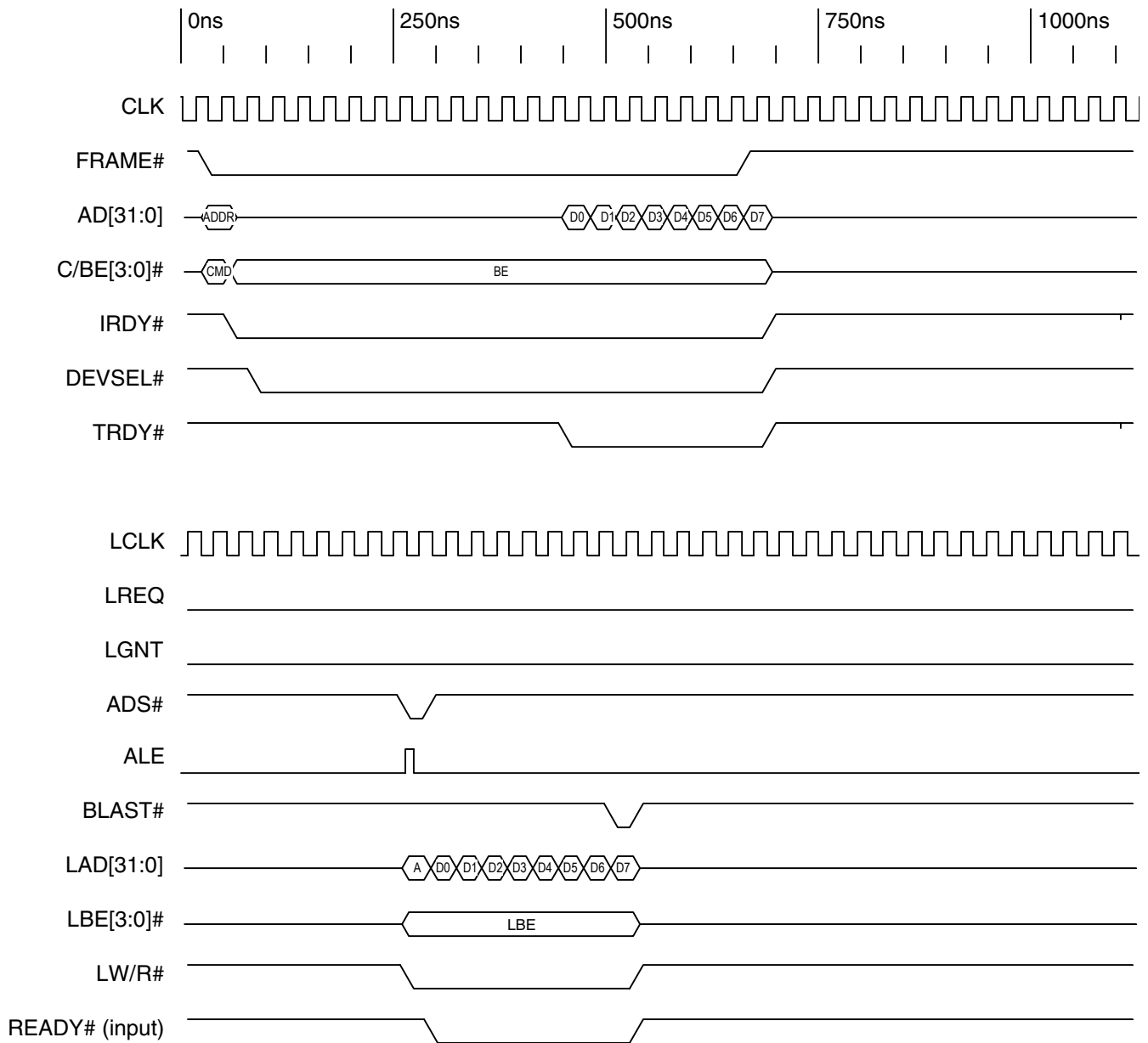
4—PCI Target

**Timing Diagram 4-25. PCI Target Burst Read with Prefetch Enabled (32-Bit Local Bus),
Prefetch Counter Set to 8, Multiplexed Mode Only**
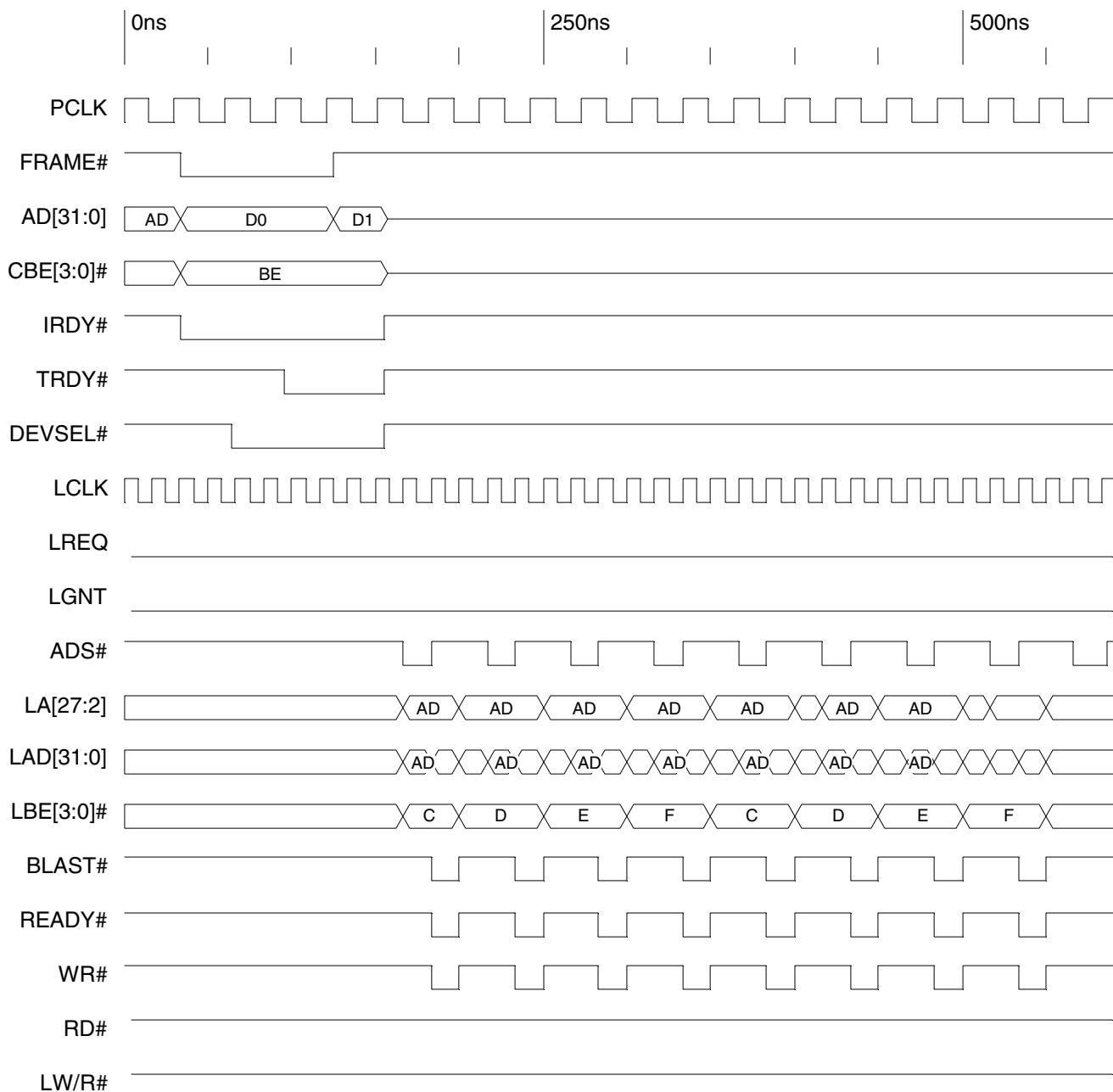
Notes: For Multiplexed mode, use the LAD[31:0] signal for address.
In Multiplexed mode, the PCI 9030 inserts one recovery state
between the last Data and the next Address cycle.

Timing Diagram 4-26. PCI Target Non-Burst Write (8-Bit Local Bus), Multiplexed Mode Only

4—PCI Target

4.4.2.2 Non-Multiplexed Mode Only Timing Diagrams
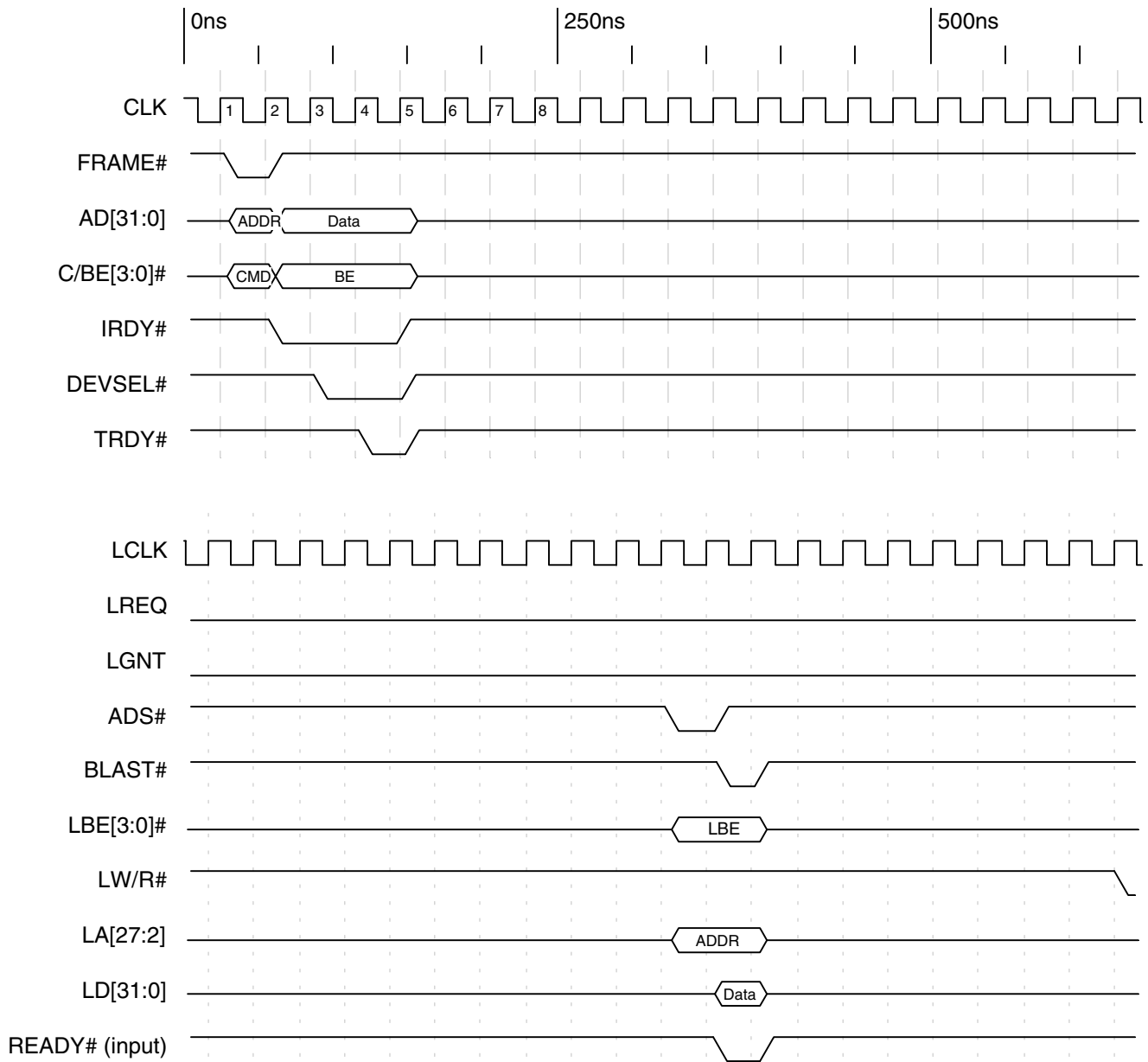
Timing Diagram 4-27. PCI Target Single Write (32-Bit Local Bus), Non-Multiplexed Mode Only
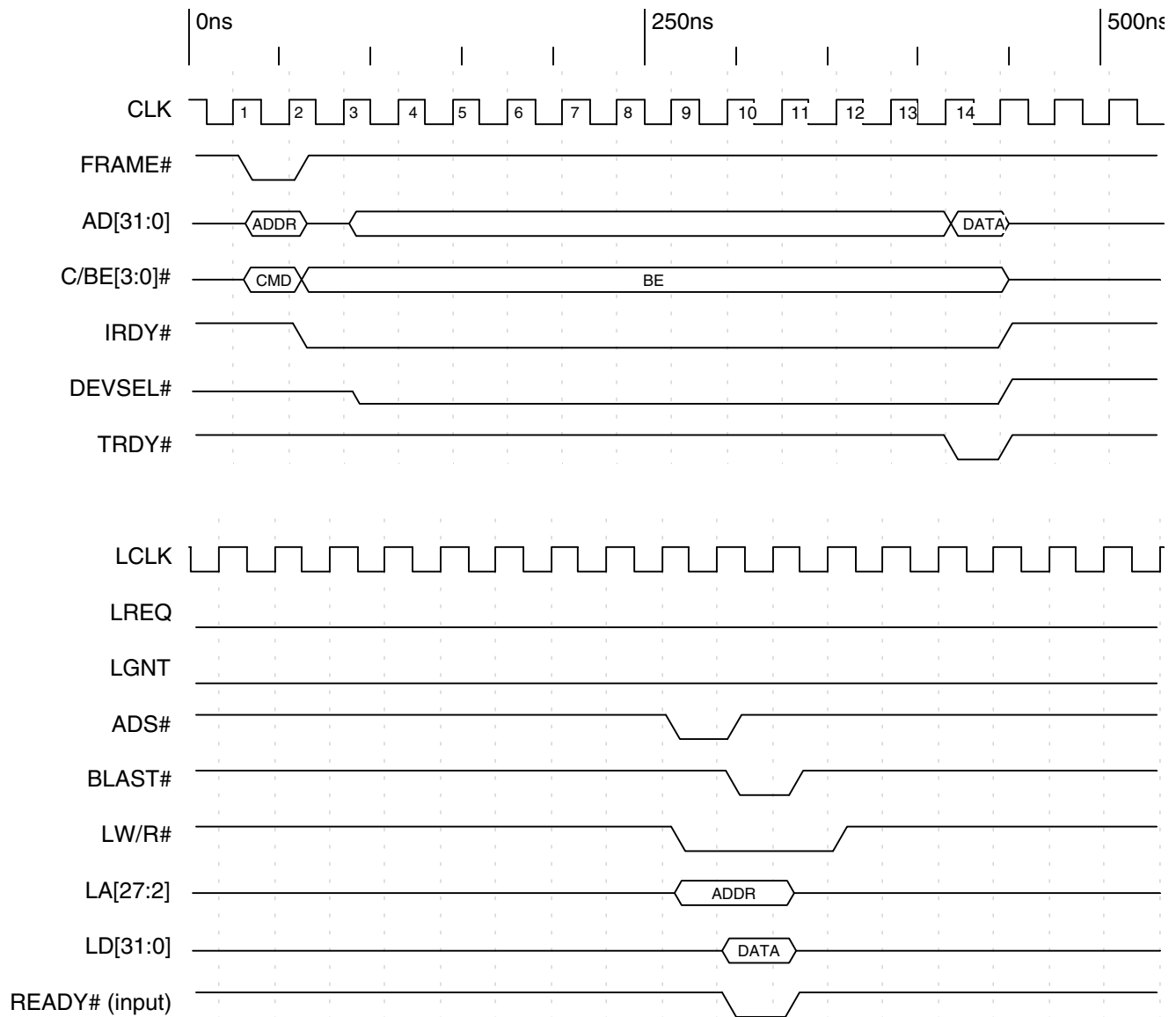
Timing Diagram 4-28. PCI Target Single Read (32-Bit Local Bus), Non-Multiplexed Mode Only
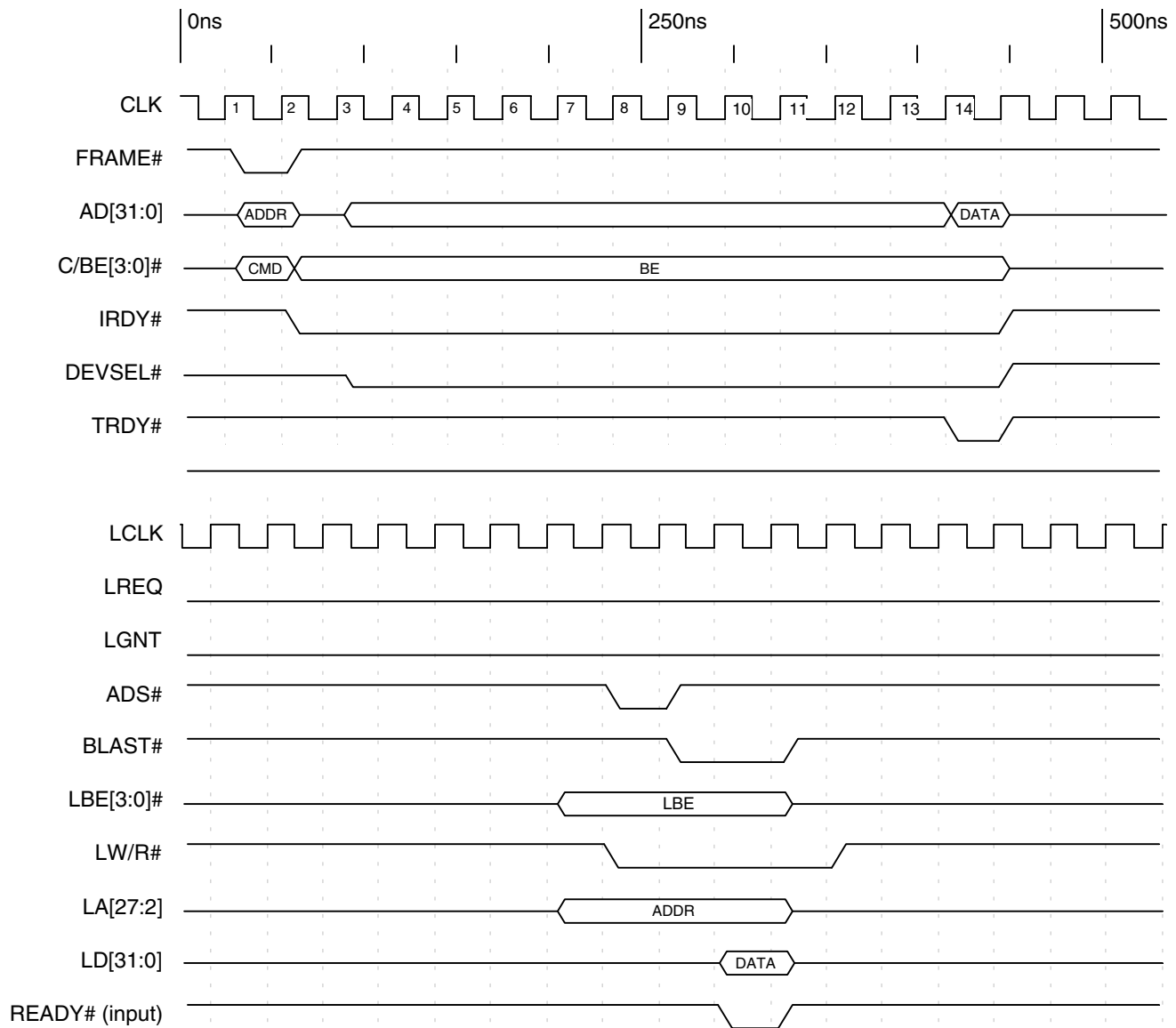
4—PCI Target

Timing Diagram 4-29. PCI Target Single Read with One Wait State Using READY# Input (32-Bit Local Bus), Non-Multiplexed Mode Only
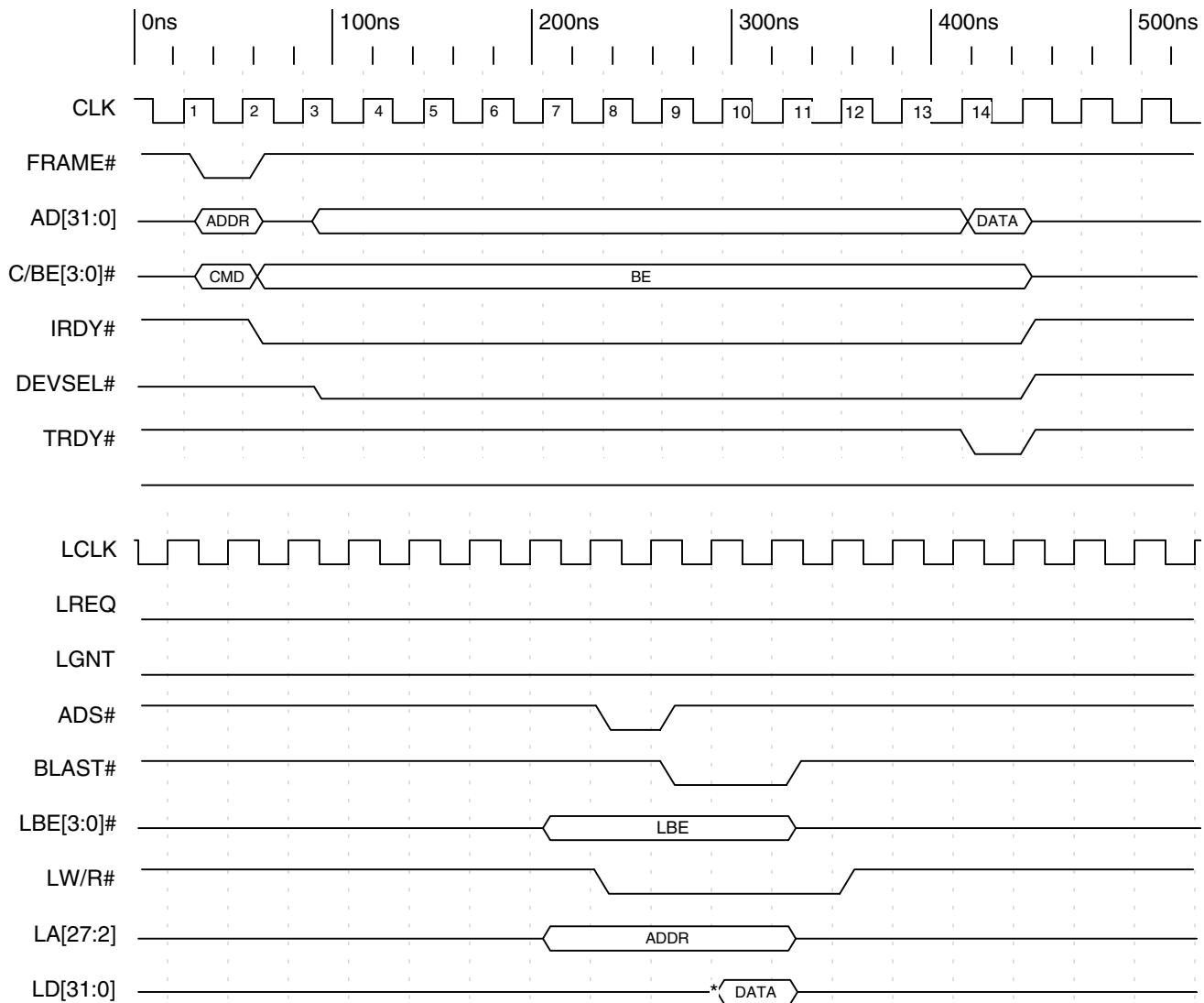
* Note: The PCI 9030 and Local memory will have one wait state without the READY# signal provided.

Timing Diagram 4-30. PCI Target Single Read with One Wait State Using Internal Wait State (32-Bit Local Bus), Non-Multiplexed Mode Only
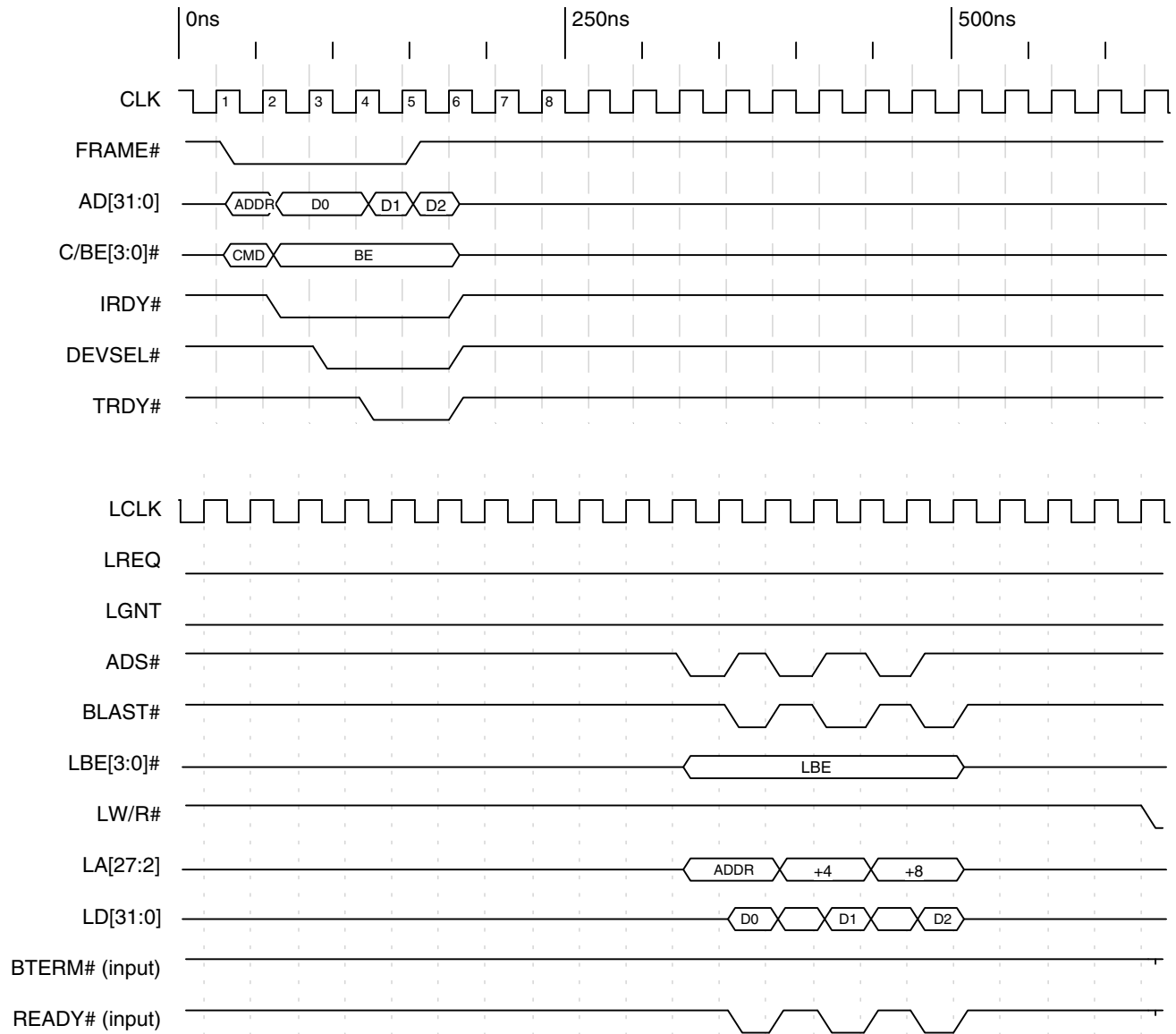
4—PCI Target

Timing Diagram 4-31. PCI Target Non-Burst Write (32-Bit Local Bus), Non-Multiplexed Mode Only

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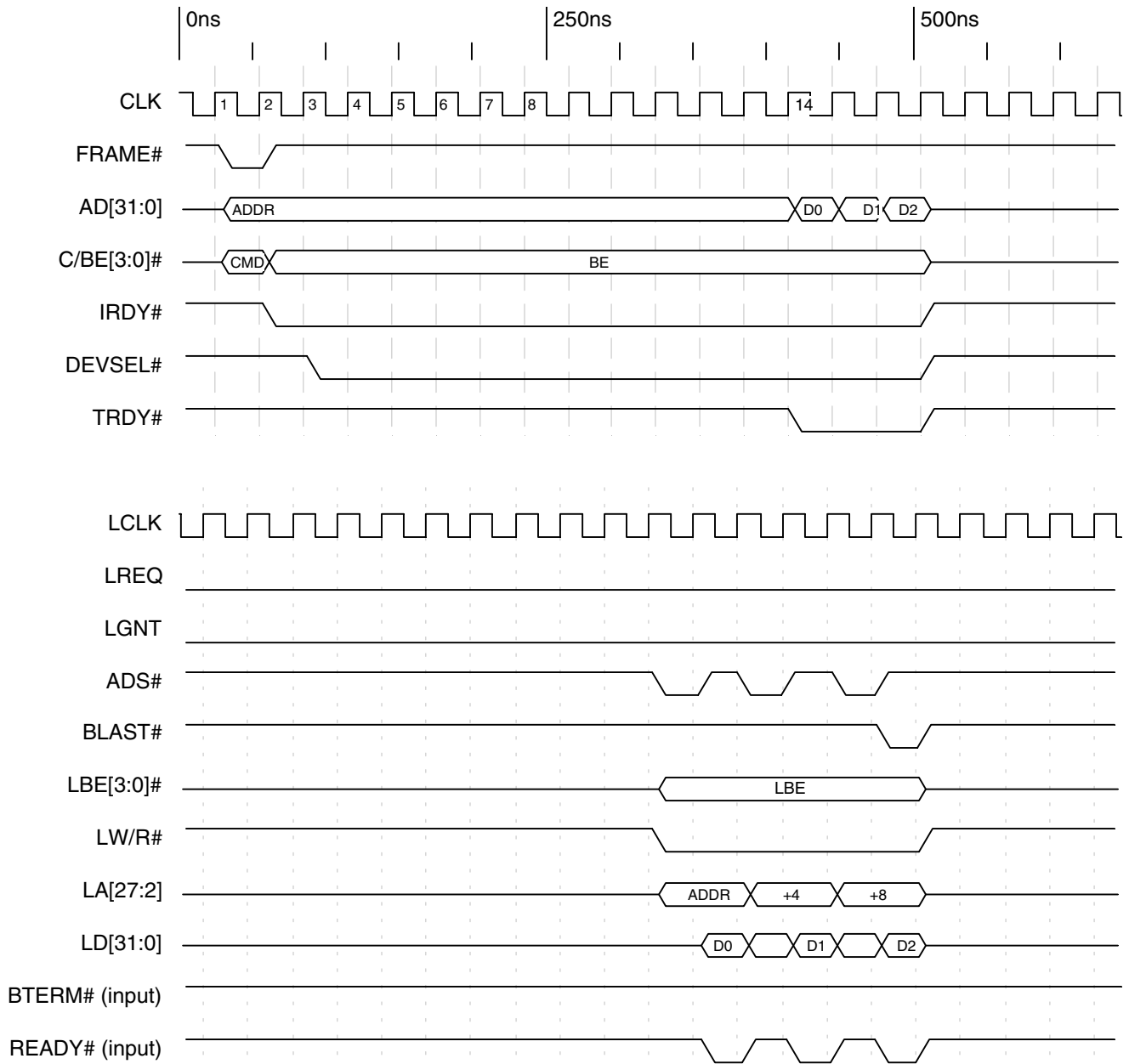
Timing Diagram 4-32. PCI Target Non-Burst Read, Non-Multiplexed Mode Only
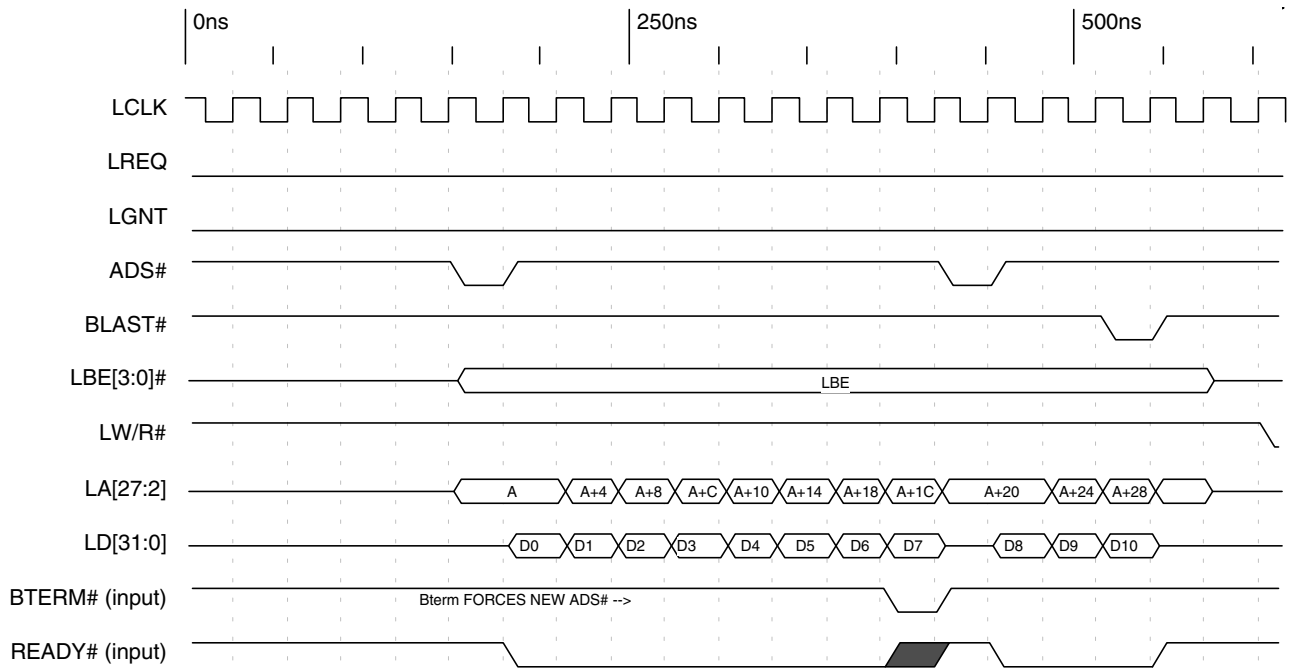
4—PCI Target

Eight Lword Burst, no wait states, Bterm enabled, Burst enabled, 32-bit Local Bus.

Note: If Bterm is disabled, a new ADS# cycle starts every quad-Lword boundary.

Timing Diagram 4-33. PCI Target Burst Write with Bterm Enabled (32-Bit Local Bus), Non-Multiplexed Mode Only

No wait states, Bterm disabled, Burst enabled, 32-bit Local Bus.
Unaligned Transfer results in new ADS#.

Note: Not all byte enables asserted on a quad boundary
LA[3:2]=11 results in a new ADS#.
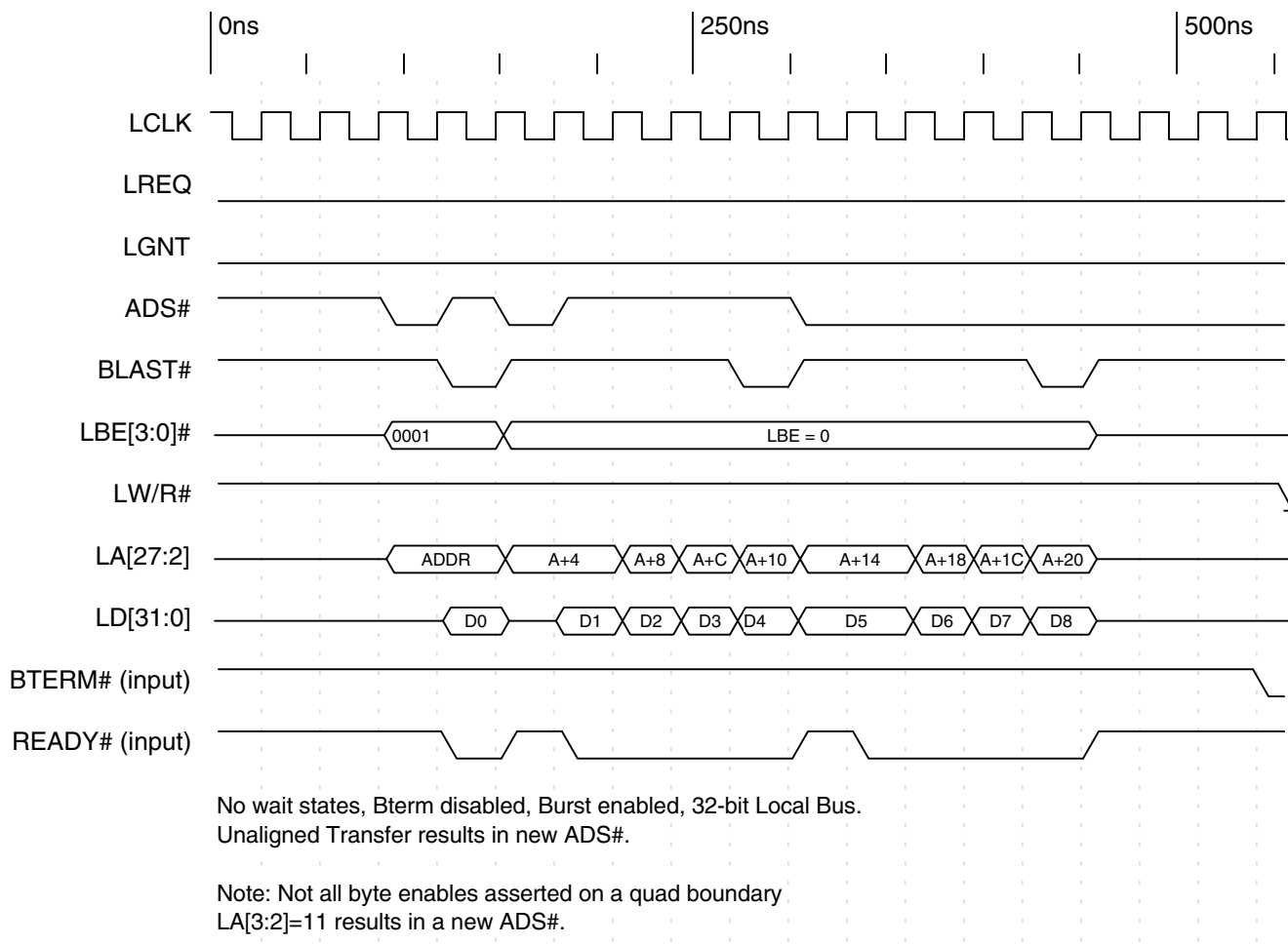
**Timing Diagram 4-34. PCI Target Burst Write with Bterm Disabled (32-Bit Local Bus),
Non-Multiplexed Mode Only**
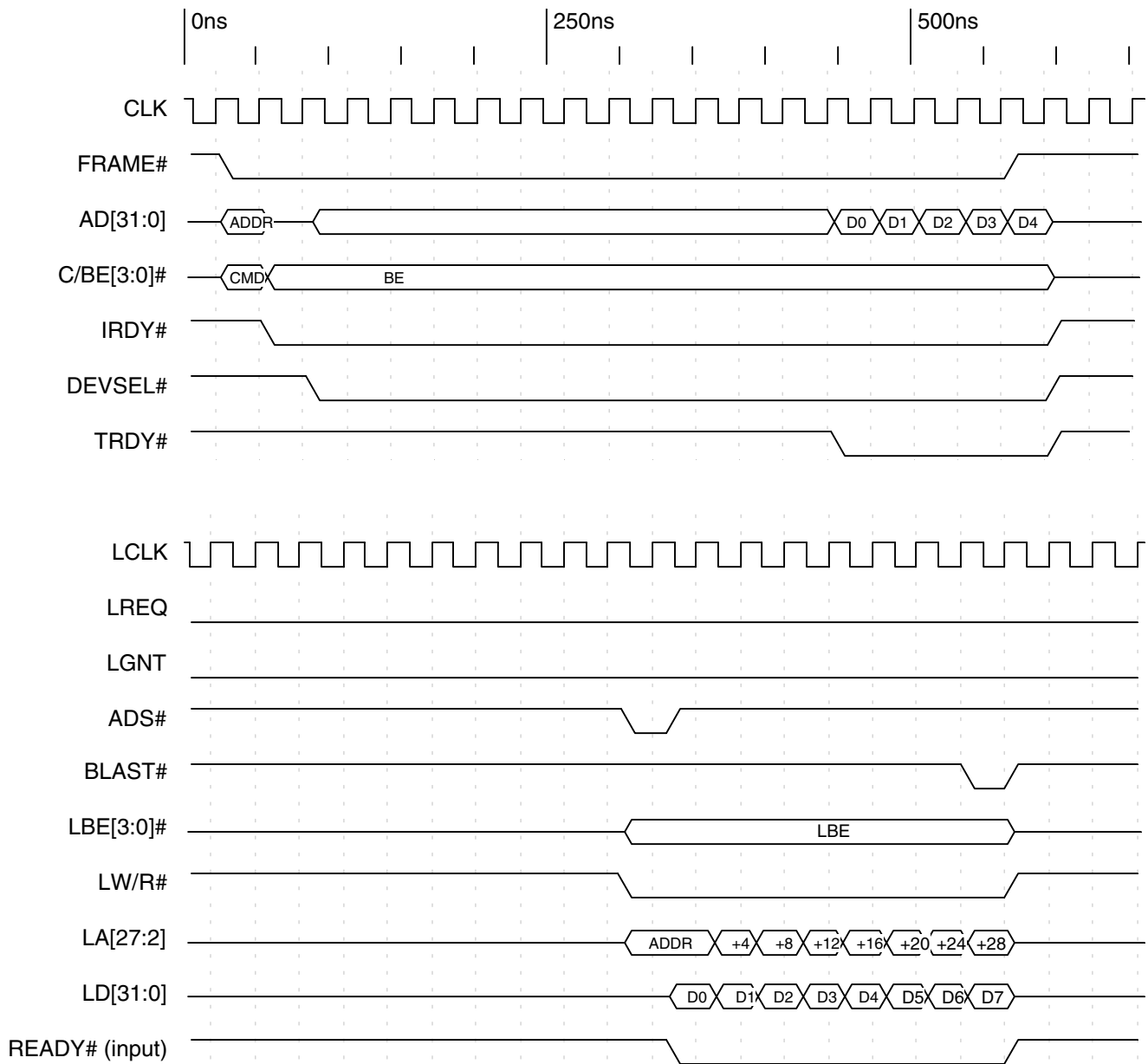
4—PCI Target

**Timing Diagram 4-35. PCI Target Burst Read with Prefetch Counter Set to 8 (32-Bit Local Bus),
Non-Multiplexed Mode Only**

Five Lwords, one external wait state, Bterm enabled, Burst enabled.
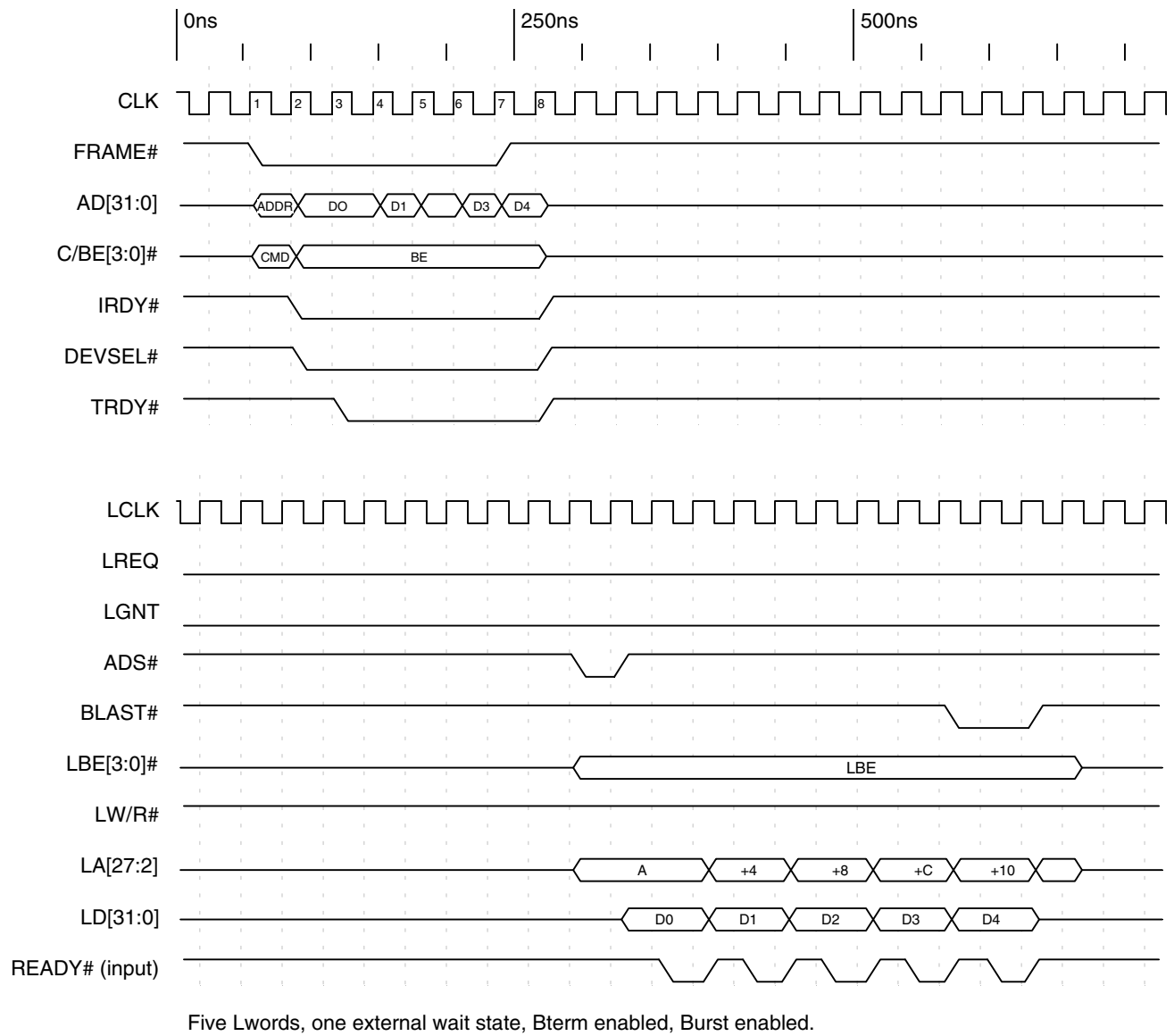
Timing Diagram 4-36. PCI Target Burst Write (32-Bit Local Bus), Non-Multiplexed Mode Only
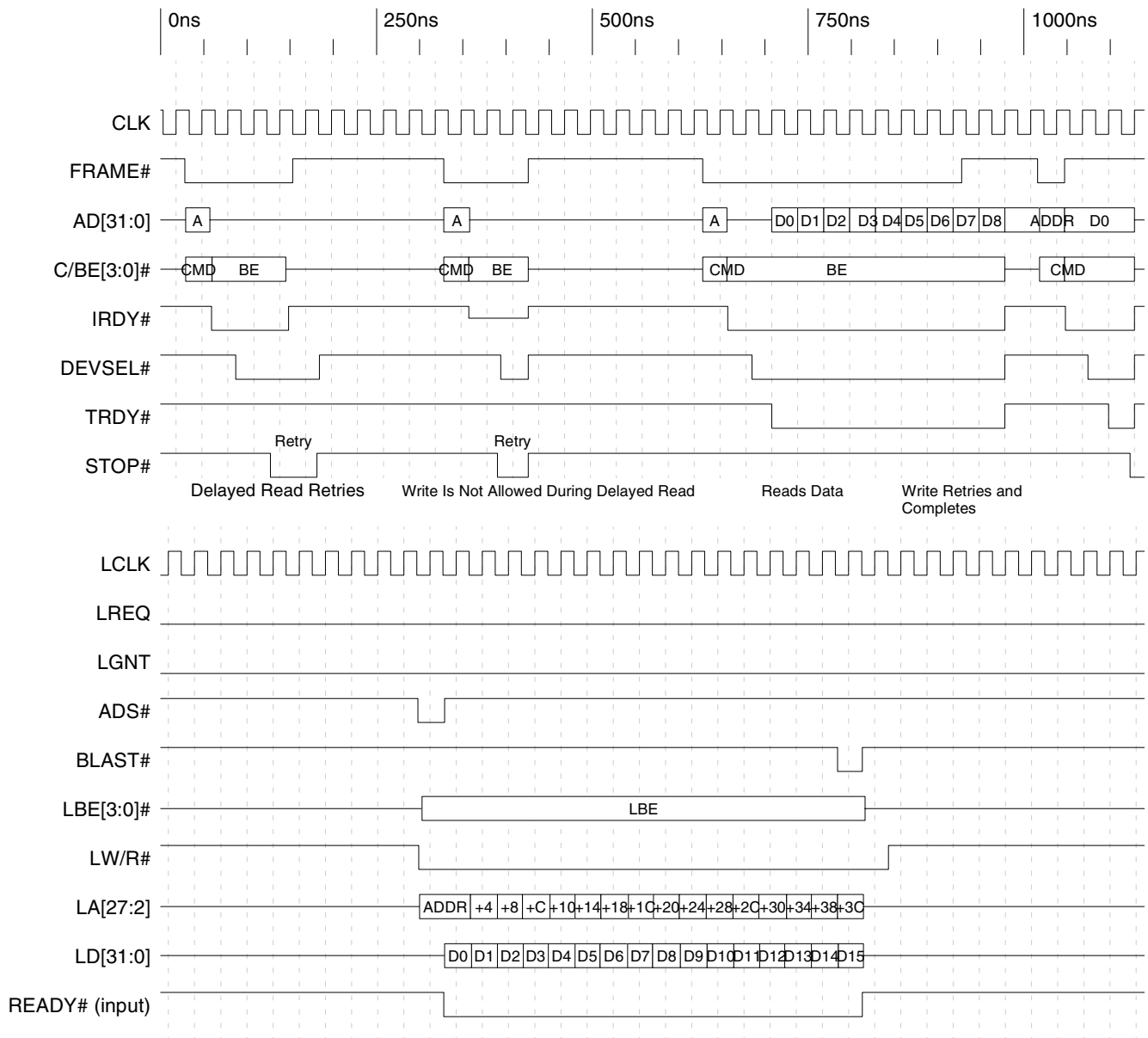
Disconnect immediately for a read. Does not affect pending reads when a Write cycle occurs, nor flush the Read FIFO if the PCI Read cycle completes.

When a read is pending, force Retry on a write. De-assert TRDY# until space is available in the

Timing Diagram 4-37. *PCI r2.2* Features Enable, Non-Multiplexed Mode Only
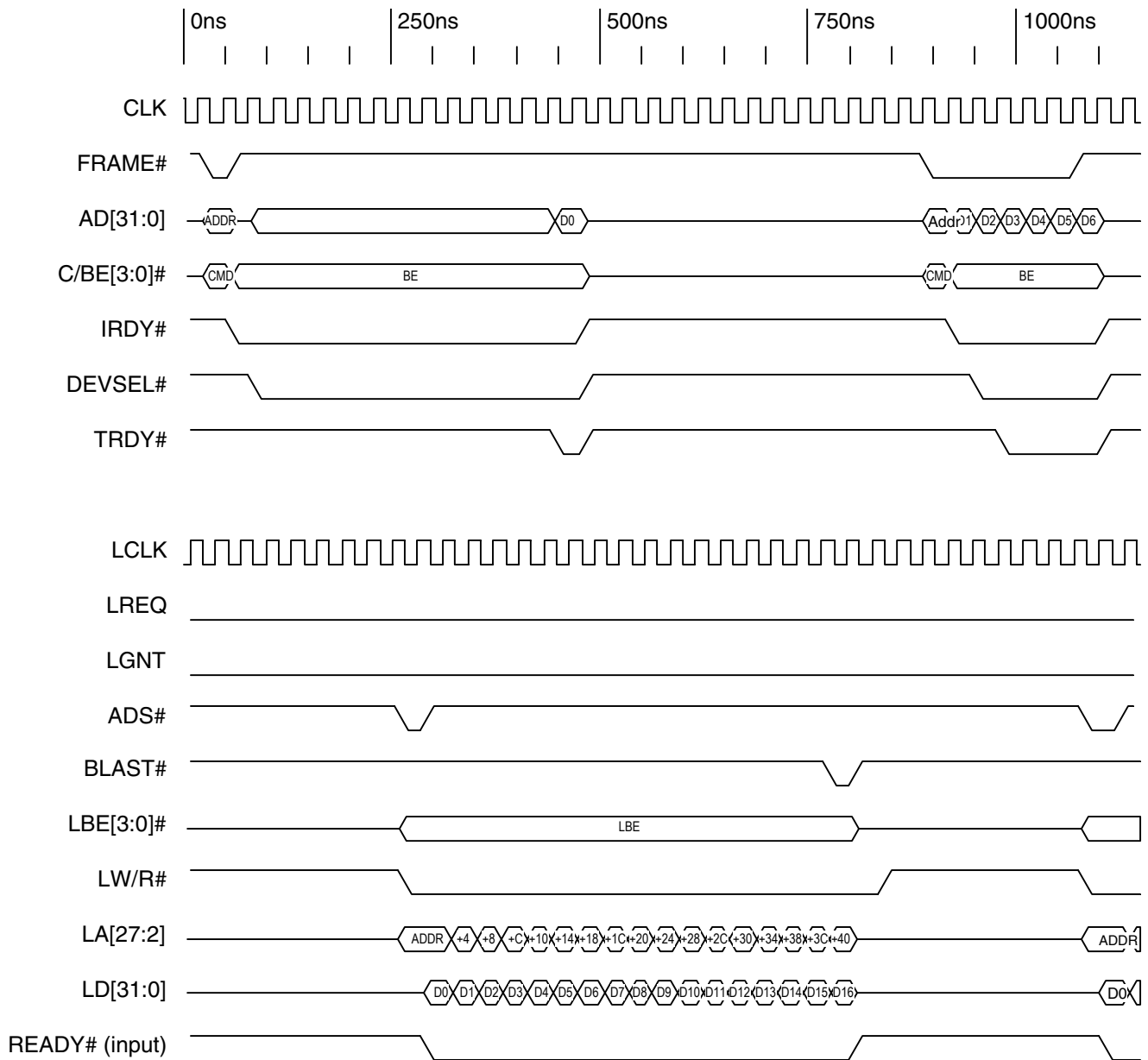
Timing Diagram 4-38. PCI Target Read No Flush Mode (Read Ahead Mode), Prefetch Enabled, Prefetch Count Disabled, Burst Enabled, Non-Multiplexed Mode Only
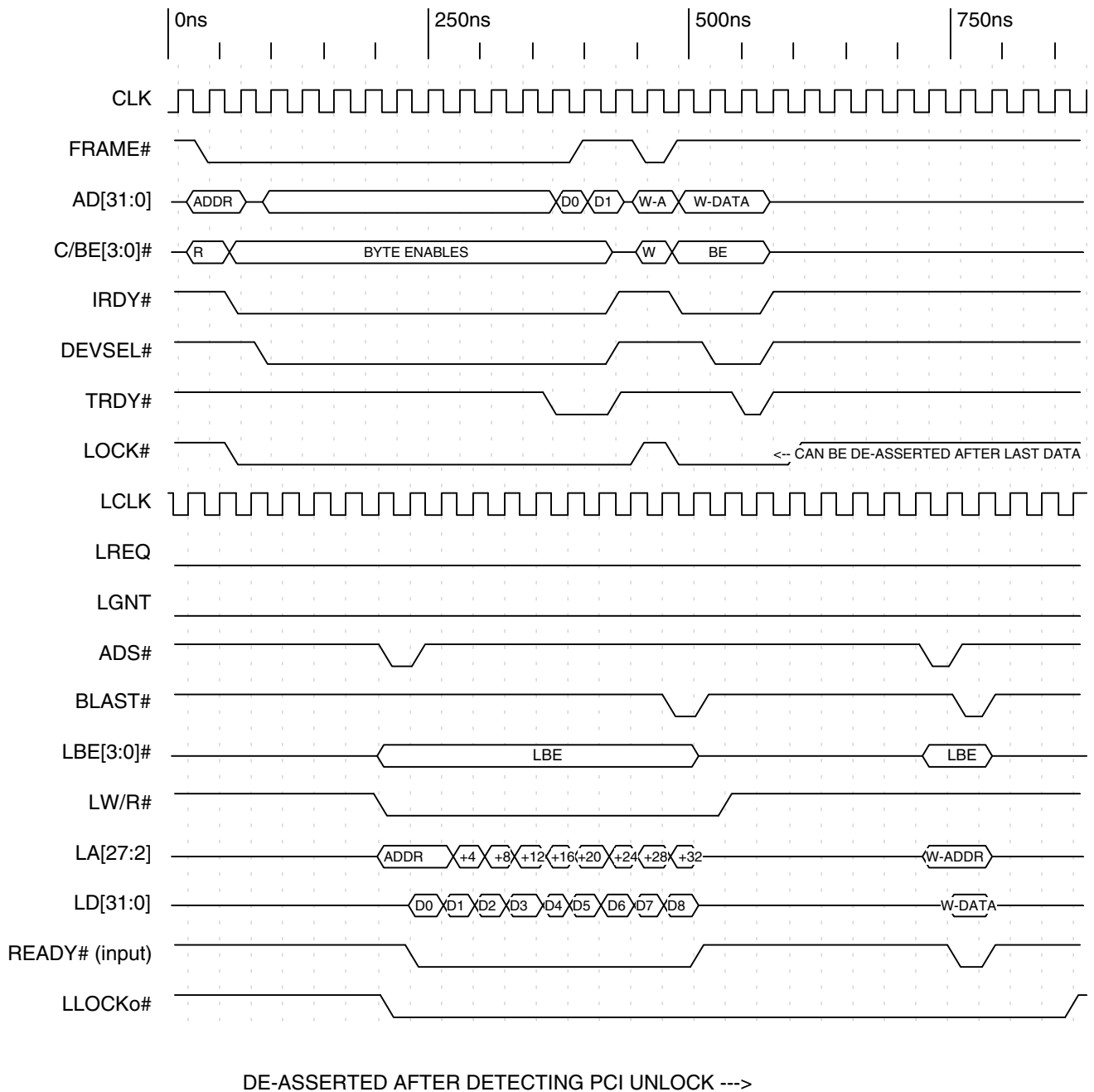
4—PCI Target

Timing Diagram 4-39. Locked PCI Target Read Followed by Write and Release (LLOCKo#), Non-Multiplexed Mode Only
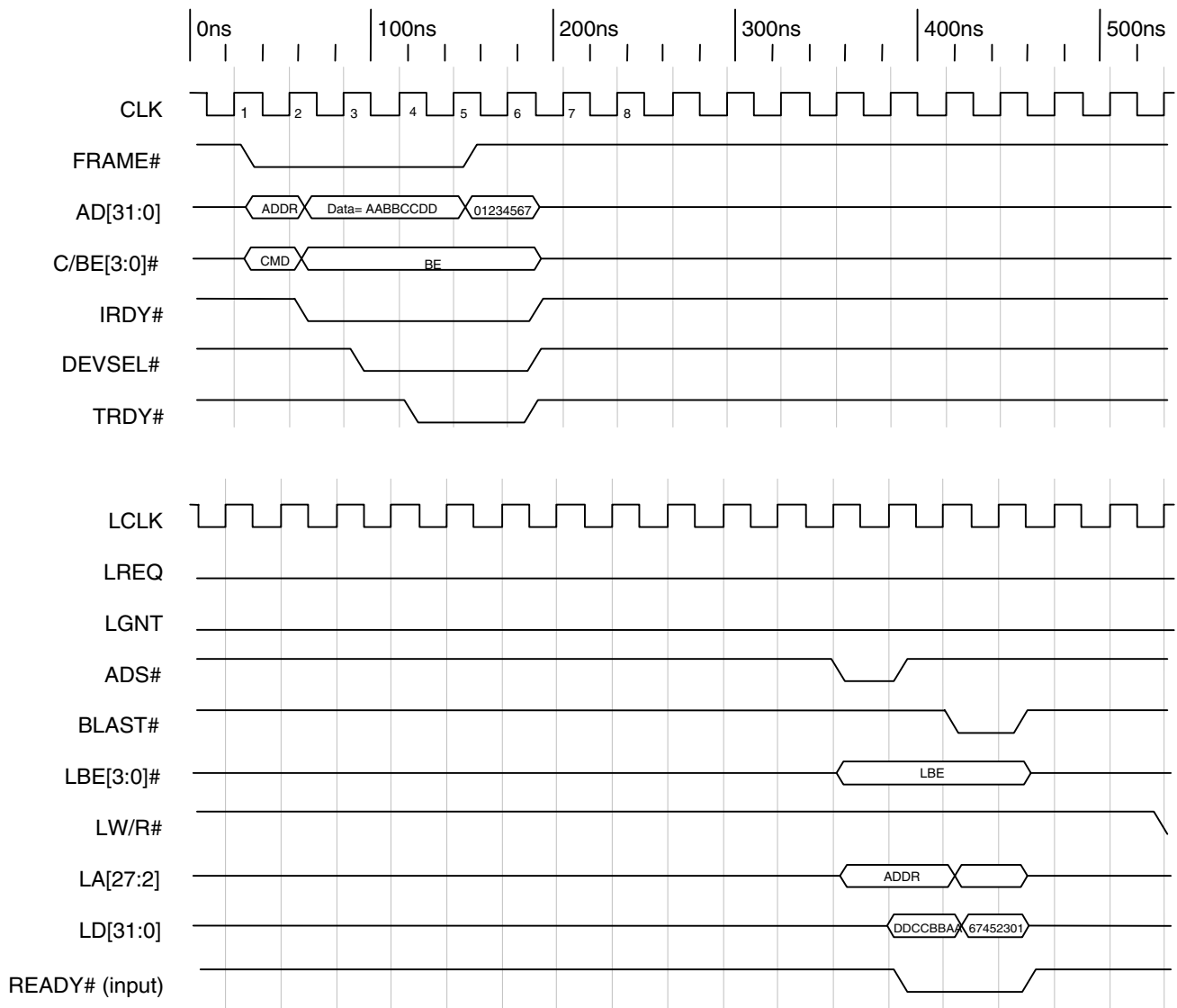
Timing Diagram 4-40. PCI Target Write to Local Target in BIGEND Mode, Non-Multiplexed Mode Only

4—PCI Target

5   LOCAL CHIP SELECTS

5.1   OVERVIEW

The PCI 9030 provides four chip select outputs to selectively enable devices on its Local Bus. Each active-low chip select is programmable and independent of any local address space. Without this feature, external address decoding logic is required to implement chip selects.

5.2   CHIP SELECT BASE ADDRESS REGISTERS

There are four Chip Select Base Address registers. These registers control the four chip select pins on the PCI 9030. [*For example*, Chip Select 0 Base Address register (CS0BASE) controls CS0#, Chip Select 1 Base Address register (CS1BASE) controls CS1#, and so forth.]

The Chip Select Base Address registers serve three purposes:

1. To enable or disable chip select functions within the PCI 9030. If enabled, the chip select signal is active if the Local Bus Address falls within the address specified by the range and base address. If disabled, the chip select signal is not active.

2. To set the range of the Local Bus Addresses for which the chip select signal(s) is active.

3. To set the Local Base Address, at which the range starts.

The three rules used to program the Chip Select Base Address registers are as follows:

1. Range must be a power of 2 (only the most significant bit is 1).

2. Base address must be a multiple of the range or 0.

3. Address range must be encompassed by one or more Local Address Spaces. Otherwise, the chip select decoder does not see addresses which have not been claimed by the PCI 9030 on behalf of a Local Address Space, and a chip select is not asserted.

Chip selects are not bound to any particular Local Address Space unless programmed accordingly in the CS*x*BASE, LAS*x*RR, and LAS*x*BA registers (where *x* is the Chip Select number or Local Address Space number, as appropriate).

Each 28-bit Chip Select Base Address register is programmed, as listed in the following table.

Table 5-1. Chip Select Base Address Register Signal Programming

MSB=27						LSB=0
XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXY

The *Y* bit (bit 0) enables or disables the chip select signal. *X* bits are used to determine the range and base address of where the CS# pin is asserted. To program the base and range, the *X* bits are set as follows:

*   Device length or range is specified by the first bit set above the *Y* bit. Determined by setting a bit in the register, calculated by shifting the range value (a power of 2) one bit to the right (range divided by 2).
*   Base Address is determined by the bit(s) set above the Range bit. The address is not shifted from its original value. The base address uses all bits in the register above (to the left of) the range bit, and none of the bits in the register at or below (to the right of) the Range bit.
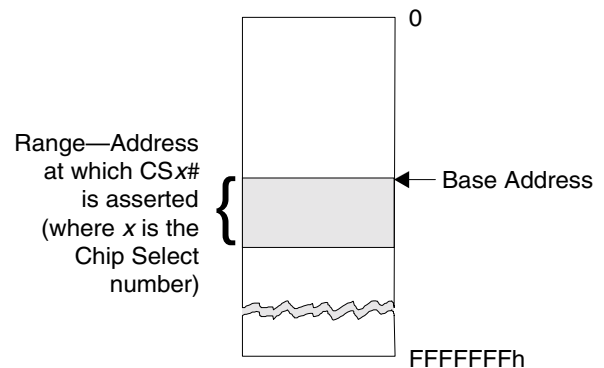
Figure 5-1. Chip Select Base Address and Range

5.3 PROCEDURE FOR USING CHIP SELECT BASE ADDRESS REGISTERS

The following describes the procedure for using the Chip Select Base Address registers.

1. Determine the range in hex. The range must be a power of 2 (only the highest order bit is set).

2. Set a bit in the Chip Select Base Address register to specify the range. Calculate this value by shifting the range value one bit to the right (range divided by 2). Only one bit may be set to encode the range.

3. Determine the base address. The base address must be a multiple of the range [the base address cannot contain ones (1) at or below (to the right of) the encoded range bit]. Set the base address directly into the bits above the range bit. The base address is not shifted from its original value.

4. Set the Enable bit (bit 0) in the Chip Select Base Address register to 1.

5.3.1 Chip Select Base Address Register Programming Example

A 16K chip select device is attached to the Local Bus and a chip select is provided. The base address is specified to be 24000h. The following figure illustrates this example.
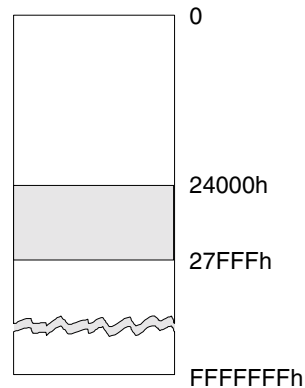
Figure 5-2. Memory Map Example

1. Determine the range in hex and divide the value by 2 (*for example*, 16K is equivalent to 4000h, leaving the range encoding at 2000h).

2. Determine the base address (*for example*, 24000h). Verify that the base address does not overwrite the range bit or any lower bits.

3. Set the base address into the bits above the range encoding. The base address is not shifted from its original value.

4. Set the Enable bit (bit 0).

The following is a complete example of setting the Chip Select Base Address register with a range of 4000h, a base address of 24000h, and enabled:

MSB=27						LSB=0
0000	0000	0010	0110	0000	0000	0001

5.4   CHIP SELECT TIMING DIAGRAMS
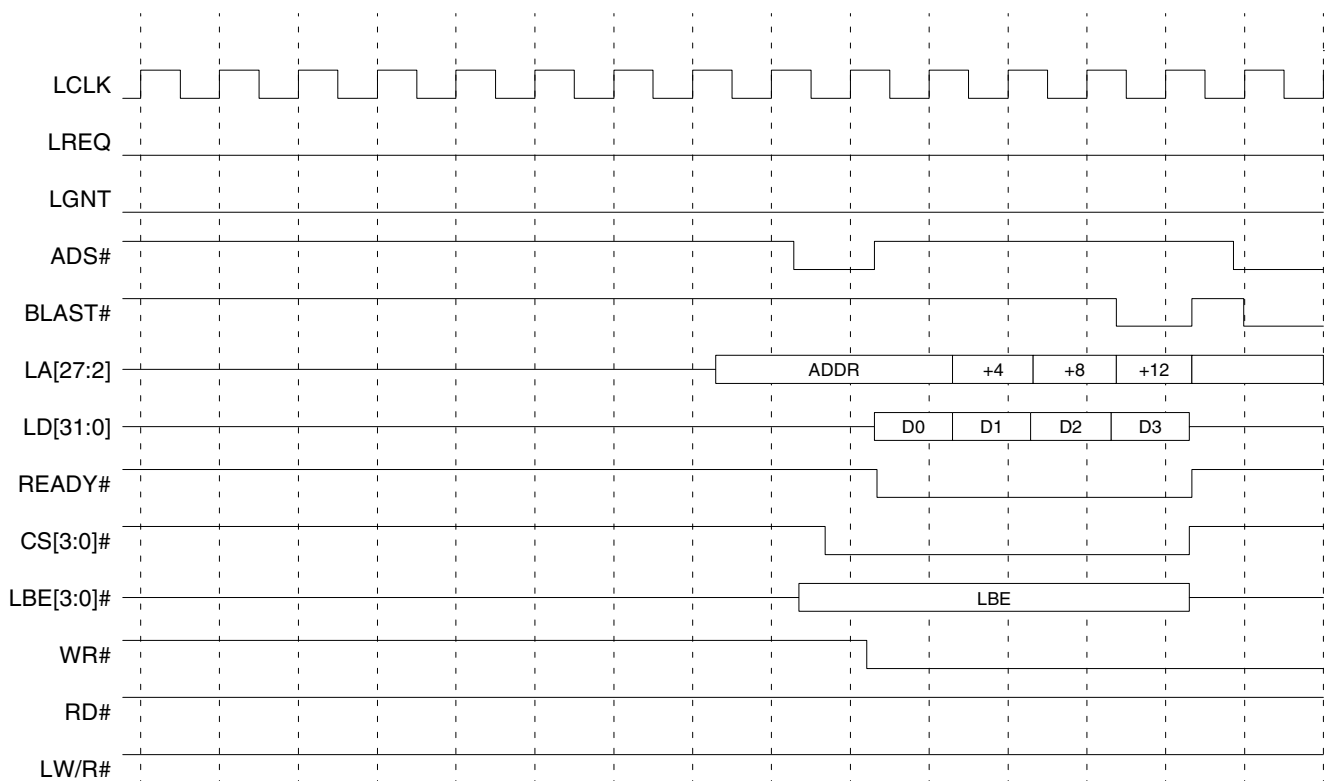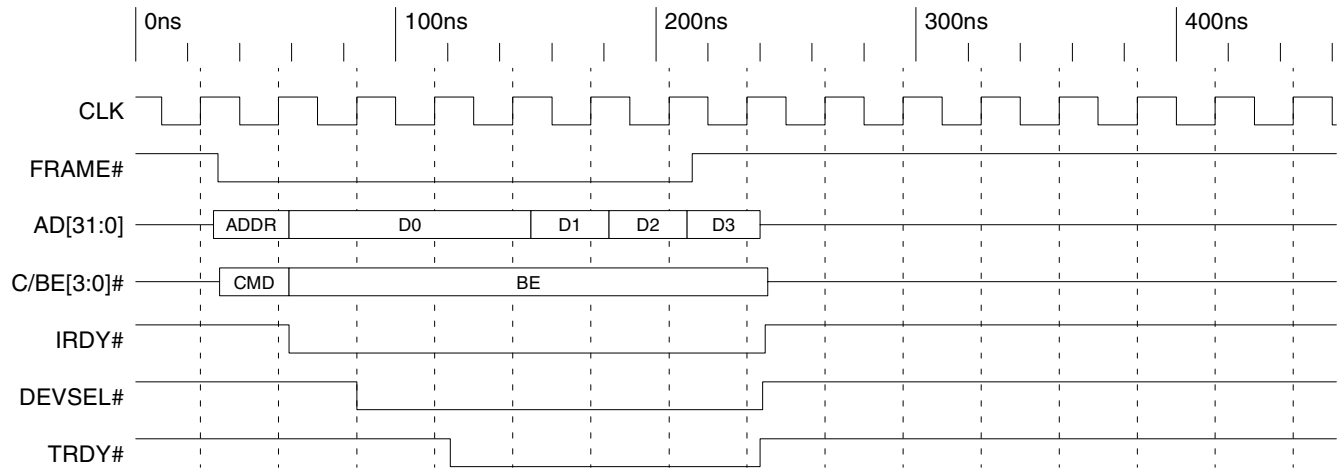
Note: CS[3:0]# Base Address is in the range of Local Address Spaces 3 through 0.

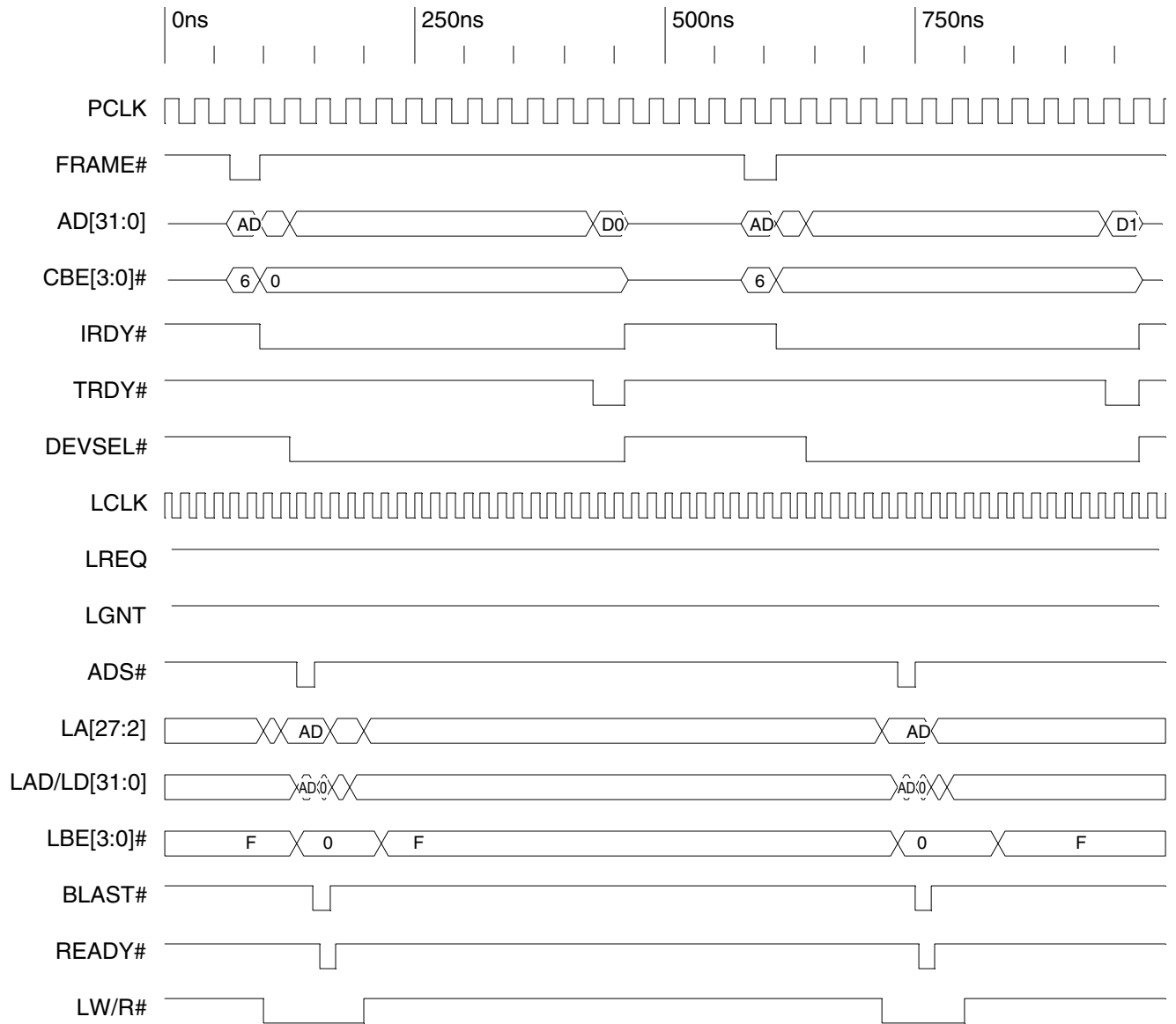**Timing Diagram 5-1. Chip Select [3:0]# (32-Bit Local Bus)**
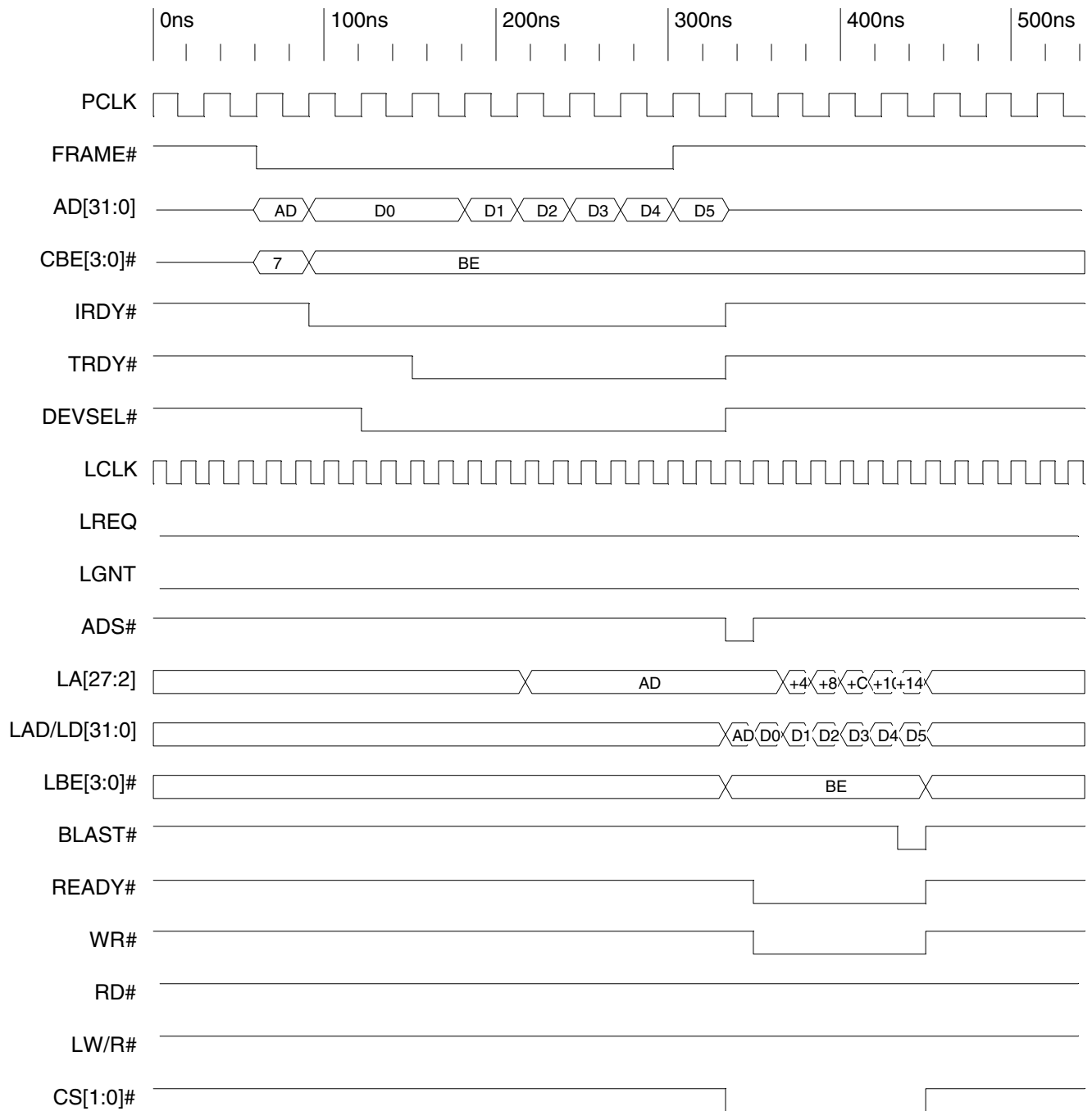
Note: For Multiplexed mode, use the LAD[31:0] signal for address.
For Non-Multiplexed mode, use the LA[27:2] signal for address.
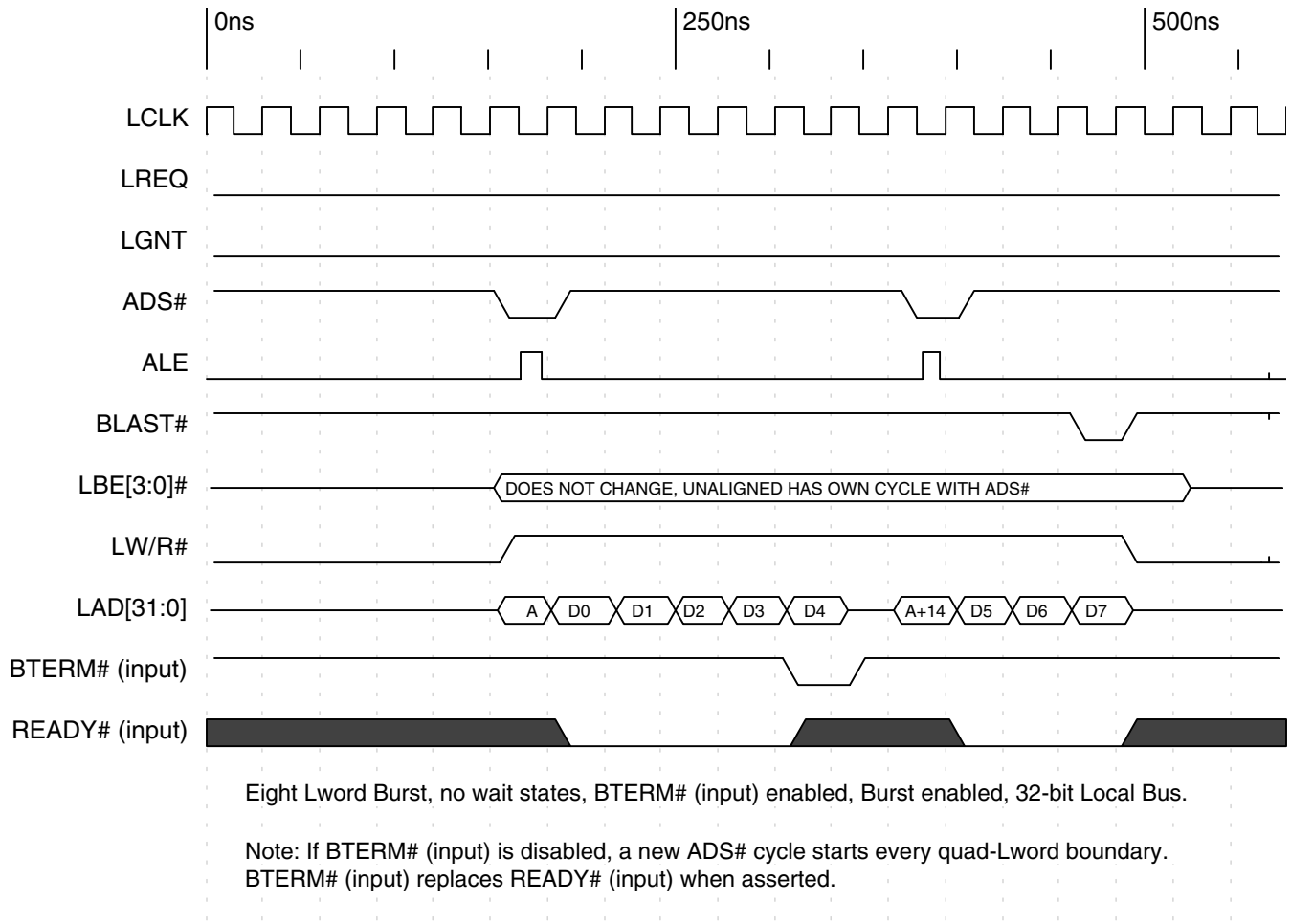
Timing Diagram 5-2. PCI Target Burst Write with Delayed Write and Chip Select Enabled (32-Bit Local Bus)

6 INTERRUPTS AND GENERAL PURPOSE I/O

6.1 OVERVIEW

The PCI 9030 provides two Local interrupt input pins (LINTi[2:1]) and a register bit in the Interrupt Control/Status register (INTCSR[7]) that can optionally trigger PCI interrupt INTA# output. The interrupt input pins have an associated register bit to enable or disable the pin (INTCSR[3, 0], respectively), and each has a Status bit to indicate whether an interrupt source is active (INTCSR[5, 2], respectively). The LINTi[2:1] pins are programmable for active-low or active-high polarity in the default Level-Sensitive mode. They can be optionally configured as a rising edge-triggered interrupt (*such as*, for ISA compatibility).

Level-sensitive interrupts are cleared when the interrupt source is no longer active, or the interrupt input pin is disabled. Edge-triggered (latched) interrupts remain active until cleared by a software write, which either asserts the associated Local Edge Triggerable Interrupt Clear bit(s) (INTCSR[11:10], respectively), or disables the interrupt input pin. INTA# output can also be de-asserted by clearing the PCI Interrupt Enable bit (INTCSR[6]=0).

6.2 INTERRUPTS
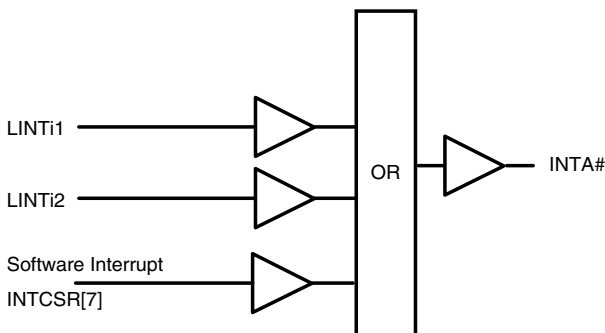
Figure 6-1. Interrupt and Error Sources

6.2.1 PCI Interrupts (INTA#)

A PCI 9030 PCI Interrupt (INTA#) can be asserted by Local Interrupt Input 2 or 1 (LINTi[2:1]), which are described in the next section. INTA# can also be asserted by setting the Software Interrupt bit (INTCSR[7]=1).

INTA# can be enabled or disabled (default configuration) in the Interrupt Control/Status register (INTCSR[6]). If a PCI interrupt is required, the PCI Interrupt Pin register (PCIIPR) must be set to a value of 1 at boot time by the serial EEPROM, or chip default value 1 if a blank or no serial EEPROM is used, so that BIOS can route INTA# to an interrupt controller interrupt request (IRQ) input. BIOS writes the assigned IRQ number to the PCI Interrupt Line register (PCIILR). PCIILR register bit values are system-architecture specific.

An INTA# assertion generated from either LINTi[2:1] input, configured as level-sensitive interrupts, is cleared when one of the following occurs:

- Interrupt source is no longer active
- Interrupt input pin is disabled
- PCI interrupts are disabled (INTCSR[6]=0)

Subsequent to disabling interrupts, if the Local interrupt input remains asserted and interrupts are re-enabled, another interrupt is generated.

An INTA# assertion generated from either LINTi[2:1] input, configured as edge-triggered interrupts, remains active regardless of the LINTi[2:1] input pin state, until the interrupt is cleared with a software write that performs one of the following:

- Asserts the associated Local Edge Triggerable Interrupt Clear bit(s) (INTCSR[11:10], respectively)
- Disables the interrupt input pin
- Disables PCI interrupts (INTCSR[6]=0)

Subsequent to disabling interrupts, if interrupts are re-enabled, another interrupt is not generated (although the LINTi[2:1] input state remains high) until the next low-to-high transition on the LINTi[2:1] input pin occurs.

A software interrupt can be enabled by setting the Software Interrupt bit (INTCSR[7]=1). INTA# is asserted if the PCI Interrupt Enable bit is also set (INTCSR[6]=1). INTA# output is subsequently de-asserted when the Software Interrupt or PCI Interrupt Enable bit is cleared (INTCSR[7 or 6]=0, respectively).

INTA# is a level output. If INTA# is asserted or de-asserted in response to LINTi[2:1] input, INTA# output timing is asynchronous to the PCI and Local clocks. If INTA# is asserted or de-asserted by software, INTA# output timing is referenced to a rising edge of the PCI clock.

Note: Regarding PLXMon, if PCI interrupts are enabled and the PCI 9030 generates an INTA#, the interrupt status displayed in PLXMon does not show the bit in the INTCSR control register as "active." This occurs because the PCI 9030 driver responds to the PCI interrupt and clears it. To test a PCI interrupt assertion and view active status with PLXMon, disable the PCI Interrupt Enable bit (INTCSR[6]=0), while keeping all other bit(s) required to generate the interrupt active. Then the driver does not see an INTA# assertion. After the screen is refreshed, following interrupt assertion, the active status can be seen in PLXMon.

6.2.2   Local Interrupt Input (LINTi[2:1])

The PCI 9030 provides two local interrupt input pins LINTi[2:1]. The Local interrupts can be used to generate a PCI interrupt, and/or software can poll the interrupt status bits (INTCSR[5,2]). LINTi[2:1] are programmable for active-low or active-high polarity (INTCSR[4, 1], respectively) in the default Level-Sensitive mode (INTCSR[9, 8]=00). Each pin can be optionally configured as a rising edge-triggered interrupt (INTCSR[8, 1, 0]=111 and INTCSR[9, 4, 3] =111), *such as*, for ISA compatibility. Level-sensitive interrupts are cleared when the interrupt source is no longer active, or the interrupt input pin is disabled. Edge-triggered (latched) interrupts remain active until cleared by a software write, which asserts the associated Interrupt Clear register bit(s) (INTCSR[11, 10]=11), or disables the interrupt input pin (INTCSR[3, 0]=00). If the PCI Interrupt Enable bit is set (INTCSR[6]=1) and INTA# is asserted for a Local interrupt input assertion, INTA# can be de-asserted by clearing the PCI Interrupt Enable bit (INTCSR[6]=0).

PCI 9030 sampling of enabled LINTi[2:1] inputs, and INTA# output state changes (if PCI interrupts are enabled) in response to enabled LINT[2:1] input, are asynchronous to the PCI and Local clocks.

6.2.3   Local Power Management Interrupt (LPMINT#)

The PCI 9030 is a PCI Target device only; therefore, there is no access to the internal registers from the Local Bus. The Local Power Management Interrupt output (LPMINT#) is included to accommodate the PCI Bus Power Management interface to a Local Bus.

The PCI 9030 asserts LPMINT# to request a Power State change to the Local Bus when the Power State bit(s) change (PMCSR[1:0]). The LPMINT# interrupt is synchronous to the Local clock. When asserted, it is a one clock-wide pulse.

External glue logic is needed to latch the Power State change and to retain the previous Power State history for further evaluation by the external Local Bus Initiator.

6.2.4   Local Power Management Enumerator Set

The Local Power Management Enumerator Set Interrupt input (LPMESET) is included to accommodate the PCI Bus Power Management interface to a Local Bus.

The external Local Bus Initiator can assert LPMESET to the PCI 9030 Power Management Control/Status register (PMCSR[15]) to set the PME# status and assert the PME# signal to the PCI Bus in case of a Wake-up Request event.

6.2.5   All Modes PCI SERR# (PCI NMI)

The PCI 9030 asserts a SERR# pulse if parity checking is enabled (PCICR[6]=1) and it detects an address parity error.

The SERR# output can be enabled or disabled with the SERR# Enable bit (PCICR[8]).

6.3   GENERAL PURPOSE I/O

The PCI 9030 supports nine general purpose input and output pins, multiplexed GPIO0/WAITo#, GPIO1/ LLOCKo#, GPIO2/CS2#, GPIO3/CS3#, GPIO4/LA27, GPIO5/LA26, GPIO6/LA25, and GPIO7/LA24, and GPIO8. The PCI 9030 default condition is the General Purpose Input for GPIO[3:0], with Local Address LA[27:24] for GPIO[4:7], and General Purpose Input for GPIO8. The general purpose I/O pins and functionality can be enabled and selected in the General Purpose I/O Control register (GPIOC[31:0]).

GPIO[8:0] pins configured as inputs (GPIO[8, 3:0] are inputs with the default GPIOC register value) are active regardless of whether the PCI 9030 owns the Local Bus.

GPIO[8:0] pins configured as outputs are driven only when the PCI 9030 owns the Local Bus. (Refer to *PCI 9030 Errata #2*.)

It is recommended that unused GPIO pins be configured as outputs, rather than inputs (by default, GPIO[8, 3:0] are inputs); otherwise, input pins should be pulled to a known state.

6—Interrupts, I/O

6.4　　INTERRUPTS AND GENERAL PURPOSE I/O TIMING DIAGRAMS
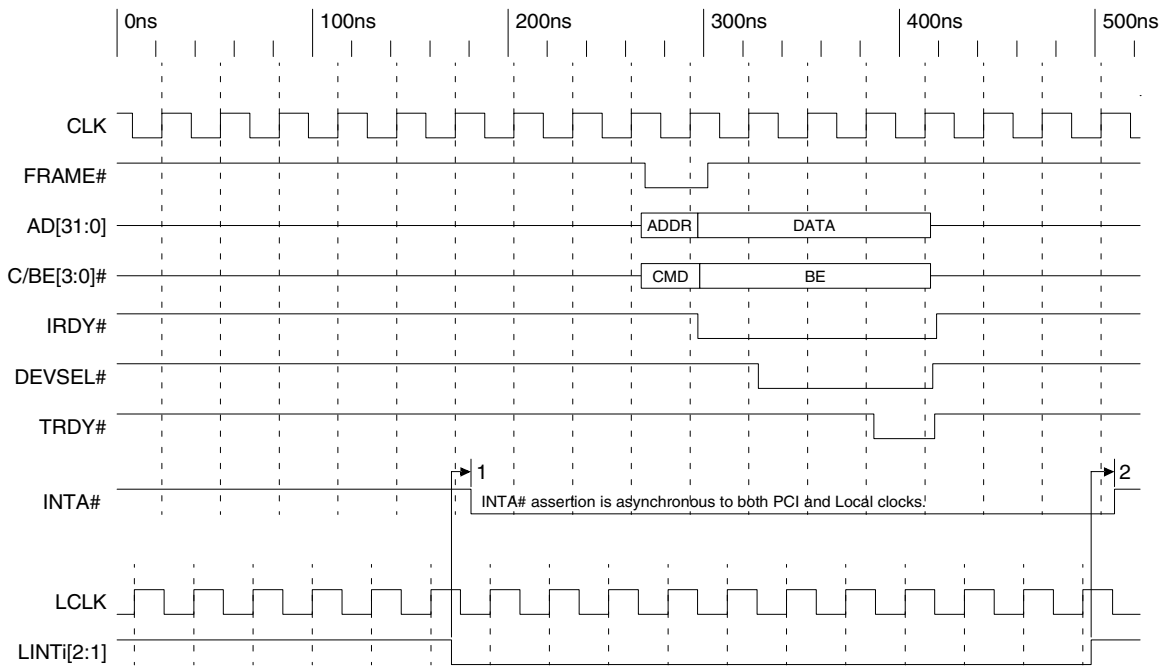
Timing Diagram 6-1.　Local Level-Triggered Interrupt Asserting PCI Interrupt
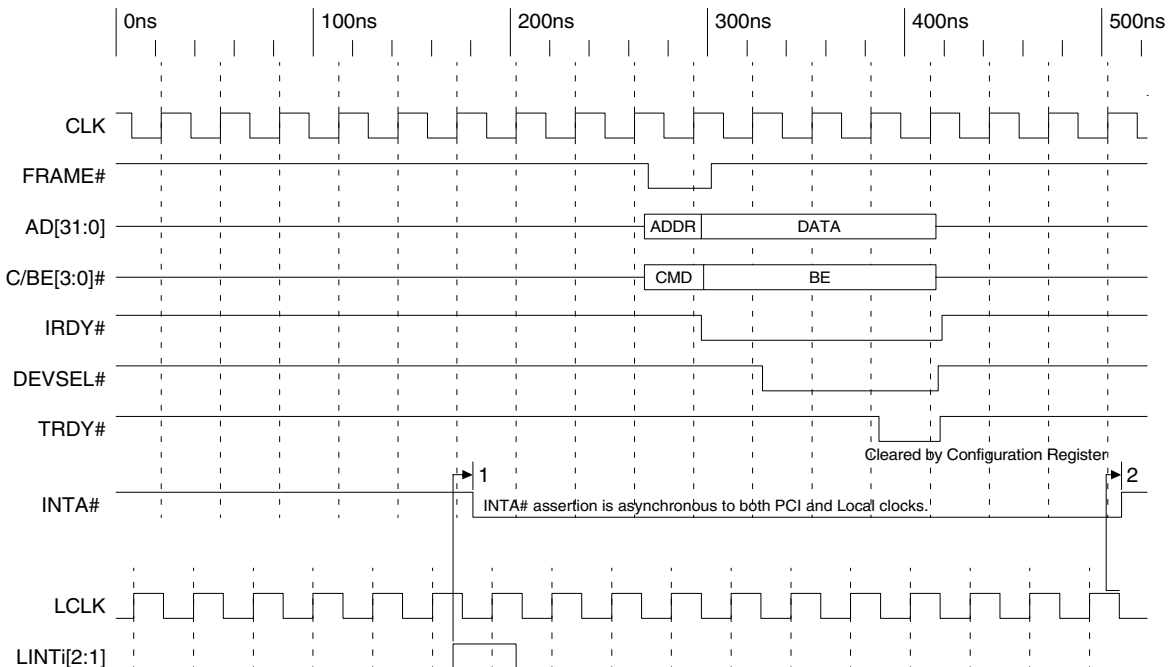
Timing Diagram 6-2.　Local Edge-Triggered Interrupt Asserting PCI Interrupt
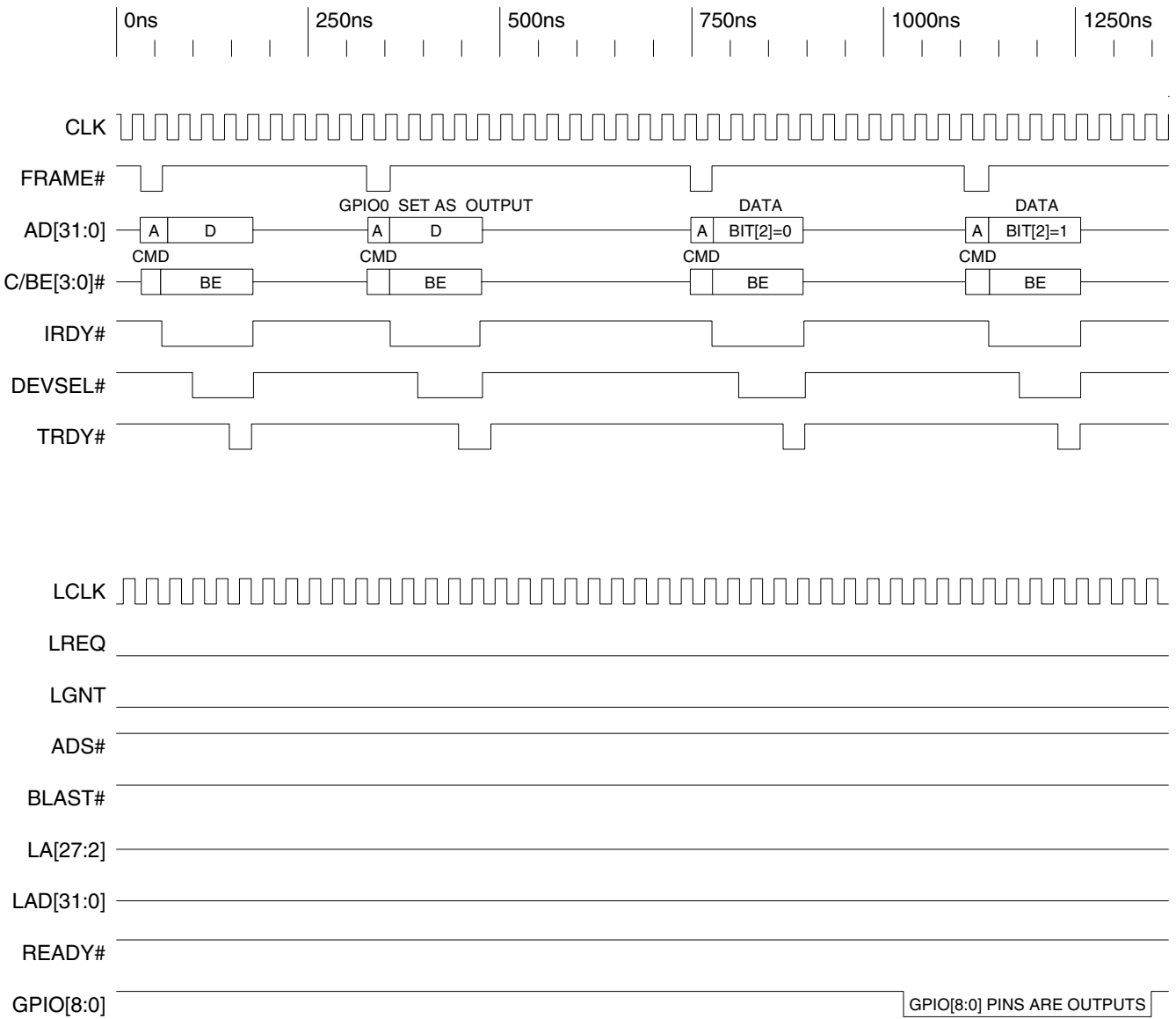
0ns   250ns   500ns   750ns   1000ns   1250ns

CLK

FRAME#

AD[31:0]   GPIO0 SET AS OUTPUT   DATA   DATA
A   D   A   D   A   BIT[2]=0   A   BIT[2]=1
CMD   CMD   CMD   CMD

C/BE[3:0]#   BE   BE   BE   BE

IRDY#

DEVSEL#

TRDY#

LCLK

LREQ

LGNT

ADS#

BLAST#

LA[27:2]

LAD[31:0]

READY#

GPIO[8:0]   GPIO[8:0] PINS ARE OUTPUTS

Note: GPIO pins configured as outputs are driven only when the PCI 9030 owns the Local Bus.
(Refer to *PCI 9030 Errata #2*.)

Timing Diagram 6-3. GPIO[8:0] as Outputs

6—Interrupts, I/O

7   PCI POWER MANAGEMENT

7.1   OVERVIEW

PCI Power Mgmt. r1.1 provides a standard mechanism for operating systems to control add-in boards for power management. It defines four PCI functional power states—D_0, D_1, D_2, and D_3. States D_0 and D_3 are required, while states D_1 and D_2 are optional. State D_0 represents the highest power consumption and state D_3 the least.

- **D_0 (Uninitialized)**—Enters this state from Power-On Reset or from state D_{3hot} or D_{3cold}. Supports only PCI Target transactions.

- **D_0 (Active)**—All functions active.

- **D_1**—Uses less power than State D_0, and more than state D_2. Light Sleep State. ***Not supported by the PCI 9030.***

- **D_2**—Uses very little power.

  Supports PCI Configuration cycles to function if clock is running (Memory, I/O, Bus Mastering, and Interrupts are disabled). It also supports the Wake-up Event from function, but not standard PCI interrupts. ***Not supported by the PCI 9030.***

- **D_{3hot}**—Uses lower power than any other state. Supports PCI Configuration cycles to function if clock is running. Supports Wake-up Event from function, but not standard PCI interrupts. When programmed for state D_0, an internal soft reset occurs. The PCI Bus drivers must be disabled. PME# context must be retained during this soft reset.

- **D_{3cold}**—No power. Supports only Bus reset. All context is lost in this state.

From a power management perspective, the PCI Bus can be characterized at any point in time by one of four power management states—B_0, B_1, B_2, and B_3:

- **B_0 (Fully On)**—Bus is fully usable with full power and clock frequency, *PCI r2.2* compliant. Fully operational bus activity. This is the only Power Management state in which data transactions can occur.

- **B_1**—Intermediate power management state. Full power with clock frequency, *PCI r2.2* compliant. PME Event driven bus activity. V_{CC} is applied to all devices on the bus, and no transactions are allowed to occur on the bus.

- **B_2**—Intermediate power management state. Full power clock frequency stopped, *PCI r2.2* compliant (in the low state). PME Event-driven bus activity. V_{CC} is applied to all devices on the bus; however, the clock is stopped and held in the Low state.

- **B_3 (Off)**—Power to the bus is switched off. PME Event-driven bus activity. V_{CC} is removed from all devices on the PCI Bus.

All system PCI Buses have an originating device, which can support one or more power states. In most cases, this creates a bridge (*such as*, a Host-to-PCI Bus or a PCI-to-PCI bridge).

Function States must be at the same or lower energy state than the bus on which they reside.

7.2   PCI POWER MANAGEMENT FUNCTIONAL DESCRIPTION

The PCI 9030 passes power management information and has no inherent power-saving feature. The PCI 9030 supports D_0, D_{3hot}, and D_{3cold} states (the PCI 9030 does not support PME# assertion in the D_{3cold} state).

The PCI Status register (PCISR) and the New Capability Pointer register (CAP_PTR) indicate whether a new capability (the Power Management function) is available. The New Capability Functions Support bit (PCISR[4]) enables a PCI BIOS to identify a New Capability function support. This bit is executable for writes from the serial EEPROM and reads from the PCI Bus. CAP_PTR provides an offset into PCI Configuration Space, the start location of the first item in a New Capabilities Linked List.

The Power Management Capability ID register (PMCAPID) specifies the Power Management Capability ID, 01h, assigned by the PCI SIG. The Power Management Next Capability Pointer register (PMNEXT) points to the first location of the next item in the capabilities linked list. If Power Management is the last item in the list, then this register should be set to 0h. The default value for the PCI 9030 is 48h (Hot Swap).

For the PCI 9030 to change the power state and assert PME#, the serial EEPROM or PCI Host should set the PME_En bit (PMCSR[8]=1). The Local Host then determines to which power state the backplane

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should change by monitoring the Power_State bits (PMCSR[1:0]), by way of the LPMINT# interrupt signal.

The PCI 9030 is a PCI Target device only; therefore, there is no access to the internal registers from the Local Bus. The Local Power Management Interrupt output (LPMINT#) is included to accommodate the PCI Power Management interface to a Local Bus.

The PCI 9030 asserts LPMINT# to request a Power State change to an external Local Bus Initiator when the Power Management Control/Status register (PMCSR[1:0]) changes. The LPMINT# interrupt is synchronous to the Local clock. When asserted, it is one clock-wide pulse.

External Local glue logic is needed to latch the Power State change and to retain the previous Power State history for further evaluation by the external Local Bus Initiator.

The PCI 9030 uses the PME_Support bits (PMC[15:11]) to identify the PME# Support corresponding to a specific power state (PMCSR[1:0]). PMC[15:11] are configured by way of the serial EEPROM.

The Local Host then sets the PME_Status bit (PMCSR[15]=1), by way of LPMESET, and the PCI 9030 asserts PME#. To clear the PME_Status bit, the PCI Host must write 1 to the status bit (PMCSR[15]=1). To disable the PME# Interrupt signal, either the PCI Host or serial EEPROM can write 0 to the PME_En bit (PMCSR[8]=0).

The Local Power Management Enumerator Set Interrupt input (LPMESET) is included to accommodate the PCI Power Management interface to a Local Bus.

The external Local Bus Initiator can assert LPMESET to the PCI 9030 Power Management Control/Status register (PMCSR[15]) to set the PME# status and assert the PME# signal in the case of a Wake-up Request event to the PCI Bus.

LPMINT# output is asserted every time the power state in the PMCSR register changes. Transition from state 11 (D_{3hot}) to state 00 (D_0) causes a soft reset and serial EEPROM reload. During a soft reset, the Local Bus interface is in Reset mode. The PCI 9030 issues LRESETo# and resets the Local Bus and all its Local Internal registers to their default values.

In state D_{3hot}, PCI Memory and I/O accesses are disabled, as well as PCI interrupts, and only configuration is allowed.

7.2.1 Power Management Data_Select, Data_Scale, and Power Data Utilization

The Data_Scale bits (PMCSR[14:13]) indicate the scaling factor to use when interpreting the value of the Power Management Data bits (PMDATA[7:0]). The value and meaning of the bits depend upon the data value specified in the Data_Select bits (PMCSR[12:9]). The Data_Scale bit value is unique for each Data_Select bit. For Data_Select values from 8 to 15, the Data_Scale bits always return a 0 (PMCSR[14:13]=0).

To accommodate the PCI Power Management interface to a local bus, two hidden registers (loadable by the serial EEPROM) are available to store all necessary information for the Power Management Data and Data_Scale register bits—(PMDATASEL; PCI:70h) for PMDATA[7:0] and (PMDATASCALE; PCI:74h) for PMCSR[14:13], respectively.

The PCI 9030 supports only D_0, D_{3hot}, and D_{3cold} Power Management States. Therefore, the PMDATA register, which provides operating data (such as power consumption and/or heat dissipation), retains only four possible power data combinations:

1. D_0 Power Consumed
2. D_3 Power Consumed
3. D_0 Power Dissipated
4. D_{3hot} Power Dissipated

Each power combination field requires an 8-bit register in which to store the data. The PCI 9030 provides a 32-bit hidden register, PMDATASEL, to store such information. The PMDATASEL register can be written only from the serial EEPROM and read from PMDATA[7:0], with the corresponding value in the Data_Select bits (PMCSR[12:9]).

Notes: The PCI 9030 complies with PCI Power Mgmt. r1.1; however, the version encoding in Power Management Version bits (PMC[2:0]) indicates compliance with PCI Power Mgmt. r1.0. PMC[2:0] can be programmed in serial EEPROM to the value 010 to indicate compliance with PCI Power Mgmt. r1.1. (Refer to PCI 9030 Design Notes.)

The New Capability Pointer bits (CAP_PTR[7:0]) must always contain the default value 40h. (Refer to PCI 9030 Errata #9.)

The PMDATASEL register loading sequence from the serial EEPROM is as follows:

- Bits [31:24]—Data Select for D_{3hot} Power Dissipated
- Bits [23:16]—Data Select for D_0 Power Dissipated
- Bits [15:8]—Data Select for D_{3hot} Power Consumed
- Bits [7:0]—Data Select for D_0 Power Consumed

The Data_Scale register bits (PMCSR[14:13]) that provide a scale factor value for the Data_Select value retains four possible scale factors—0, 1, 2, and 3. (Refer to *PCI Power Mgmt. r1.1* for the scale factor derivative values.) Each Data_Scale field requires a 2-bit register in which to store the data. The PCI 9030 provides an 8-bit hidden register, PMDATASCALE, to store such information. The PMDATASCALE register can be written only from the serial EEPROM and read from the PMCSR[14:13] with the corresponding Data_Select value in the Power Management Control/Status register bits (PMCSR[12:9]).

The loading sequence of the PMDATASCALE register from the serial EEPROM is as follows:

- Bits [7:6]—Data_Scale for D_{3hot} Power Dissipated
- Bits [5:4]—Data_Scale for D_0 Power Dissipated
- Bits [3:2]—Data_Scale for D_{3hot} Power Consumed
- Bits [1:0]—Data_Scale for D_0 Power Consumed

7.2.2 Reading Hidden Data Example

An example of reading hidden data follows:

1. PMCSR[12:9] Data_Select retains a value of 0h.

   PMCSR[14:13] provides a scale factor for the D_0 Power Consumed from the Data_Scale 0 bits (PMDATASCALE[1:0]).

   PMDATA[7:0] provides the D_0 Power Consumed value from the D_0 Power Consumed bits (PMDATASEL[7:0]).

2. PMCSR[12:9] Data_Select retains a value of 7h.

   PMCSR[14:13] provides a scale factor for the D_{3hot} Power Dissipated from the Data_Scale 7 bits (PMDATASCALE[7:6]).

   PMDATA[7:0] provides the D_{3hot} Power Dissipated value, from the D_3 Power Dissipated bits (PMDATASEL[31:24]).

7.3 SYSTEM CHANGES POWER MODE EXAMPLE

An example of system changes power mode follows:

1. The Host writes to the PCI 9030 PMCSR register to change the power states.

2. The PCI 9030 sends a Local Power Management Interrupt (LPMINT# output) to a Local CPU (LCPU).

3. The LCPU has 200 µs to respond to the power management information change (LPMINT#) from the PCI 9030 PMCSR register to implement the power saving function.

4. After the LCPU implements the power saving function, the PCI 9030 disables all PCI Target accesses and PCI Interrupt output (INTA#).

Notes: In Power-Saving mode, all PCI and Local Configuration cycles are granted.

The PCI 9030 automatically performs a soft reset to a Local Bus on D_3-to-D_0 transitions, then reloads the Configuration register values stored in the serial EEPROM.

7.4 WAKE-UP REQUEST EXAMPLE

An example of a wake-up request follows:

1. The add-in board (with a PCI 9030 chip installed) is in a powered-down state.

2. The Local CPU performs a LPMESET interrupt assertion (PCI 9030 PMCSR[15]) to request a wake-up procedure.

3. As soon as the request is detected, the PCI 9030 drives PME# out to the PCI Bus.

4. The PCI Host accesses the PCI 9030 PMCSR register to disable the PME# output signal and restores the PCI 9030 to the D_0 power state.

5. The PCI 9030 completes the power management task by issuing the Local Power Management Interrupt (LPMINT# output) to the Local CPU, indicating that the power mode has changed.

7—Power Management

8   COMPACTPCI HOT SWAP

The PCI 9030 is compliant with *PICMG 2.1, R2.0* requirements for Hot Swap silicon, including support for Programming Interface 0 (PI = 0), Precharge Bias Voltage, and Early Power.

8.1   OVERVIEW

Hot Swap is used for many CompactPCI applications. Hot Swap functionality allows the orderly insertion and removal of boards without adversely affecting system operation. This is done for repair of faulty boards or system reconfiguration. Additionally, Hot Swap provides access to Hot Swap services, allowing system reconfiguration and fault recovery to occur with no system down time and minimum operator interaction. Adapter insertion/removal logic control resides on the individual adapters. The PCI 9030 uses four pins—BD_SEL#, CPCISW, ENUM# and LEDon#—to implement the hardware aspects of Hot Swap functionality. The PCI 9030 uses the Hot Swap Capabilities register to implement the software aspects of Hot Swap.

The PCI 9030 supports the following features specified in the *PICMG 2.1, R2.0* requirements for Hot Swap Silicon:

- *PICMG 2.1, R2.0* compliance
- Tolerate V_{CC} from early power
- Tolerate asynchronous reset
- Tolerate precharge bias voltage
- I/O Buffers must meet modified V/I requirements
- Limited I/O pin leakage at precharge bias voltage
- **Incorporates Hot Swap Control/Status register (HS_CSR)**—Contained within the configuration space.
- **Incorporates an Extended Capability Pointer (ECP) mechanism**—It is required that Software retain a standard method of determining whether a specific function is designed in accordance with *PICMG 2.1, R2.0*. The Capabilities Pointer is located within standard CSR space, in the New Capability Functions Support bit (PCISR[4]).
- Incorporates remaining software connection control resources. Provides ENUM#, Hot Swap switch, and the blue LED.
- Early Power Support.

- **Incorporates a 1V precharge bias voltage to the PCI I/O pins**—All PCI Bus signals are required to be precharged to a 1V bias through a 10K-Ohm resistor during the Hot Swap process. The PCI 9030 provides an internal voltage regulator to supply 1V, with a built-in 10K-Ohm resistor, to all required PCI I/O buffers. Other PCI signals can be precharged to V_{IO}.

8.2   CONTROLLING CONNECTION PROCESSES

The following sections are excerpts from *PICMG 2.1, R2.0*. Refer to this specification for more details.

8.2.1   Connection Control

Hardware Control provides a means for the platform to control the hardware connection process. The signals listed in the following sections must be supported on all Hot Swap boards for interoperability. Implementations on different platforms may vary.

8.2.1.1   Board Slot Control

BD_SEL#, one of the shortest pins from the CompactPCI backplane, is driven low to enable power-on. For systems not implementing hardware control, it is grounded on the backplane.

Systems implementing hardware control radially connect BD_SEL# to a Hot Swap Controller (HSC). The controller terminates the signal with a weak pull-down, and can detect board present when the board pull-up overrides the pull-down. HSC can then control the power-on process by driving BD_SEL# low.

The PCI 9030 uses the BD_SEL# signal to three-state all local output buffers during the insertion and extraction process. In addition, the PCI 9030 uses BD_SEL# as a qualifier to dynamically connect 1V and V_{IO} precharge bias resistors to all required PCI I/O buffers. A pull-up resistor must be provided to the BD_SEL# pin or add-in card, where the pull-up resistor is connected to an Early Power power supply, which provides for proper PCI 9030 operation. (Refer to Section 11, "Pin Description," for precharge connections.)
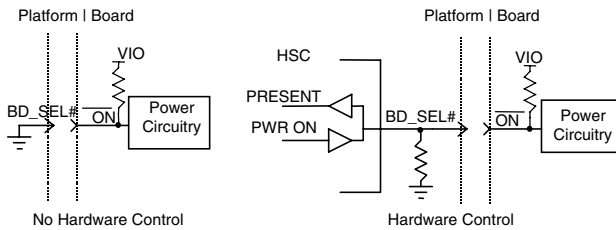
Figure 8-1. Redirection of BD_SEL#

8.2.1.2   Board Healthy

A second radial signal is used to acknowledge board health. It signals that a board is suitable to be released from reset and allowed onto the PCI Bus.

Minimally, this signal must be connected to the board's power controller "power good" status line. Use of HEALTHY# can be expanded for applications requiring additional conditions to be met for the board to be considered healthy.

On platforms that do not use Hardware Connection Control, this line is not monitored. Platforms implementing this signaling, route these signals radially to a Hot Swap Controller.
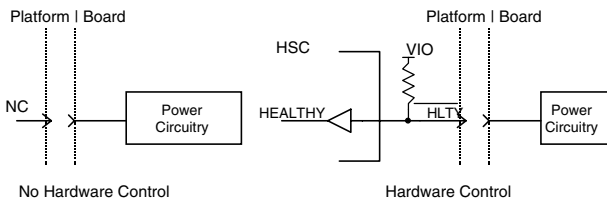
Figure 8-2. Board Healthy

8.2.1.3   Platform Reset

Reset (PCI_RST#), as defined by *PICMG 2.1, R2.0*, is a bus signal on the backplane, driven by the Host. Platforms may implement this signal as a radial signal from the Hot Swap Controller to further control the electrical connection process. Platforms that maintain function of the bus signal must *OR* the Host reset signal with the slot-specific signal.

Locally, boards must not exit reset until the H1 State is reached (healthy), and they must honor the backplane reset. The Local board reset (Local_PCI_RST#) must be the logical *OR* of these two conditions. Local_PCI_RST# is connected to the PCI 9030 RST# input pin.

During a precharge bias voltage and platform reset, in insertion and extraction procedures, all PCI I/O buffers must be in a high-impedance state. The PCI 9030 supports this condition when the Host RST# is asserted. To protect the Local board components from Early Power, the PCI 9030 floats the Local Bus I/Os. The BD_SEL# pin is used to perform the high-impedance condition on the Local Bus. With full contact of the add-in card to the backplane, BD_SEL# is asserted, which ensures that the PCI 9030 asserts the LRESETo# signal to complete a Local board reset task.
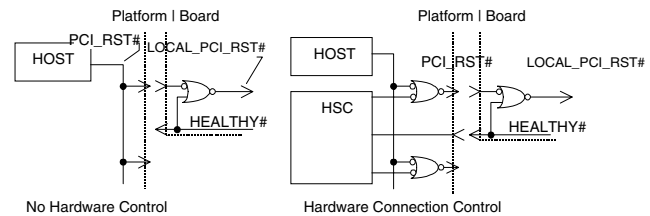
Figure 8-3. PCI Reset

8.2.2   Software Connection Control

Software Connection Control provides a means to control the Software Connection Process. Hot Swap board resources facilitate software Connection Control. Access to these resources occurs by way of the bus, using PCI protocol transfers (in-band).

These resources consist of four elements:

- ENUM# driven active indicates the need to change the Hot Swap Board state
- A switch, tied to the ejector, indicates the intent to remove a board
- LED indicates the software connection process status
- Control/Status register allows the software to interact with these resources

8.2.2.1   Ejector Switch and Blue LED

A microswitch (switch), located in the Hot Swap CompactPCI board card-ejector mechanism, is used to signal impending board removal. This signal asserts ENUM#. When the switch is activated, it is necessary to wait for the LED to turn on, indicating it is now okay to remove the board. The PCI 9030 implements separate control logic for the microswitch and blue

LED in two different pins (CPCISW and LEDon#, respectively).

When the ejector is opened or closed, the switch bounces for a time. The PCI 9030 uses internal debounce circuitry to clean the signal before the remainder of Hot Swap logic acknowledges it. The switch state is sampled six times, at 1 ms intervals, before it is determined to be closed or open.

The blue "Status" LED, located on the front of the Hot Swap CompactPCI board, is turned on when it is permissible to remove a board. The hardware connection layer provides protection for the system during all insertions and extractions. This LED indicates the system software is in a state that tolerates board extraction.

Upon insertion, the LED is automatically turned on by the hardware until the hardware connection process completes. The LED remains *OFF* until the software uses it to indicate extraction is once again permitted.

The PCI 9030 uses an open-drain output pin to sink the external LED. The LED state is driven from the LED Software On/Off Switch bit (HS_CSR[3]). LEDon# is also asserted during PCI reset (RST# asserted).

The CPCISW input signal acknowledges the state ejector handle change to identify when a board is inserted or removed. The appropriate status bits are set (HS_CSR[7:6]=1).

8.2.2.2   ENUM#

ENUM# is provided to notify the Host CPU that a board was recently inserted or is about to be removed. This signal informs the CPU that system configuration changed, at which time the CPU performs necessary maintenance such as installing a device driver upon board insertion, or quiescing a device driver prior to board extraction.

ENUM# is an open collector bused signal with a pull-up on the Host Bus. It may drive an interrupt (preferred) or be polled by the system software at regular intervals. The CompactPCI Hot-Plug system driver on the system Host manages the ENUM# sensing. Full Hot Swap boards assert ENUM# until serviced by the Hot-Plug system driver.

When a board is inserted into the system and comes out of reset, the PCI 9030 acknowledges the ejector switch state. If this switch is open (ejector handle closed), the PCI 9030 asserts the ENUM# interrupt and sets the ENUM# Status Indicator for Board Insertion bit (HS_CSR[7]). Once the Host CPU installs the proper drivers, it can logically include this board by clearing the interrupt.

When a board is about to be removed, the PCI 9030 acknowledges the ejector handle is open, asserts the ENUM# interrupt, and sets the ENUM# Status Indicator for the Board Removal bit (HS_CSR[6]). The Host then logically removes the board and turns on the LED, at which time the board can be removed from the system.

8.2.2.3   Hot Swap Control/Status Register (HS_CSR)

The PCI 9030 supports Hot Swap directly, as a control/status register in Configuration space. This register is accessed through the PCI Extended Capabilities Pointer (ECP) mechanism.

The Hot Swap Control/Status register (HS_CSR) provides status read-back for the Hot-Plug system software to determine which board is driving ENUM#. This register is also used to control the Hot Swap Status LED on the board front panel, and to de-assert ENUM#.

8—Hot Swap

8.2.2.4   Hot Swap Capabilities Register

Hot Swap ID. Bits [7:0] (HS_CNTL[7:0]; PCI:48h). These bits are set to a default value of 06h.

Next_Cap Pointer. Bits [15:8] (HS_NEXT[7:0]; PCI:49h). These bits either point to the next New Capability structure, or are set to 0h if this is the last capability in the structure. Bits [9:8] are *reserved* by *PCI r2.2*, and should be set to 00.

Control. Bits [23:16] (HS_CSR[7:0]; PCI:4Ah). This 8-bit control register is defined in Table 8-1.

31 24	23 16	15 8	7 0
Reserved	Control	Next_Cap Pointer	Hot Swap ID (06h)

Figure 8-4. Hot Swap Capabilities

Table 8-1. Hot Swap Control

Bit	Description
23	ENUM# status—Insertion (1 = board is inserted).
22	ENUM# status—Removal (1 = board is being removed).
21:20	Programming Interface 0 (PI = 0).
19	LED state (1 = LED on, 0 = LED off).
18	*Not used.*
17	ENUM# interrupt enable (1 = de-assert, 0 = enable interrupt).
16	*Not used.*

9   PCI VITAL PRODUCT DATA (VPD)

9.1   OVERVIEW

The *PCI r2.2* Vital Product Data (VPD) function defines a new location and access method. It also defines the Read Only and Read/Write bits. Currently Device ID, Vendor ID, Revision ID, Class Code, Subsystem ID, and Subsystem Vendor ID are required in the Configuration Space Header and for basic device identification and configuration. Although this information allows a device to be configured, it is not sufficient to allow a device to be uniquely identified. With the addition of VPD, optional information is provided that allows a device to be uniquely identified and tracked. These additional bits enable current and/ or future support tools and reduces the total cost of ownership of PCs and systems.

This provides an alternate access method other than Expansion ROM for VPD. VPD is stored in an external serial EEPROM, which is accessed using the Configuration Space New Capabilities function.

The VPD registers—PVPDCNTL, PVPD_NEXT, PVPDAD, and PVPDATA—are not accessible for reads from the Local Bus. The VPD function can be exercised only from the PCI Bus.

9.2   VPD CAPABILITIES REGISTER

VPD ID. Bits [7:0] (PVPDCNTL[7:0]; PCI:4Ch). The PCI SIG assigned these bits a value of 03h. The VPD ID is hardwired.

Next_Cap Pointer. Bits [15:8] (PVPD_NEXT[7:0]; PCI:4Dh). These bits either point to the next New Capability structure, or are set to 0 if this is the last capability in the structure. The PCI 9030 defaults to 0h. This value can be overwritten from the serial EEPROM. Bits [9:8] are *reserved* by *PCI r2.2* and should be set to 00.

VPD Address. Bits [24:16] (PVPDAD[14:0]; PCI:4Eh). These bits specify the Lword-aligned VPD byte address to be accessed. All accesses are 32-bit wide; bits [17:16] must be 00, with the maximum serial EEPROM size being 4K bits. Bits [30:25] are ignored.

F. Bit 31 (PVPDAD[15]; PCI:4Eh). This bit sets a flag to indicate when a serial EEPROM data operation completes. For Write cycles, the four bytes of data are first written into the VPD Data bits, after which the VPD Address is written at the same time the F flag is set to 1. The F flag clears when the serial EEPROM Data transfer completes. For Read cycles, the VPD Address is written at the same time the F flag is cleared to 0. The F flag is set when four bytes of data are read from the serial EEPROM. (Refer to *PCI 9030 Errata #1*.)

VPD Data. Bits [31:0] (PVPDATA[31:0]; PCI:50h). The PVPDATA register is not a pure read/write register. The data read from the register depends upon the last Read operation performed in PVPDAD[15]. VPD data is written or read through this register. Least-significant byte corresponding to VPD Byte at the address specified by the VPD Address register. Four bytes are always transferred between the register and the serial EEPROM.

31	30 16	15 8	7 0
F	VPD Address	Next_Cap Pointer (0h)	VPD ID (03h)
VPD Data			

Figure 9-1. VPD Capabilities

9.3   VPD SERIAL EEPROM PARTITIONING

To support VPD, the serial EEPROM is partitioned into read-only and read/write sections.

9.4   SEQUENTIAL READ ONLY

The first 1088 bits (136 bytes) of the serial EEPROM contain read-only information. The read-only portion of the serial EEPROM is loaded into the PCI 9030, using a sequential read protocol to the serial EEPROM and occurs after PCI reset. Sequential words are read by holding EECS asserted, following issuance of a serial EEPROM Read command.

9.5 RANDOM ACCESS READ AND WRITE

The PCI 9030 has full access to the read/write portion of the serial EEPROM. The serial EEPROM, starting at Lword Boundary for VPD Accesses bits (PROT_AREA[6:0]), designates this portion. This register is loaded upon power-on and can be written with a desired value, starting at location 0. This provides the capability of writing the entire serial EEPROM. Writes to the serial EEPROM are comprised of the following commands:

* Write Enable
* Write command, followed by the upper 16-bit Write data
* Write command, followed by the lower 16-bit Write data
* Write Disable

This is done to ensure against accidental write of the serial EEPROM. Randomly occurring cycles allow VPD information to be written and read at any time.

To perform a simple VPD write to the serial EEPROM, the following steps are necessary:

1. Change the write-protected serial EEPROM address in PROT_AREA[6:0], if required. 00000000h makes the serial EEPROM writable from the beginning.

2. Write the desired data into the PVPDATA register.

3. Write the destination serial EEPROM address and flag of operation to a value of 1.

4. Probe the flag of operation until it changes to a 0 to ensure the write is complete.

To perform a simple VPD read from the serial EEPROM, the following steps are necessary:

1. Write a destination serial EEPROM address and flag of operation to a value of 0.

2. Probe the flag of operation until it changes to a 1 to ensure the Read data is available.

3. Read back the PVPDATA register to see the requested data.

10   REGISTERS

10.1   NEW REGISTER DEFINITIONS SUMMARY
(AS COMPARED TO THE PCI 9050 AND PCI 9052)

Refer to the description column in the following tables for a full explanation.

Table 10-1. New Registers Definitions Summary (As Compared to the PCI 9050 and PCI 9052)

PCI Register Address	Local Offset from Base Address	Register	Bits	Description
34h	—	New Capability Pointer	7:0	Provides offset into PCI Configuration space for the location of the first item in the New Capability Linked List.
40h	—	Power Management	31:0	Provides Power Management ID, Power Management Next Capability Pointer, and Power Management Capabilities.
44h	—	Power Management	31:0	Provides Power Management Status, PMCSR Bridge Support Extensions, and Power Management Data.
48h	—	CompactPCI Hot Swap	31:0	Hot Swap Control, Hot Swap Next Capability Pointer, and Hot Swap Control/Status Register.
4Ch	—	PCI Vital Product Data	31:0	VPD ID, VPD Next Capability Pointer, and VPD Address Pointer.
50h	—	PCI Vital Product Data	31:0	VPD Data.
—	4Eh	Serial EEPROM Write-Protected Address Boundary	6:0 15:7	Serial EEPROM Write-Protected Address Boundary. ***Reserved***.
—	50h	PCI Target Response, Serial EEPROM, and Initialization Control	5:0 6 7 8 9 11:10 31	***Reserved***. PCI Target Write FIFO Full Condition. Local Arbiter LGNT Select Enable. Local Ready Timeout Enable. Local Ready Timeout Select. PCI Target Delayed Write Mode Access Select. Disconnect with Flush Read FIFO.
—	54h	General Purpose I/O Control	26:0 31:27	GPIO[8:0] Control Select bits. ***Reserved.***
—	70h	Hidden 1 Power Management Data Select	31:0	Data Select register for Power Consumed and Dissipated. Written only by the serial EEPROM.
—	74h	Hidden 2 Power Management Data Scale	7:0 31:8	Data Scale Factor Values for Power Consumed and Dissipated. Written only by the serial EEPROM. ***Reserved.***

10.2   REGISTER ADDRESS MAPPING

Table 10-2. PCI Configuration Register Address Mapping

PCI Configuration Register Address	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits.				PCI Writable	Serial EEPROM Writable
	31 30 24 23 16 15 8 7 0					
00h	Device ID		Vendor ID		N	Y
04h	Status		Command		Y	Y [20]
08h	Class Code			Revision ID	N	Y
0Ch	Built-In Self Test *(Not Supported)*	Header Type	PCI Bus Latency Timer *(Not Supported)*	Cache Line Size	Y [7:0]	N
10h	PCI Base Address 0 for Memory Accesses to Local Configuration Registers				Y	N
14h	PCI Base Address 1 for I/O Accesses to Local Configuration Registers				Y	N
18h	PCI Base Address 2 for Accesses to Local Address Space 0				Y	N
1Ch	PCI Base Address 3 for Accesses to Local Address Space 1				Y	N
20h	PCI Base Address 4 for Accesses to Local Address Space 2				Y	N
24h	PCI Base Address 5 for Accesses to Local Address Space 3				Y	N
28h	PCI Cardbus Information Structure (CIS) Pointer *(Not Supported)*				N	N
2Ch	Subsystem ID		Subsystem Vendor ID		N	Y
30h	PCI Base Address for Local Expansion ROM				Y	N
34h	*Reserved*			New_Cap Pointer	N	Y [7:0]
38h	*Reserved*				N	N
3Ch	Maximum Latency *(Not Supported)*	Minimum Grant *(Not Supported)*	Interrupt Pin	Interrupt Line	Y [7:0]	Y [15:8]
40h	Power Management Capabilities		Power Management Next_Cap Pointer	Power Management Capability ID	N	Y [30:27, 21, 19:16, 15:8]
44h	Power Management Data	PMCSR Bridge Support Extensions	Power Management Control/Status		Y [15, 12:8, 1:0]	Y [12:8]
48h	*Reserved*	Hot Swap Control/Status	Hot Swap Next_Cap Pointer	Hot Swap Capability ID	Y [23:16]	Y [15:0]
4Ch	F VPD Address		VPD Next_Cap Pointer	VPD Capability ID	Y [31:16]	Y [15:8]
50h	VPD Data				Y	N

Note: *Refer to PCI r2.2 for definitions of these registers.*

10—Registers

Table 10-3. Local Configuration Register Address Mapping

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI Writable	Serial EEPROM Writable
00h	Local Address Space 0 Range	Y	Y
04h	Local Address Space 1 Range	Y	Y
08h	Local Address Space 2 Range	Y	Y
0Ch	Local Address Space 3 Range	Y	Y
10h	Expansion ROM Range	Y	Y
14h	Local Address Space 0 Local Base Address (Remap)	Y	Y
18h	Local Address Space 1 Local Base Address (Remap)	Y	Y
1Ch	Local Address Space 2 Local Base Address (Remap)	Y	Y
20h	Local Address Space 3 Local Base Address (Remap)	Y	Y
24h	Expansion ROM Local Base Address (Remap)	Y	Y
28h	Local Address Space 0 Bus Region Descriptor	Y	Y
2Ch	Local Address Space 1 Bus Region Descriptor	Y	Y
30h	Local Address Space 2 Bus Region Descriptor	Y	Y
34h	Local Address Space 3 Bus Region Descriptor	Y	Y
38h	Expansion ROM Bus Region Descriptor	Y	Y

Table 10-4. Chip Select Register Address Mapping

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI Writable	Serial EEPROM Writable
3Ch	Chip Select 0 Base Address	Y	Y
40h	Chip Select 1 Base Address	Y	Y
44h	Chip Select 2 Base Address	Y	Y
48h	Chip Select 3 Base Address	Y	Y

Table 10-5. Control Register Address Mapping

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PCI 9030 family and to ensure compatibility with future enhancements, write 0 to all unused bits.			PCI Writable	Serial EEPROM Writable
	31 28 27 24	23 16	15 0		
4Ch	*Reserved*	Serial EEPROM Write-Protected Address Boundary	Interrupt Control/Status	Y [31:8]	Y
50h	PCI Target Response, Serial EEPROM Control, and Initialization Control			Y	Y
54h	*Reserved*	General Purpose I/O Control		Y	Y
70h	Hidden 1 Register for Power Management Data Select, Power Consumed and Dissipated Values			N	Y
74h	Hidden 2 Register for Power Management Data Scale, Power Consumed and Dissipated Values			N	Y

10.3   PCI CONFIGURATION REGISTERS

All registers may be written to or read from in Byte, Word, or Lword accesses.

Register 10-1. (PCIIDR; PCI:00h) PCI Configuration ID

Bit	Description	Read	Write	Value after Reset
15:0	**Vendor ID.** Identifies manufacturer of device. Defaults to the PCI SIG-issued Vendor ID of PLX (10B5h) if blank or if no serial EEPROM is present.	Yes	Serial EEPROM	10B5h
31:16	**Device ID.** Identifies particular device. Defaults to PLX part number for PCI interface chip (9030h) if blank or no serial EEPROM is present.	Yes	Serial EEPROM	9030h

Register 10-2. (PCICR; PCI:04h) PCI Command

Bit	Description	Read	Write	Value after Reset
0	**I/O Space.** Writing 1 allows the device to respond to I/O Space accesses. Writing 0 disables the device from responding to I/O Space accesses.	Yes	Yes	0
1	**Memory Space.** Writing 1 allows the device to respond to Memory Space accesses. Writing 0 disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	**Master Enable.** *Not Supported.*	Yes	No	0
3	**Special Cycle.** *Not Supported.*	Yes	No	0
4	**Memory Write and Invalidate Enable.** *Not Supported.*	Yes	No	0
5	**VGA Palette Snoop.** *Not Supported.*	Yes	No	0
6	**Parity Error Response.** Writing 0 indicates parity error is ignored and the operation continues. Writing 1 indicates parity checking is enabled.	Yes	Yes	0
7	**Stepping Control.** Controls whether a device does address/data stepping. Writing 0 indicates the device never does stepping. Writing 1 indicates the device always does stepping. ***Note:*** *Hardwired to 0.*	Yes	No	0
8	**SERR# Enable.** Writing 1 enables SERR# driver. Writing 0 disables SERR# driver.	Yes	Yes	0
9	**Fast Back-to-Back Enable.** Indicates what type of fast back-to-back transfers a Master can perform on the bus. Writing 1 indicates fast back-to-back transfers can occur to any agent on the bus. Writing 0 indicates fast back-to-back transfers can occur only to the same agent as in the previous cycle. ***Note:*** *Hardwired to 0.*	Yes	No	0
15:10	*Reserved*.	Yes	No	0h

Register 10-3. (PCISR; PCI:06h) PCI Status

Bit	Description	Read	Write	Value after Reset
3:0	*Reserved.*	Yes	No	0h
4	**New Capability Functions Support.** Writing 1 supports New Capabilities Functions. If enabled, the first New Capability Function ID is located at the PCI Configuration Space offset determined by the New Capabilities linked list pointer value at offset 34h. Can be written only from the serial EEPROM. Read-only from the PCI Bus.	Yes	Serial EEPROM	1
6:5	*Reserved.*	Yes	No	0
7	**Fast Back-to-Back Capable.** Writing 1 indicates an adapter can accept fast back-to-back transactions. ***Note:*** *Hardwired to 1.*	Yes	No	1
8	**Master Data Parity Error.** *Not Supported.*	Yes	No	0
10:9	**DEVSEL# Timing.** Indicates timing for DEVSEL# assertion. Writing 01 sets this bit to medium. ***Note:*** *Hardwired to 01.*	Yes	No	01
11	**Signaled Target Abort.** When set to 1, indicates the PCI 9030 signaled a Target Abort. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
12	**Received Target Abort.** When set to 1, indicates the PCI 9030 received a Target Abort signal. *Not Supported.*	Yes	No	0
13	**Received Master Abort.** When set to 1, indicates the PCI 9030 received a Master Abort signal. *Not Supported.*	Yes	No	0
14	**Signaled System Error.** When set to 1, indicates the PCI 9030 reported a system error on SERR#. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
15	**Detected Parity Error.** When set to 1, indicates the PCI 9030 detected a PCI Bus parity error, even if parity error handling is disabled [the Parity Error Response bit in the Command register is clear (PCICR[6]=0). This bit is set when the PCI 9030 detects a parity error during a PCI Address phase or a PCI Data phase when it is the Target of a write. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0

Register 10-4. (PCIREV; PCI:08h) PCI Revision ID

Bit	Description	Read	Write	Value after Reset
7:0	**Revision ID.** PCI 9030 Silicon revision.	Yes	Serial EEPROM	Current Rev #

Register 10-5. (PCICCR; PCI:09-0Bh) PCI Class Code

Bit	Description	Read	Write	Value after Reset
7:0	**Register Level Programming Interface.** None defined.	Yes	Serial EEPROM	0h
15:8	**Subclass Code (Other Bridge Device).**	Yes	Serial EEPROM	80h
23:16	**Base Class Code (Bridge Device).**	Yes	Serial EEPROM	06h

Register 10-6. (PCICLSR; PCI:0Ch) PCI Cache Line Size

Bit	Description	Read	Write	Value after Reset
7:0	**System Cache Line Size.** Specified in units of 32-bit words (8 or 16 Lwords). Can be written and read; however, the value does not affect PCI 9030 operation.	Yes	Yes	0h

Register 10-7. (PCILTR; PCI:0Dh) PCI Bus Latency Timer

Bit	Description	Read	Write	Value after Reset
7:0	**PCI Bus Latency Timer.** *Not Supported*.	Yes	No	0h

Register 10-8. (PCIHTR; PCI:0Eh) PCI Header Type

Bit	Description	Read	Write	Value after Reset
6:0	**Configuration Layout Type.** Specifies layout of registers 10h through 3Fh in configuration space. Header Type 0 is defined for all PCI devices other than PCI-to-PCI bridges (Header Type 1) and Cardbus bridges (Header Type 2).	Yes	No	0h
7	**Multi-Function Device.** Value of 1 indicates multiple (up to eight) functions (logical devices) each containing its own, individually addressable configuration space, 64 Lwords in size. ***Note:*** *Hardwired to 0 (that is, device is single function, as multi-function = false).*	Yes	No	0

Register 10-9. (PCIBISTR; PCI:0Fh) PCI Built-In Self Test (BIST)

Bit	Description	Read	Write	Value after Reset
7:0	**Built-In Self Test.** Value of 0 indicates device passed its test. ***Not Supported***.	Yes	No	0h

Register 10-10. (PCIBAR0; PCI:10h) PCI Base Address 0 for Memory Accesses to Local Configuration Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. ***Note:*** *Hardwired to 0.*	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit Memory Address space 11 = **Reserved** ***Note:*** *Hardwired to 00.*	Yes	No	00
3	**Prefetchable.** Writing 1 indicates there are no side effects on reads. Does not affect PCI 9030 operation. ***Note:*** *Hardwired to 0.*	Yes	No	0
6:4	**Memory Base Address.** Memory base address for access to Local Configuration registers (requires 128 bytes). ***Note:*** *Hardwired to 000.*	Yes	No	000
31:7	**Memory Base Address.** Memory base address for access to Local Configuration registers.	Yes	Yes	0h

Note: *PCIBAR0 can be enabled or disabled by using CNTRL[13:12].*

Register 10-11. (PCIBAR1; PCI:14h) PCI Base Address 1 for I/O Accesses to Local Configuration Registers

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. ***Note:*** *Hardwired to 1.*	Yes	No	1
1	***Reserved.***	Yes	No	0
6:2	**I/O Base Address.** Base Address for I/O access to Local Configuration registers (requires 128 bytes). ***Note:*** *Hardwired to 0h.*	Yes	No	0h
31:7	**I/O Base Address.** Base Address for I/O access to Local Configuration registers.	Yes	Yes	0h

Note: *PCIBAR1 can be enabled or disabled by using CNTRL[13:12].*

Register 10-12. (PCIBAR2; PCI:18h) PCI Base Address 2 for Accesses to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Specified in the LAS0RR register.)	Yes	No	0
2:1	**Register Location (If Memory Space).** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit Memory Address space 11 = **Reserved** (Specified in the LAS0RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Writing 1 indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect PCI 9030 operation. The associated Bus Region Descriptor register (LAS0BRD) controls prefetching functions of this address space. (Specified in the LAS0RR register.) If I/O Space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 0.	Yes	Yes	0h

Note: *If allocated, Local Address Space 0 can be enabled*
or disabled by setting or clearing LAS0BA[0].

Register 10-13. (PCIBAR3; PCI:1Ch) PCI Base Address 3 for Accesses to Local Address Space 1

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Specified in the LAS1RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit Memory Address space 11 = **Reserved** (Specified in the LAS1RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Writing 1 indicates there are no side effects on reads. Reflects value of LAS1RR[3] and provides only status to the system. Does not affect PCI 9030 operation. The associated Bus Region Descriptor register (LAS1BRD) controls prefetching functions of this address space. (Specified in the LAS1RR register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 1.	Yes	Yes	0h

Note: *If allocated, Local Address Space 1 can be enabled*
or disabled by setting or clearing LAS1BA[0].

Register 10-14. (PCIBAR4; PCI:20h) PCI Base Address 4 for Accesses to Local Address Space 2

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Specified in the LAS2RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit Memory Address space 11 = **Reserved** (Specified in the LAS2RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Writing 1 indicates there are no side effects on reads. Reflects value of LAS2RR[3] and provides only status to the system. Does not affect PCI 9030 operation. The associated Bus Region Descriptor register (LAS2BRD) controls prefetching functions of this address space. (Specified in the LAS2RR register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 2.	Yes	Yes	0h

Note: *If allocated, Local Address Space 2 can be enabled
or disabled by setting or clearing LAS2BA[0].*

Register 10-15. (PCIBAR5; PCI:24h) PCI Base Address 5 for Accesses to Local Address Space 3

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Specified in the LAS3RR register.)	Yes	No	0
2:1	**Register Location**. Values: 00 = Locate anywhere in 32-bit Memory Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit Memory Address space 11 = **Reserved** (Specified in the LAS3RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	**Prefetchable (If Memory Space).** Writing 1 indicates there are no side effects on reads. Reflects value of LAS3RR[3] and provides only status to the system. Does not affect PCI 9030 operation. The associated Bus Region Descriptor register (LAS3BRD) controls prefetching functions of this address space. (Specified in the LAS3RR register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address.** Memory base address for access to Local Address Space 3.	Yes	Yes	0h

Note: *If allocated, Local Address Space 3 can be enabled
or disabled by setting or clearing LAS3BA[0].*

Register 10-16. (PCICIS; PCI:28h) PCI Cardbus Information Structure Pointer

Bit	Description	Read	Write	Value after Reset
31:0	**Cardbus Information Structure (CIS) Pointer for PC Cards.** *Not Supported.*	Yes	No	0h

Register 10-17. (PCISVID; PCI:2Ch) PCI Subsystem Vendor ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem Vendor ID (Unique Add-in Board Vendor ID).**	Yes	Serial EEPROM	0h

Register 10-18. (PCISID; PCI:2Eh) PCI Subsystem ID

Bit	Description	Read	Write	Value after Reset
15:0	**Subsystem ID (Unique Add-in Board Device ID).**	Yes	Serial EEPROM	0h

Register 10-19. (PCIERBAR; PCI:30h) PCI Expansion ROM Base Address

Bit	Description	Read	Write	Value after Reset
0	**Address Decode Enable.** Writing 1 indicates a device accepts accesses to the Expansion ROM address. Writing 0 indicates a device does not accept accesses to Expansion ROM address. Should be set to 0 if there is no Expansion ROM. Works in conjunction with EROMRR[0].	Yes	Yes	0
10:1	*Reserved*.	Yes	No	0h
31:11	**Expansion ROM Base Address (upper 21 bits).**	Yes	Yes	0h

Register 10-20. (CAP_PTR; PCI:34h) New Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**New Capability Pointer.** Provides an offset into PCI Configuration Space for location of the first item in the New Capabilities Linked List. Bits [1:0] are **reserved** by *PCI r2.2*, and should be set to 00 (the byte value points to an Lword boundary.) **Note:** *These bits must always contain the default value 40h. (Refer to PCI 9030 Errata #9.)*	Yes	Serial EEPROM	40h
31:8	*Reserved.*	Yes	No	0h

Register 10-21. (PCIILR; PCI:3Ch) PCI Interrupt Line

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Line Routing Value.** Indicates to which system interrupt controller(s) input the interrupt line is connected. The PCI 9030 does not use this value, rather the value is used by device drivers and operating systems for priority and vector information. Values in this register are system-architecture specific. For x86-based PCs, the values in this register correspond to IRQ numbers (0 through 15) of the standard dual 8259 interrupt controller configuration. The value 255 is defined as "unknown" or "no connection" to the interrupt controller. Values 15 through 255 are ***reserved***.	Yes	Yes	0h

Register 10-22. (PCIIPR; PCI:3Dh) PCI Interrupt Pin

Bit	Description	Read	Write	Value after Reset
7:0	**Interrupt Pin Register.** Indicates which interrupt pin the device uses. The following values are decoded: 0h = No Interrupt Pin 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# The PCI 9030 supports only INTA#. Because PCIHTR[7]=0, values 2h, 3h, and 4h have no meaning. All other values (05h–FFh) are ***reserved*** by *PCI r2.2*.	Yes	Serial EEPROM	1h

Register 10-23. (PCIMGR; PCI:3Eh) PCI Minimum Grant

Bit	Description	Read	Write	Value after Reset
7:0	**Min_Gnt.** Specifies the length required for a Burst period device, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 μs increments. ***Not Supported.***	Yes	No	0h

Register 10-24. (PCIMLR; PCI:3Fh) PCI Maximum Latency

Bit	Description	Read	Write	Value after Reset
7:0	**Max_Lat.** Specifies how often the device must gain access to the PCI Bus. Value is a multiple of 1/4 μs increments. ***Not Supported.***	Yes	No	0h

Register 10-25. (PMCAPID; PCI:40h) Power Management Capability ID

Bit	Description	Read	Write	Value after Reset
7:0	**Power Management Capability ID.**	Yes	No	1h

Register 10-26. (PMNEXT; PCI:41h) Power Management Next Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**Next_Cap Pointer.** Provides an offset into PCI Configuration space for location of the next item in the New Capabilities Linked List. Bits [1:0] are *reserved* by *PCI r2.2*, and should be set to 00 (the byte value points to an Lword boundary). If Power Management is the last capability in the list, set to 0h.	Yes	Serial EEPROM	48h

Register 10-27. (PMC; PCI:42h) Power Management Capabilities

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** The value 001 indicates compliance with *PCI Bus Power Management Interface Specification, Revision 1.0*, and its definition for PMC register format. This value can be changed in serial EEPROM to 010 to indicate compliance with *PCI Power Mgmt. r1.1*. (Refer to *PCI 9030 Design Note #1* for PMC register definition under *PCI Power Mgmt. r1.1*.)	Yes	Serial EEPROM	001
3	**PCI Clock Required for PME# Signal.** When set to 1, indicates a function relies on PCI clock presence for PME# operation. The PCI 9030 does not require the PCI clock for PME#, so this bit should be set to 0 in serial EEPROM.	Yes	Serial EEPROM	0
4	**Auxiliary Power Source.** Because the PCI 9030 does not support PME# while in a D_{3cold} state, this bit is always set to 0. ***Not Supported.***	Yes	No	0
5	**Device-Specific Initialization (DSI).** When set to 1, the PCI 9030 requires special initialization following a transition to a D_0 uninitialized state before a generic class device driver is able to use it.	Yes	Serial EEPROM	0
8:6	*Reserved.*	Yes	No	000
9	**D_1_Support.** When set to 1, the PCI 9030 supports the D_1 power state. ***Not Supported.***	Yes	No	0
10	**D_2_Support.** When set to 1, the PCI 9030 supports the D_2 power state. ***Not Supported.***	Yes	No	0
15:11	**PME_Support.** Indicates power states in which the PCI 9030 may assert PME#. Values: XXXX1 = PME# can be asserted from D_0 XXXXX = The PCI 9030 does not support the D_1 power state XXXXX = The PCI 9030 does not support the D_2 power state X1XXX = PME# can be asserted from D_{3hot} XXXXX = PME# cannot be asserted from D_{3cold}	Yes	[14:11]: Serial EEPROM [15]: No	01001

Register 10-28. (PMCSR; PCI:44h) Power Management Control/Status

Bit	Description	Read	Write	Value after Reset
1:0	**Power State.** Determines or changes the current power state. Values: 00 = D_0 11 = D_{3hot} Transition from a D_{3hot} state to a D_0 state causes a soft reset, LRESETo# assertion, an LPMINT# pulse, clearing of Local Configuration registers (including the Chip Select and Control registers), and reloading of the Configuration registers from the serial EEPROM. In a D_{3hot} state, PCI Memory and I/O accesses are disabled, as well as PCI interrupts, and only configuration is allowed.	Yes	Yes	00
7:2	*Reserved.*	Yes	No	0h
8	**PME_En.** Writing 1 enables PME# to be asserted.	Yes	Yes/ Serial EEPROM	0
12:9	**Data_Select.** Selects which data to report through the Data register and Data_Scale bits.	Yes	Yes/ Serial EEPROM	0h
14:13	**Data_Scale.** Indicates the scaling factor to use when interpreting the Data register value. Value and meaning of this bit depends on the data value selected by the Data_Select bit. When the Local CPU initializes the Data_Scale values, it must use the Data_Select bit to determine which Data_Scale value it is writing. For Power Consumed and Power Dissipated data, the following scale factors are used. Unit values are in watts. Values: 0 = Unknown 1 = 0.1x 2 = 0.01x 3 = 0.001x *Note:* Information regarding hidden register use is provided in Section 7.2.1.	Yes	Serial EEPROM by way of PMDATASCALE	00
15	**PME_Status.** Indicates PME# is being driven if the PME_En bit is set (PMCSR[8]=1). Asserting LPMESET input high sets this bit; writing 1 from the PCI Bus clears this bit to 0. Depending on the current power state, set only if the appropriate PME_Support bit(s) is set (*for example*, PMC[15:11]=1).	Yes	Local Interrupt/Set, PCI/Clr	0

Register 10-29. (PMCSR_BSE; PCI:46h) PMCSR Bridge Support Extensions

Bit	Description	Read	Write	Value after Reset
7:0	*Reserved.*	Yes	No	0h

Register 10-30. (PMDATA; PCI:47h) Power Management Data

Bit	Description	Read	Write	Value after Reset
7:0	**Power Management Data.** Provides operating data, such as power consumed or heat dissipation. Data returned is selected by the Data_Select bit(s) (PMCSR[12:9]) and scaled by the Data_Scale bit(s) (PMCSR[14:13]). Data Select values: 0 = D_0 Power Consumed 1 = *Reserved* 2 = *Reserved* 3 = D_3 Power Consumed 4 = D_0 Power Dissipated 5 = *Reserved* 6 = *Reserved* 7 = D_{3hot} Power Dissipated ***Note:*** *Information regarding hidden register use is provided in Section 7.2.1.*	Yes	Serial EEPROM by way of PMDATASEL	0h

Register 10-31. (HS_CNTL; PCI:48h) Hot Swap Control

Bit	Description	Read	Write	Value after Reset
7:0	**Hot Swap ID.** Capability ID = 06h for Hot Swap.	Yes	Serial EEPROM	06h

Register 10-32. (HS_NEXT; PCI:49h) Hot Swap Next Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**Next_Cap Pointer.** Provides an offset into PCI Configuration space for location of the next item in the New Capabilities Linked List. Bits [1:0] are ***reserved*** by *PCI r2.2*, and should be set to 00 (the byte value points to an Lword boundary). If Hot Swap is the last capability in the list, set to 0h.	Yes	Serial EEPROM	4Ch

Register 10-33. (HS_CSR; PCI:4Ah) Hot Swap Control/Status

Bit	Description	Read	Write	Value after Reset
0	*Reserved.*	Yes	No	0
1	**ENUM# Interrupt Mask (EIM).** Writing 0 enables the interrupt. Writing 1 masks the interrupt.	Yes	PCI	0
2	*Reserved.*	Yes	No	0
3	**LED Software On/Off Switch.** Writing 1 turns on the LED. Writing 0 turns off the LED.	Yes	PCI	0
5:4	**Programming Interface 0 (PI = 0).**	Yes	No	00
6	**ENUM# Status Indicator for Board Removal.** Value of 1 reports the ENUM# assertion for removal process. Writing 1 clears the ENUM# Interrupt and Status bit.	Yes	PCI/Clr	0
7	**ENUM# Status Indicator for Board Insertion.** Value of 1 reports the ENUM# assertion for the insertion process. Writing 1 clears the ENUM# Interrupt and Status bit.	Yes	PCI/Clr	0
15:8	*Reserved.*	Yes	No	0h

Register 10-34. (PVPDCNTL; PCI:4Ch) PCI Vital Product Data Control

Bit	Description	Read	Write	Value after Reset
7:0	**VPD ID.** Capability ID = 03h for VPD.	PCI	No	03h

Register 10-35. (PVPD_NEXT; PCI:4Dh) PCI Vital Product Data Next Capability Pointer

Bit	Description	Read	Write	Value after Reset
7:0	**Next_Cap Pointer.** Provides an offset into PCI Configuration space for location of the next item in the New Capabilities Linked List. Bits [1:0] are **reserved** by *PCI r2.2*, and should be set to 00 (the byte value points to an Lword boundary). Because VPD is the last capability in the list, set to 0h.	PCI	Serial EEPROM	0h

Register 10-36. (PVPDAD; PCI:4Eh) PCI Vital Product Data Address

Bit	Description	Read	Write	Value after Reset
14:0	**VPD Address.** Lword-aligned Byte address of the VPD address to be accessed. All accesses are 32-bit wide; bits [1:0] must be 00, with the maximum serial EEPROM size being 4K bits (supports 2K or 4K bit serial EEPROM). Bits [14:9] are ignored.	PCI	Yes	0h
15	**F.** Flag used to indicate when the data transfer between PVPDATA and the storage component completes. Writing 0 along with the VPD address causes a read of VPD information into PVPDATA. The hardware sets this bit to 1 when the VPD Data transfer completes. Writing 1 along with the VPD address causes a write of VPD information from PVPDATA into a storage component. The hardware sets this bit to 0 after the Write operation completes. (Refer to *PCI 9030 Errata #1*.)	PCI	Yes	0

Register 10-37. (PVPDATA; PCI:50h) PCI VPD Data

Bit	Description	Read	Write	Value after Reset
31:0	**VPD Data Register.**	PCI	Yes	0h

10.4   LOCAL CONFIGURATION REGISTERS

Register 10-38. (LAS0RR; 00h) Local Address Space 0 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates Local Address Space 0 maps into PCI Memory space. Writing 1 indicates Local Address Space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit PCI Address space 11 = **Reserved** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 0. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR2). Default is 1 MB. ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.* *User should limit each I/O-mapped space to 256 bytes per PCI r2.2.*	Yes	Yes	FF0000h
31:28	**Reserved.** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-39. (LAS1RR; 04h) Local Address Space 1 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates Local Address Space 1 maps into PCI Memory space. Writing 1 indicates Local Address Space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit PCI Address space 11 = **Reserved** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 1. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR3). ***Notes:*** *Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range.* *User should limit each I/O-mapped space to 256 bytes per PCI r2.2.*	Yes	Yes	0h
31:28	**Reserved.** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-40. (LAS2RR; 08h) Local Address Space 2 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates Local Address Space 2 maps into PCI Memory space. Writing 1 indicates Local Address Space 2 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit PCI Address space 11 = **Reserved** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 2. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR4). **Notes:** Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range. User should limit each I/O-mapped space to 256 bytes per PCI r2.2.	Yes	Yes	0h
31:28	**Reserved.** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-41. (LAS3RR; 0Ch) Local Address Space 3 Range

Bit	Description	Read	Write	Value after Reset
0	**Memory Space Indicator.** Writing 0 indicates Local Address Space 3 maps into PCI Memory space. Writing 1 indicates Local Address Space 3 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 00 = Locate anywhere in 32-bit PCI Address space 01 = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, **Reserved** 10 = Locate anywhere in 64-bit PCI Address space 11 = **Reserved** When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [27:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing 1 indicates reads are prefetchable (does not affect PCI 9030 operation, but is used for system status). When mapped into I/O space, it is included with bits [27:2] to indicate the decoding range.	Yes	Yes	0
27:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 3. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIBAR5). **Notes:** Range (**not** Range register) must be power of 2. "Range register value" is two's complement of range. User should limit each I/O-mapped space to 256 bytes per PCI r2.2.	Yes	Yes	0h
31:28	**Reserved.** (PCI Address bits [31:28] are always included in decoding.)	Yes	No	0h

Register 10-42. (EROMRR; 10h) Expansion ROM Range

Bit	Description	Read	Write	Value after Reset
0	**Address Decode Enable.** Bit 0 can only be enabled from the serial EEPROM. To disable, set the PCI Expansion ROM Address Decode Enable bit to 0 (PCIERBAR[0]=0).	Yes	Serial EEPROM Only	0
10:1	*Reserved.*	Yes	No	0h
27:11	Specifies which PCI Address bits to use for decoding a PCI-to-Local Bus Expansion ROM. Each bit corresponds to a PCI Address bit. Bit 27 corresponds to address bit 27. Write 1 to all bits that are to be included in decode and 0 to all others (used in conjunction with PCIERBAR). Default is 64 KB; minimum range, if enabled, is 2 KB, and maximum range allowed by *PCI r2.2* is 16 MB. **Note:** *Range (not Range register) must be power of 2. "Range register value" is two's complement of range.* EROMRR should normally be programmed by way of the serial EEPROM to a value of 0h, unless Expansion ROM is present on the Local Bus. If the value is not 0h (default value is 64 KB), system BIOS may attempt to allocate Expansion ROM address space and th*en access it at the local base address specified in EROMBA (default value is 1 MB) to determine whether the Expansion ROM image is valid. If the image is not valid, as defined in Section 6.3.1.1 (PCI Expansion ROM Header Format) of PCI r2.2, the system BIOS unmaps the Expansion ROM address space it initially allocated, by writing 0h to PCIERBAR[31:0].*	Yes	Yes	1111111111110 0000
31:28	*Reserved.* (PCI Address bits [31:28] are always included in decoding.)	Yes	Yes	1111

Register 10-43. (LAS0BA; 14h) Local Address Space 0 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 0 Enable.** Writing 1 enables decoding of PCI addresses for PCI Target access to Local Address Space 0. Writing 0 disables decoding.	Yes	Yes	1
1	***Reserved.***	Yes	No	0
3:2	If Local Address Space 0 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCIBAR2 Base Address to Local Address Space 0 Base Address.** The PCIBAR2 base address translates to the Local Address Space 0 Base Address programmed in this register. A PCI Target access to an offset from PCIBAR2 maps to the same offset from this Local Base Address. ***Notes:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local Address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-44. (LAS1BA; 18h) Local Address Space 1 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 1 Enable.** Writing 1 enables decoding of PCI addresses for PCI Target access to Local Address Space 1. Writing 0 disables decoding. PCIBAR3 can be enabled or disabled by setting or clearing this bit.	Yes	Yes	0
1	***Reserved.***	Yes	No	0
3:2	If Local Address Space 1 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCIBAR3 Base Address to Local Address Space 1 Base Address.** The PCIBAR3 base address translates to the Local Address Space 1 Base Address programmed in this register. A PCI Target access to an offset from PCIBAR3 maps to the same offset from this Local Base Address. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	***Reserved.*** (Local Address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-45. (LAS2BA; 1Ch) Local Address Space 2 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 2 Enable.** Writing 1 enables decoding of PCI addresses for PCI Target access to Local Address Space 2. Writing 0 disables decoding. PCIBAR4 can be enabled or disabled by setting or clearing this bit.	Yes	Yes	0
1	*Reserved.*	Yes	No	0
3:2	If Local Address Space 2 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCIBAR4 Base Address to Local Address Space 2 Base Address.** The PCIBAR4 base address translates to the Local Address Space 2 Base Address programmed in this register. A PCI Target access to an offset from PCIBAR4 maps to the same offset from this Local Base Address. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	*Reserved.* (Local Address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-46. (LAS3BA; 20h) Local Address Space 3 Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
0	**Space 3 Enable.** Writing 1 enables decoding of PCI addresses for PCI Target access to Local Address Space 3. Writing 0 disables decoding. PCIBAR5 can be enabled or disabled by setting or clearing this bit.	Yes	Yes	0
1	*Reserved.*	Yes	No	0
3:2	If Local Address Space 3 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [27:4] for remapping.	Yes	Yes	00
27:4	**Remap PCIBAR5 Base Address to Local Address Space 3 Base Address.** The PCIBAR5 base address translates to the Local Address Space 3 Base Address programmed in this register. A PCI Target access to an offset from PCIBAR5 maps to the same offset from this Local Base Address. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0h
31:28	*Reserved.* (Local Address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-47. (EROMBA; 24h) Expansion ROM Local Base Address (Remap)

Bit	Description	Read	Write	Value after Reset
10:0	*Reserved.*	Yes	No	0h
27:11	**Remap PCI Expansion ROM Space into Local Address Space.** Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a Range multiple (**not** the Range register).*	Yes	Yes	0000000100000 0000
31:28	*Reserved.* (Local Address bits [31:28] do not exist in the PCI 9030.)	Yes	No	0h

Register 10-48. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Local Address Space 0 Burst Enable.** Writing 1 enables bursting. Writing 0 disables bursting. If burst is disabled, the Local Bus performs continuous single cycles for Burst PCI Read/Write cycles. PCI reads are completed as single cycle on the PCI Bus if Local burst is disabled or prefetch is disabled (bits [5:3]=100).	Yes	Yes	0
1	**Local Address Space 0 READY# Input Enable.** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes	0
2	**Local Address Space 0 BTERM# Input Enable.** Writing 1 enables BTERM# input. Writing 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (Prefetch Counter enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and the Prefetch Count is not 00, the PCI 9030 prefetches up to the number of Lwords specified in the Prefetch Count. When set to 0, the PCI 9030 ignores the count and continues prefetching, until terminated by PCI Bus transaction completion if Read Ahead mode is disabled (CNTRL[16]=0), or if Read Ahead mode is enabled, until the Read FIFO fills. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (bits [5:3]=100).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	00000
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD/LD Bus Write data is not valid during NXDA wait states. (Wait states between consecutive bus requests. NXDA wait states are inserted only after the last Data transfer of a PCI Target access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD/LD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	00000
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Local Address Space 0 Local Bus Width.** Writing of the following values indicates the associated bus width: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = *Reserved*	Yes	Yes	10

Register 10-48. (LAS0BRD; 28h) Local Address Space 0 Bus Region Descriptor (Continued)

Bit	Description	Read	Write	Value after Reset
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing 1 specifies that in Big Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing 0 specifies that in Big Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD/LD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Register 10-49. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Local Address Space 1 Burst Enable.** Writing 1 enables bursting. Writing 0 disables bursting. If burst is disabled, the Local Bus performs continuous single cycles for Burst PCI Read/Write cycles. PCI reads are completed as single cycle on the PCI Bus if Local burst is disabled or prefetch is disabled (bits [5:3]=100).	Yes	Yes	0
1	**Local Address Space 1 READY# Input Enable.** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes	0
2	**Local Address Space 1 BTERM# Input Enable.** Writing 1 enables BTERM# input. Writing 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (Prefetch Counter enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and the Prefetch Count is not 00, the PCI 9030 prefetches up to the number of Lwords specified in the Prefetch Count. When set to 0, the PCI 9030 ignores the count and continues prefetching, until terminated by PCI Bus transaction completion if Read Ahead mode is disabled (CNTRL[16]=0), or if Read Ahead mode is enabled, until the Read FIFO fills. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (bits [5:3]=100).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	00000
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD/LD Bus Write data is not valid during NXDA wait states. (Wait states between consecutive bus requests. NXDA wait states are inserted only after the last Data transfer of a PCI Target access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD/LD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	00000
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Local Address Space 1 Local Bus Width.** Writing of the following values indicates the associated bus width: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = *Reserved*	Yes	Yes	10

Register 10-49. (LAS1BRD; 2Ch) Local Address Space 1 Bus Region Descriptor (Continued)

Bit	Description	Read	Write	Value after Reset
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing 1 specifies that in Big Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing 0 specifies that in Big Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD/LD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Register 10-50. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Local Address Space 2 Burst Enable.** Writing 1 enables bursting. Writing 0 disables bursting. If burst is disabled, the Local Bus performs continuous single cycles for Burst PCI Read/Write cycles. PCI reads are completed as single cycle on the PCI Bus if Local burst is disabled or prefetch is disabled (bits [5:3]=100).	Yes	Yes	0
1	**Local Address Space 2 READY# Input Enable.** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes	0
2	**Local Address Space 2 BTERM# Input Enable.** Writing 1 enables BTERM# input. Writing 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (Prefetch Counter enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and the Prefetch Count is not 00, the PCI 9030 prefetches up to the number of Lwords specified in the Prefetch Count. When set to 0, the PCI 9030 ignores the count and continues prefetching, until terminated by PCI Bus transaction completion if Read Ahead mode is disabled (CNTRL[16]=0), or if Read Ahead mode is enabled, until the Read FIFO fills. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (bits [5:3]=100).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	00000
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD/LD Bus Write data is not valid during NXDA wait states. (Wait states between consecutive bus requests. NXDA wait states are inserted only after the last Data transfer of a PCI Target access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD/LD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	00000
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Local Address Space 2 Local Bus Width.** Writing of the following values indicates the associated bus width: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = *Reserved*	Yes	Yes	10

Register 10-50. (LAS2BRD; 30h) Local Address Space 2 Bus Region Descriptor (Continued)

Bit	Description	Read	Write	Value after Reset
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing 1 specifies that in Big Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing 0 specifies that in Big Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD/LD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Register 10-51. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Local Address Space 3 Burst Enable.** Writing 1 enables bursting. Writing 0 disables bursting. If burst is disabled, the Local Bus performs continuous single cycles for Burst PCI Read/Write cycles. PCI reads are completed as single cycle on the PCI Bus if Local burst is disabled or prefetch is disabled (bits [5:3]=100).	Yes	Yes	0
1	**Local Address Space 3 READY# Input Enable.** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes	0
2	**Local Address Space 3 BTERM# Input Enable.** Writing 1 enables BTERM# input. Writing 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (Prefetch Counter enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and the Prefetch Count is not 00, the PCI 9030 prefetches up to the number of Lwords specified in the Prefetch Count. When set to 0, the PCI 9030 ignores the count and continues prefetching, until terminated by PCI Bus transaction completion if Read Ahead mode is disabled (CNTRL[16]=0), or if Read Ahead mode is enabled, until the Read FIFO fills. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (bits [5:3]=100).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	00000
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD/LD Bus Write data is not valid during NXDA wait states. (Wait states between consecutive bus requests. NXDA wait states are inserted only after the last Data transfer of a PCI Target access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD/LD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	00000
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Local Address Space 3 Local Bus Width.** Writing of the following values indicates the associated bus width: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = **Reserved**	Yes	Yes	10

Register 10-51. (LAS3BRD; 34h) Local Address Space 3 Bus Region Descriptor (Continued)

Bit	Description	Read	Write	Value after Reset
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing 1 specifies that in Big Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing 0 specifies that in Big Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD/LD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

Register 10-52. (EROMBRD; 38h) Expansion ROM Bus Region Descriptor

Bit	Description	Read	Write	Value after Reset
0	**Expansion ROM Burst Enable.** Writing 1 enables bursting. Writing 0 disables bursting. If burst is disabled, the Local Bus performs continuous single cycles for Burst PCI Read/Write cycles. PCI reads are completed as single cycle on the PCI Bus if Local burst is disabled or prefetch is disabled (bits [5:3]=100).	Yes	Yes	0
1	**Expansion ROM Space READY# Input Enable.** Writing 1 enables READY# input. Writing 0 disables READY# input.	Yes	Yes	0
2	**Expansion ROM Space BTERM# Input Enable.** Writing 1 enables BTERM# input. Writing 0 disables BTERM# input. For more information, refer to Section 2.2.4.3.	Yes	Yes	0
4:3	**Prefetch Count.** Number of Lwords to prefetch during Memory Read cycle. Used only if bit 5 is high (Prefetch Counter enabled). Values: 00 = Do not prefetch. Only read bytes specified by C/BE lines. 01 = Prefetch four Lwords if bit 5 is set. 10 = Prefetch eight Lwords if bit 5 is set. 11 = Prefetch 16 Lwords if bit 5 is set.	Yes	Yes	00
5	**Prefetch Counter Enable.** When set to 1 and the Prefetch Count is not 00, the PCI 9030 prefetches up to the number of Lwords specified in the Prefetch Count. When set to 0, the PCI 9030 ignores the count and continues prefetching, until terminated by PCI Bus transaction completion if Read Ahead mode is disabled (CNTRL[16]=0), or if Read Ahead mode is enabled, until the Read FIFO fills. To disable prefetch, enable the Prefetch Counter and set the prefetch count to 0 (bits [5:3]=100).	Yes	Yes	0
10:6	**NRAD Wait States.** Number of Read Address-to-Data wait states (0-31). (Wait states between the Address cycle and first Read Data cycle.)	Yes	Yes	00000
12:11	**NRDD Wait States.** Number of Read Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst read.)	Yes	Yes	00
14:13	**NXDA Wait States.** Number of Read/Write Data-to-Address wait states (0-3). LAD/LD Bus Write data is not valid during NXDA wait states. (Wait states between consecutive bus requests. NXDA wait states are inserted only after the last Data transfer of a PCI Target access.)	Yes	Yes	00
19:15	**NWAD Wait States.** Number of Write Address-to-Data wait states (0-31). LAD/LD Bus data is valid during NWAD wait states. (Wait states between the Address cycle and first Write Data cycle.)	Yes	Yes	00000
21:20	**NWDD Wait States.** Number of Write Data-to-Data wait states (0-3). (Wait states between consecutive Data cycles of a Burst write.)	Yes	Yes	00
23:22	**Expansion ROM Local Bus Width.** Writing of the following values indicates the associated bus width: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = **Reserved**	Yes	Yes	00

Register 10-52. (EROMBRD; 38h) Expansion ROM Bus Region Descriptor (Continued)

Bit	Description	Read	Write	Value after Reset
24	**Byte Ordering.** Value of 1 indicates Big Endian. Value of 0 indicates Little Endian.	Yes	Yes	0
25	**Big Endian Byte Lane Mode.** Writing 1 specifies that in Big Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing 0 specifies that in Big Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
27:26	**Read Strobe Delay.** Number of clocks from beginning of cycle until RD# strobe is asserted (0-3). Value must be ≤ NRAD for RD# to be asserted.	Yes	Yes	00
29:28	**Write Strobe Delay.** Number of clocks from beginning of cycle until WR# strobe is asserted (0-3). Value must be ≤ NWAD for WR# to be asserted.	Yes	Yes	00
31:30	**Write Cycle Hold.** Number of clocks from WR# de-assertion until end of cycle (0-3). Data (LAD/LD[31:0]) remains valid, and BLAST# remains asserted, during Write Cycle Hold bus cycles.	Yes	Yes	00

10.5   CHIP SELECT REGISTERS

Register 10-53. (CS0BASE; 3Ch) Chip Select 0 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 0 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 0.** Write zeros (0) in the least significant bits to define the range for Chip Select 0. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	*Reserved.*	Yes	No	0h

Note: *For a chip select to assert, the address must be encompassed within a Local Address Space.*

Register 10-54. (CS1BASE; 40h) Chip Select 1 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 1 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 1.** Write zeros (0) in the least significant bits to define the range for Chip Select 1. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	*Reserved.*	Yes	No	0h

Note: *For a chip select to assert, the address must be encompassed within a Local Address Space.*

Register 10-55. (CS2BASE; 44h) Chip Select 2 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 2 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 2.** Write zeros (0) in the least significant bits to define the range for Chip Select 2. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define the base address.	Yes	Yes	0h
31:28	*Reserved.*	Yes	No	0h

Notes: *Chip Select 2 (CS2#) functionality of the GPIO2/CS2#*
multiplexed pin is enabled by configuring GPIOC[6] from the default
value of 0 (GPIO2) to 1.

For a chip select to assert, the address must be encompassed
within a Local Address Space.

Register 10-56. (CS3BASE; 48h) Chip Select 3 Base Address

Bit	Description	Read	Write	Value after Reset
0	**Chip Select 3 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
27:1	**Local Base Address of Chip Select 3.** Write zeros (0) in the least significant bits to define the range for Chip Select 3. Starting from bit 1 and scanning toward bit 27, the first "1" found defines size. The remaining most significant bits, excluding the first "1" found, define base address.	Yes	Yes	0h
31:28	*Reserved.*	Yes	No	0h

Notes: *Chip Select 3 (CS3#) functionality of the GPIO3/CS3#*
multiplexed pin is enabled by configuring GPIOC[9] from the default
value of 0 (GPIO3) to 1.

For a chip select to assert, the address must be encompassed
within a Local Address Space.

10.6   CONTROL REGISTERS

Register 10-57. (INTCSR; 4Ch) Interrupt Control/Status

Bit	Description	Read	Write	Value after Reset
0	**LINTi1 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
1	**LINTi1 Polarity.** Value of 1 indicates active high. Value of 0 indicates active low.	Yes	Yes	0
2	**LINTi1 Status.** Value of 1 indicates interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
3	**LINTi2 Enable.** Value of 1 indicates enabled. Value of 0 indicates disabled.	Yes	Yes	0
4	**LINTi2 Polarity.** Value of 1 indicates active high. Value of 0 indicates active low.	Yes	Yes	0
5	**LINTi2 Status.** Value of 1 indicates interrupt active. Value of 0 indicates Interrupt not active.	Yes	No	0
6	**PCI Interrupt Enable.** Value of 1 enables PCI interrupt.	Yes	Yes	0
7	**Software Interrupt.** Value of 1 generates PCI interrupt (INTA# output asserted) if the PCI Interrupt Enable bit is set (bit [6]=1).	Yes	Yes	0
8	**LINTi1 Select Enable.** Value of 1 indicates enabled edge triggerable interrupt. Value of 0 indicates enabled level triggerable interrupt. ***Note:*** *Operates only in High-Polarity mode (bit [1]=1).*	Yes	Yes	0
9	**LINTi2 Select Enable.** Value of 1 indicates enabled edge triggerable interrupt. Value of 0 indicates enabled level triggerable interrupt. ***Note:*** *Operates only in High-Polarity mode (bit [4]=1).*	Yes	Yes	0
10	**Local Edge Triggerable Interrupt Clear.** Writing 1 to this bit clears LINTi1.	Yes	Yes	0
11	**Local Edge Triggerable Interrupt Clear.** Writing 1 to this bit clears LINTi2.	Yes	Yes	0
15:12	***Reserved.***	Yes	No	0h

Register 10-58. (PROT_AREA; 4Eh) Serial EEPROM Write-Protected Address Boundary

Bit	Description	Read	Write	Value after Reset
6:0	**Serial EEPROM.** Serial EEPROM starting at Lword boundary (48 Lwords = 192 bytes) for VPD accesses. Serial EEPROM addresses below this boundary are read-only. ***Note:*** *PCI 9030 configuration data is stored below Lword address 22h.*	Yes	Yes	0110000
15:7	***Reserved.***	Yes	No	0h

Register 10-59. (CNTRL; 50h) PCI Target Response, Serial EEPROM, and Initialization Control

Bit	Description	Read	Write	Value after Reset
5:0	*Reserved*.	Yes	No	0h
6	**PCI Target Write FIFO Full Condition.** Value of 1 guarantees that when the PCI Target Write FIFO is full with PCI Target Write data, there is always one location remaining empty for the PCI Target Read address to be accepted by the PCI 9030. Value of 0 Retries all PCI Target Read accesses when the PCI Target Write FIFO is full with PCI Target Write data.	Yes	Yes	0
7	**Local Arbiter LGNT Signal Select Enable.** Value of 1 selects LGNT to remain active until LREQ is de-asserted, although the PCI 9030 has a PCI Target transaction pending. Value of 0 selects LGNT to be de-asserted as soon as the PCI 9030 detects a PCI Target transaction pending and waits for LREQ to be de-asserted (Preempt condition).	Yes	Yes	0
8	**READY# Timeout Enable.** Value of 1 enables READY# timeout enable.	Yes	Yes	0
9	**READY# Timeout Select.** Values: 1 = 64 clocks 0 = 32 clocks	Yes	Yes	0
11:10	**PCI Target Delayed Write Mode.** Delay in LCLKs of ADS# from valid address. Values: 00 = 0 LCLKs 10 = 8 LCLKs 01 = 4 LCLKs 11 = 16 LCLKs	Yes	Yes	00
13:12	**PCI Configuration Base Address Register (PCIBAR) Enables.** Values: 00, 11 = PCIBAR0 (Memory) and PCIBAR1 (I/O) enabled 01 = PCIBAR0 (Memory) only 10 = PCIBAR1 (I/O) only ***Note:** PCIBAR0 and PCIBAR1 should be enabled for the PC platform.*	Yes	Yes	00
14	***PCI r2.2* Features Enable.** When set to 1, the PCI 9030 performs all PCI Read and Write transactions in compliance with *PCI r2.2*. Setting this bit enables Delayed Reads, 2^{15} PCI Clock timeout on Retries, 16- and 8-clock PCI latency rules, and enables the option to select PCI Read No Write Mode (Retries for writes) (bit [17]) and/or PCI Read with Write Flush Mode (bit [15]). Refer to Section 4.2.1.2 for additional information. Value of 0 causes TRDY# to remain de-asserted on reads until Read data is available. If Read data is not available before the PCI Target Retry Delay Clocks counter (bits [22:19]) expires, a PCI Retry is issued.	Yes	Yes	0
15	**PCI Read with Write Flush Mode.** When the *PCI r2.2* Features Enable bit is set (bit [14]=1), value of 1 flushes a pending Delayed Read cycle if a Write cycle is detected. Value of 0 (or bit [14]=0) does not affect a pending Delayed Read when a Write cycle occurs.	Yes	Yes	0

Register 10-59. (CNTRL; 50h) PCI Target Response, Serial EEPROM, and Initialization Control (Continued)

Bit	Description	Read	Write	Value after Reset
16	**PCI Read No Flush Mode.** Value of 1 does not flush the Read FIFO if the PCI Read cycle completes (PCI Target Read Ahead mode). Value of 0 flushes the Read FIFO if a PCI Read cycle completes. Read Ahead mode requires that Prefetch be enabled in the LAS*x*BRD and/or EROMBRD registers for the Memory-Mapped spaces that use Read Ahead mode. The PCI 9030 flushes its Read FIFO for each I/O-Mapped access.	Yes	Yes	0
17	**PCI Read No Write Mode (PCI Retries for Writes).** When the *PCI r2.2* Features Enable bit is set (bit [14]=1), value of 1 forces a PCI Retry on writes if a Delayed Read is pending. Value of 0 (or bit [14] =0) allows writes to occur while a Delayed Read is pending.	Yes	Yes	0
18	**PCI Write Release Bus Mode Enable.** Value of 1 disconnects if the Write FIFO becomes full. Value of 0 de-asserts TRDY# until space is available in the Write FIFO (PCI Write Hold Bus mode).	Yes	Yes	0
22:19	**PCI Target Retry Delay Clocks.** Number of PCI clocks (multiplied by 8) from the beginning of a PCI Target access, after which a PCI Retry is issued if the transfer has not completed. Valid for Read cycles only if bit [14]=0. Valid for Write cycles only if bit [18]=0.	Yes	Yes	Fh
23	**PCI Target LOCK# Enable.** Value of 1 enables PCI Target locked sequences. Value of 0 disables PCI Target locked sequences.	Yes	Yes	0
24	**Serial EEPROM Clock for PCI Bus Reads or Writes to Serial EEPROM.** Toggling this bit generates a serial EEPROM clock. (Refer to manufacturer's data sheet for the particular serial EEPROM being used.)	Yes	Yes	0
25	**Serial EEPROM Chip Select.** For PCI Bus reads or writes to the serial EEPROM, setting this bit to 1 provides serial EEPROM chip select.	Yes	Yes	0
26	**Write Bit to Serial EEPROM.** For writes, this output bit is the input to serial EEPROM. Clocked into the serial EEPROM by serial EEPROM clock.	Yes	Yes	0
27	**Read Serial EEPROM Data Bit.** For reads, this input bit is the output of serial EEPROM. Clocked out of the serial EEPROM by serial EEPROM clock.	Yes	No	—
28	**Serial EEPROM Present.** Value of 1 indicates a blank or programmed serial EEPROM is present.	Yes	No	0
29	**Reload Configuration Registers.** When set to 0, writing 1 causes the PCI 9030 to reload the Local Configuration registers from serial EEPROM.	Yes	Yes	0
30	**PCI Adapter Software Reset.** Value of 1 resets the PCI 9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI 9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI and Local Configuration registers are not reset. The PCI Interface is not reset. *Note: If PCI Target Read Ahead mode is enabled (bit [16]=1), disable it prior to a software reset, or if following a software reset, perform a PCI Target read of any valid Local Bus address, except the next sequential Lword referenced from the last PCI Target read, to flush the PCI Target Read FIFO.*	Yes	Yes	0
31	**Disconnect with Flush Read FIFO.** When the *PCI r2.2* Features Enable bit is set (bit [14]=1), value of 1 causes acceptance of a new Read request with flushing of the Read FIFO when a PCI Target Read request does not match an existing, pending Delayed Read in the Read FIFO. Value of 0, or clearing of the *PCI r2.2* Features Enable bit (bit [14]=0), causes a new Target Read request (different command, address and/or byte enables) to be Retried when a Delayed Read is pending in the Read FIFO.	Yes	Yes	0

Register 10-60. (GPIOC; 54h) General Purpose I/O Control

Bit	Description	Read	Write	Value after Reset
0	**GPIO0 or WAITo# Pin Select.** Selects the function of GPIO0/WAITo# pin. Value of 1 indicates pin is WAITo#. Value of 0 indicates pin is GPIO0.	Yes	Yes	0
1	**GPIO0 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if WAITo# function is selected.	Yes	Yes	0
2	**GPIO0 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
3	**GPIO1 or LLOCKo# Pin Select.** Selects the function of GPIO1/LLOCKo# pin. Value of 1 indicates pin is LLOCKo#. Value of 0 indicates pin is GPIO1.	Yes	Yes	0
4	**GPIO1 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if LLOCK function is selected.	Yes	Yes	0
5	**GPIO1 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
6	**GPIO2 or CS2# Pin Select.** Selects the function of GPIO2/CS2# pin. Value of 1 indicates pin is CS2#. Value of 0 indicates pin is GPIO2.	Yes	Yes	0
7	**GPIO2 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if CS2# function is selected.	Yes	Yes	0
8	**GPIO2 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
9	**GPIO3 or CS3# Pin Select.** Selects the function of GPIO3/CS3# pin. Value of 1 indicates pin is CS3#. Value of 0 indicates pin is GPIO3.	Yes	Yes	0
10	**GPIO3 Direction.** Value of 0 indicates Input. Value of 1 indicates output. Always an output if CS3# function is selected.	Yes	Yes	0
11	**GPIO3 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
12	**GPIO4 or LA27 Pin Select.** Selects the function of GPIO4/LA27 pin. Value of 1 indicates LA27. Value of 0 indicates GPIO4.	Yes	Yes	1
13	**GPIO4 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA27 is selected.	Yes	Yes	0
14	**GPIO4 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
15	**GPIO5 or LA26 Pin Select.** Selects the function of GPIO5/LA26 pin. Value of 1 indicates LA26. Value of 0 indicates GPIO5.	Yes	Yes	1
16	**GPIO5 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA26 is selected.	Yes	Yes	0
17	**GPIO5 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
18	**GPIO6 or LA25 Pin Select.** Selects the function of GPIO6/LA25 pin. Value of 1 indicates LA25. Value of 0 indicates GPIO6.	Yes	Yes	1
19	**GPIO6 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA25 is selected.	Yes	Yes	0
20	**GPIO6 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
21	**GPIO7 or LA24 Pin Select.** Selects the function of GPIO7/LA24 pin. Value of 1 indicates LA24. Value of 0 indicates GPIO7.	Yes	Yes	1
22	**GPIO7 Direction.** Value of 0 indicates input. Value of 1 indicates output. Always an output if LA24 is selected.	Yes	Yes	0
23	**GPIO7 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0

Register 10-60. (GPIOC; 54h) General Purpose I/O Control (Continued)

Bit	Description	Read	Write	Value after Reset
24	*Reserved.*	Yes	Yes	0
25	**GPIO8 Direction.** Value of 0 indicates input. Value of 1 indicates output.	Yes	Yes	0
26	**GPIO8 Data.** If programmed as output, writing 1 causes corresponding pin to go high. If programmed as input, reading provides state of corresponding pin.	Yes	Yes	0
31:27	*Reserved.*	Yes	Yes	0h

Note: GPIO pins configured as outputs are driven only when the
PCI 9030 owns the Local Bus. When another local master owns the
bus (LGNT asserted), GPIO pins configured as outputs are floated.
(Refer to PCI 9030 Errata #2 for additional information.)

Register 10-61. (PMDATASEL; 70h) Hidden 1 Power Management Data Select

Bit	Description	Read	Write	Value after Reset
7:0	**D_0 Power Consumed.** Provides the power consumed in the D_0 state. Value read from PMDATA register when Data_Select = 0.	Refer to Note	Serial EEPROM	0h
15:8	**D_3 Power Consumed.** Provides the power consumed in the D_3 state. Value read from PMDATA register when Data_Select = 3.	Refer to Note	Serial EEPROM	0h
23:16	**D_0 Power Dissipated.** Provides the power dissipated in the D_0 state. Value read from PMDATA register when Data_Select = 4.	Refer to Note	Serial EEPROM	0h
31:24	**D_3 Power Dissipated.** Provides the power dissipated in the D_3 state. Value read from PMDATA register when Data_Select = 7.	Refer to Note	Serial EEPROM	0h

Note: This register can be read only eight bits at a time,
through PMDATA[7:0]. The eight bits of PMDATASEL returned
in PMDATA[7:0] are selected by PMCSR[12:9].

Register 10-62. (PMDATASCALE; 74h) Hidden 2 Power Management Data Scale

Bit	Description	Read	Write	Value after Reset
1:0	**Data_Scale 0.** Provides the D_0 Power Consumed scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 0.	Refer to Note	Serial EEPROM	00
3:2	**Data_Scale 3.** Provides the D_3 Power Consumed scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 3.	Refer to Note	Serial EEPROM	00
5:4	**Data_Scale 4.** Provides the D_0 Power Dissipated scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 4.	Refer to Note	Serial EEPROM	00
7:6	**Data_Scale 7.** Provides the D_3 Power Dissipated scaling factor read in PMDATA[7:0]. Value read in PMCSR[14:13] when Data_Select = 7.	Refer to Note	Serial EEPROM	00
31:8	*Reserved.*	Refer to Note	Serial EEPROM	0h

Note: This register can be read only two bits at a time, through
PMCSR[14:13]. The two bits of PMDATASCALE returned in
PMCSR[14:13] are selected by PMCSR[12:9].

11   PIN DESCRIPTION

11.1   PIN SUMMARY

Tables in this section describe each PCI 9030 pin. Table 11-5 through Table 11-10 provide pin information common to all Local Bus modes of operation:

- Power and Ground
- Serial EEPROM Interface
- Test and Debug
- PCI System Bus Interface
- PCI Mode Independent Interface
- Local Bus Mode Independent Interface

Pins in Table 11-11 and Table 11-12 correspond to the PCI 9030 Local Bus modes—Multiplexed and Non-Multiplexed:

- Multiplexed Bus Mode Interface Pin Description (32-bit address/32-bit data)
- Non-Multiplexed Bus Mode Interface Pin Description (32-bit address/32-bit data)

For a visual of the chip pinout, refer to Section 13, "Physical Specifications."

The following table lists abbreviations used in this section to represent various pin types.

Table 11-1. Pin Type Abbreviations

Abbreviation	Pin Type
DTS	Driven three-state, driven high for one-half CLK before float
I	Input only
I/O	Input and output
O	Output only
OD	Open drain
STS	Sustained three-state, driven high for one CLK before float
TP	Totem pole
TS	Three-state

Note: A "#" in the pin name indicates active low.

Note for PCI pins: DO NOT pull up or down on any pins unless the PCI 9030 is being used in an embedded design. Refer to PCI r2.2.

11.2   PULL-UP AND PULL-DOWN RESISTOR RECOMMENDATIONS

Except for a 50K pull-up resistor on EEDO and a 50K pull-down resistor on BD_SEL#/TEST, no internal pull-up or pull-down resistors are present in the PCI 9030. To prevent oscillation, unused inputs should be terminated rather than left floating. The suggested values for external pull-up and pull-down resistors are 1K to 10K Ohms.

11.2.1   Input Pins (Pin Type I)

This section discusses the pull-up and pull-down resistor requirements for the following input pins—BD_SEL#/TEST, BTERM#, CPCISW, EEDO, LCLK, LINTi[2:1], LPMESET, LREQ, MODE, READY#, TCK, TDI, TMS, TRST#. (Refer to Table 11-2 for resistor requirements.)

Table 11-2. Input Pin Pull-Up and Pull-Down Resistor Requirements

Signal	Requirements
BD_SEL#/TEST	For CompactPCI Hot Swap, pull up to Early Power; otherwise, pull or tie low because the internal 50K-Ohm pull-down resistor is not sufficiently strong to guarantee proper operation.
BTERM#	If enabled, connect to a pull-up resistor to hold signal in an inactive state. If disabled for all local address spaces (default) in LASxBRD and EROMBRD, tie high or low.
CPCISW	If CompactPCI Hot Swap is not used, pull or tie low
EEDO	Use an external pull-up resistor due to the weak value (50K Ohms) of the internal pull-up resistor. The pull-up resistor must be pulled to Early Power V_{DD} in CompactPCI Hot Swap platforms and normal V_{DD} in regular PCI platforms. A missing pull-up resistor for the EEDO signal may intermittently bring the PCI 9030 to a quiescent state. If no serial EEPROM is present, can be tied to V_{DD}.
LCLK	Local clock is required. Must start prior to PCI RST# de-assertion.

Table 11-2. Input Pin Pull-Up and Pull-Down Resistor Requirements (Continued)

Signal	Requirements
LINTi[2:1]	If configured as level-sensitive (default) in INTCSR[9:8], connect to a pull-up or pull-down resistor to hold the signal in an inactive state, for the polarity configured in INTCSR[4, 1] (default is active-low). Unused pins can be tied to V_{DD} or V_{SS} to hold the input in the inactive state (V_{DD} for default active-low configuration).
LPMESET	If used to trigger PME# assertion, connect to a pull-down resistor to hold the signal in the inactive state. If not used, pull low or tie to V_{SS}.
LREQ	Pull or drive low, or tie to V_{SS} to provide Local Bus ownership to the PCI 9030.
MODE	Tie high for Multiplexed mode, or low for Non-Multiplexed mode.
READY#	If enabled, connect to a pull-up resistor to hold the signal in an inactive state. If disabled or all local address spaces (default) in LAS*x*BRD and EROMBRD, tie high or low.
TCK	If JTAG is not used, tie high or low. If used, an external pull-up resistor is required.
TDI	
TMS	
TRST#	Must be pulled low during PCI RST# assertion. If JTAG is not used, it is recommended that TRST# always be pulled low to place JTAG functionality in the reset state and enable normal chip logic operation. (Refer to *PCI 9030 Errata #5*.)

Note: *IEEE Standard 1149.1-1990 requires pull-up resistors on TDI, TMS, and TRST#. To remain compliant with PCI r2.2, no internal pull-up resistors are provided on JTAG pins in the PCI 9030; therefore, the pull-up resistors must be externally added to the PCI 9030.*

11.2.2 Output Pins (Pin Type O)

This section discusses the pull-up and pull-down resistor requirements for the following Local Bus output pins—ADS#, ALE, BCLKo, BLAST#, CS[1:0]#, EECS, EEDI, EESK, ENUM#, LA[23:2], LBE[3:0]#, LEDon#, LGNT, LPMINT#, LRESETo#, LW/R#, RD#, TDO, and WR#.

11.2.2.1 Three-State Output Pins

Three-state (TS) output pins are ADS#, ALE, BLAST#, CS[1:0]#, LA[23:2], LBE[3:0]#, LW/R#, RD#, TDO, and WR#.

The PCI 9030 drives Local Bus three-state output signals when it owns the Local Bus, and floats Local Bus three-state output signals when it does not own the Local Bus (LGNT asserted). Three-state output signals are also floated during PCI reset.

When the PCI 9030 is used in a system with multiple masters on the Local Bus, pull-up and/or pull-down resistors may be required on three-state output pins to hold control signals in the inactive state when the PCI 9030 does not own the Local Bus, and/or to reduce noise coupling between Local Bus devices.

11.2.2.2 Totem-Pole Output Pins

Totem-pole (TP) output pins are BCLKo, EECS, EEDI, EESK, LGNT, LPMINT#, and LRESETo#.

Totem-pole outputs are always driven, except when the BD_SEL#/TEST input is high and the EEDO input is low (IDDQ test state).

11.2.2.3 Open-Drain Output Pins

Open-drain (OD) output pins are ENUM# and LEDon#. (Refer to Table 11-3 for resistor requirements.)

Table 11-3. Output Pin Pull-Up and Pull-Down Resistor Requirements

Signal	Requirements
ENUM#	ENUM# is a three-state buffer that is configured as an output; therefore, a pull-up resistor is required to ensure the buffer input value is in a known state.
LEDon#	LEDon# is an open-drain output that is always enabled. HS_CSR[3] (default = 0) controls whether LEDon# sinks current or floats (default = OFF); therefore, neither a pull-up nor pull-down resistor is required. *Note:* *LEDon# is also asserted while PCI RST# input is asserted.*

11.2.3 I/O Pins (Pin Type I/O)

This section discusses the pull-up and pull-down resistor requirements for the following Local Bus I/O pins—GPIO0/WAITo#, GPIO1/LLOCKo#, GPIO2/CS2#, GPIO3/CS3#, GPIO4/LA27, GPIO5/LA26, GPIO6/LA25, GPIO7/LA24, GPIO8, LAD/LD[31:0].

The PCI 9030 drives Local Bus I/O signals when it owns the Local Bus, and floats Local Bus I/O signals when it does not own the Local Bus (LGNT asserted). During PCI reset, the PCI 9030 drives the GPIO4/LA27, GPIO5/LA26, GPIO6/LA25, GPIO7/LA24, and LAD/LD[31:0] signals low. (Refer to Table 11-4 for resistor requirements and *PCI 9030 Errata #4*.)

Table 11-4. I/O Pin Pull-Up and Pull-Down Resistor Requirements

Signal	Requirements
GPIO0/WAITo#	If GPIO[8:0] are configured as inputs and not used, pull or tie these pins to V_{DD} or V_{SS}. Under default register configuration, the following pins are configured as inputs—GPIO0/WAITo#, GPIO1/LLOCKo#, GPIO2/CS2#, GPIO3/CS3#, and GPIO8.
GPIO1/LLOCKo#	
GPIO2/CS2#	
GPIO3/CS3#	
GPIO4/LA27	
GPIO5/LA26	
GPIO6/LA25	
GPIO7/LA24	
GPIO8	***Note:*** *Refer to PCI 9030 Errata #2, regarding the GPIO[8:0] pins which, when configured as outputs, are floated when the PCI 9030 does not own the Local Bus.*
LAD/LD[31:0]	Connect unused Data Bus pins to a pull-up or pull-down resistor. Depending upon design, it is recommended to add resistors to all Data pins. When reading from a local device, the LAD/LD lines are effectively floated, and if the local device is not driving these pins (*such as* during wait states), then noise can couple into the LAD/LD inputs.

11—Pin Description

11.3   PINOUT COMMON TO ALL BUS MODES

Table 11-5. Power and Ground Pins (176-Pin PQFP)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	Function
V_{DD}	Power (+3.3V)	11	I	1, 14, 32, 45, 56, 70, 85, 100, 117, 133, 162	3.3V power supply pins for core and I/O buffers. Liberal 0.01 to 0.1 µF decoupling capacitors should be placed near the PCI 9030.
$V_{I/O}$	Voltage Input/Output	1	I	53	System voltage select, 3.3 or 5V, from the PCI Bus.
V_{SS}	Ground	14	I	13, 31, 44, 57, 66, 78, 88, 101, 113, 122, 132, 146, 163, 176	Ground pins.
Total		26			

Note: *The die contains 224 pads. Power and Grounds are double bounded in the PQFP packages to meet proper drive strength of the buffers.*

Table 11-6. Power, Ground, and No Connect Pins (180-Pin µBGA)

Symbol	Signal Name	Total Die Pads	Total Pins	Pin Type	µBGA Pin Number	Function
NC	Spare	—	4	—	A1, A14, P1, P14	Applicable only to 180-Pin µBGA. ***Unused***.
V_{DD}	Power (+3.3V)	34	11	I	B2, B6, B13, E1, F11, J5, K13, M8, N2, N5, P12	3.3V power supply pins for core and I/O buffers. Liberal 0.01 to 0.1 µF decoupling capacitors should be placed near the PCI 9030.
$V_{I/O}$	Voltage Input/Output	1	1	I	L5	System voltage select, 3.3 or 5V, from the PCI Bus.
V_{SS}	Ground	39	14	I	A2, A10, B14, C6, E13, F5, G13, J3, J10, K6, L7, N1, N10, P13	Ground pins.
Total		74	30			

Table 11-7. Serial EEPROM Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
EECS	Serial EEPROM Chip Select	1	O TP 6 mA	158	C7	Serial EEPROM chip select.
EEDI	Serial EEPROM Data In	1	O TP 6 mA	161	D6	Write data to serial EEPROM.
EEDO	Serial EEPROM Data Out	1	I	159	E7	Read data from serial EEPROM. When the BD_SEL#/TEST input pin is pulled high for Test mode, the EEDO input functions as an IDDQ Test Enable pin. When BD_SEL#/TEST input is high and EEDO is input low, the PCI 9030 output buffers are in a quiescent state and the PCI 9030 draws minimum power. When BD_SEL#/TEST and EEDO inputs are both high, all outputs except LEDon# are floated. However, the analog precharge circuits are active, and power consumption is consequently higher than a quiescent state, but is less than that consumed during normal operation.
EESK	Serial Data Clock	1	O TP 6 mA	160	A7	Serial EEPROM clock pin.
Total		4				

11—Pin Description

Note: *The serial EEPROM interface operates at core voltage (+3.3V). The PCI 9030 requires a serial EEPROM that can operate at 250 kHz, and supports sequential reads.*

Table 11-8. Test and Debug Pins

Symbol	Signal Name	Total Pins	Pin Type	CompactPCI Hot Swap Precharge Bias Voltage	PQFP Pin Number	µBGA Pin Number	Function
BD_SEL# TEST	Board Select Test Pin	1	I	No Connect	112	G11	**CompactPCI Hot Swap Systems:** Should be pulled high externally. The pull-up resistor needs to be connected to Early Power. **Non-Hot Swap and other Systems:** Should be pulled low externally. **In combination with EEDO:** Used as an IDDQ test enable pin. When pulled high, all outputs except LEDon# are placed in three-state, and PCI Hot Swap precharge resistors are active. When pulled low, all outputs remain in normal operation and PCI Hot Swap precharge resistors are not active.
TCK	Test Clock Input	1	I	1V	165	A6	Clock source for the PCI 9030 test access port (TAP). The maximum clock rate into the TCK pin is LCLK rate or less than one-half of the LCLK rate.
TDI	Test Data In	1	I	1V	168	A5	Used to input serial data into the TAP. When the TAP enables this pin, it is sampled on the rising edge of TCK and the data is input to the selected TAP Shift register. ***Note:*** *No internal pull-up.*
TDO	Test Data Output	1	O TS PCI	1V	167	C5	Used to transmit data from the PCI 9030 TAP. Data from the selected TAP Shift registers is shifted out on TDO.
TMS	Test Mode Select	1	I	1V	166	B5	Sampled by TAP on the rising edge of TCK. The TAP state machine uses the TMS pin to determine the mode in which the TAP operates. ***Note:*** *Not used to select JTAG operation.*
TRST#	Test Reset	1	I	1V	164	E6	Reset used by JTAG testers. TRST# must be asserted during PCI RST# assertion; otherwise, the PCI 9030 can initialize into an undefined state, precluding normal logic operation. If JTAG is not used, it is recommended that TRST# always be pulled low to put JTAG functionality into the reset state and enable normal chip logic operation.
Total		6					

Table 11-9. PCI System Bus Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	CompactPCI Hot Swap Precharge Bias Voltage	PQFP Pin Number	µBGA Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS PCI	1V	173-175, 2-6, 9-12, 15-18, 30, 33-39, 41-43, 46-50	A3, D4, B3, C3, C2, B1, C1, D3, E4, D1, E3, E2, F3, F2, F4, F1, J2, J1, K2, K3, K1, K4, L2, L3, M1, L4, M2, M3, N3, P2, P3, M4	All multiplexed on the same PCI pins. The Bus transaction consists of an Address phase, followed by one or more Data phases. The PCI 9030 supports both Read and Write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I	1V	7, 19, 29, 40	D2, G5, J4, L1	All multiplexed on the same PCI pins. During the Transaction Address phase, defines the bus command. During the Data phase, used as byte enables. Refer to the *PCI r2.2* for further details.
DEVSEL#	Device Select	1	O STS PCI	1V	23	G1	When actively driven, indicates the driving device decoded its address as Target of current access.
ENUM#	Enumeration	1	O OD PCI	$V_{I/O}$	51	N4	Interrupt output set when an adapter using the PCI 9030 was recently inserted or ready to be removed from a PCI slot. Used for implementing CompactPCI Hot Swap.
FRAME#	Cycle Frame	1	I	1V	20	G2	Driven by the current Master to indicate the beginning and duration of an access. FRAME# is asserted to indicate the bus transaction is beginning. While FRAME# is asserted, Data transfers continue. When FRAME# is de-asserted, the transaction is in the final Data phase.
IDSEL	Initialization Device Select	1	I	1V	8	E5	Used as a chip select during Configuration Read and Write transactions.
INTA#	Interrupt A	1	O OD PCI	$V_{I/O}$	170	B4	PCI Interrupt request.
IRDY#	Initiator Ready	1	I	1V	21	G3	Indicates initiating agent (Bus Master) ability to complete the current transaction Data phase.
LOCK#	Lock	1	I	1V	25	H2	Indicates an atomic operation that may require multiple transactions to complete.

11—Pin Description

Table 11-9. PCI System Bus Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	CompactPCI Hot Swap Precharge Bias Voltage	PQFP Pin Number	µBGA Pin Number	Function
PAR	Parity	1	I/O TS PCI	1V	28	H1	Even parity across AD[31:0] and C/BE[3:0]#. All PCI agents require parity generation. PAR is stable and valid one clock after the Address phase. For Data phases, PAR is stable and valid one clock after either IRDY# is asserted on a Write transaction or TRDY# is asserted on a Read transaction. Once PAR is valid, it remains valid until one clock after current Data phase completes.
PCLK	Clock	1	I	No Connection	172	A4	Provides timing for all transactions on the PCI Bus and is an input to every PCI device. The PCI 9030 operates up to 33 MHz. ***Note:*** *On Expansion boards, trace length for the PCI PCLK signal must be 2.5 inches ±0.1 inches, and must be routed to only one load, per PCI r2.2.*
PERR#	Parity Error	1	O STS PCI	1V	26	H3	Reports data parity errors during all PCI transactions, except during a special cycle.
PME#	Power Management Event	1	O OD PCI	$V_{I/O}$	169	D5	Wake-up event interrupt. ***Note:*** *If PME# is implemented, a field-effect transistor (FET) should be used to isolate the signal when power is removed from the card. (Refer to PCI Power Mgmt. r1.1.) If PME# is not used, then connect it through a pull-up resistor to $V_{I/O}$.*
RST#	Reset	1	I	$V_{I/O}$	171	C4	Used to bring PCI-specific registers, sequencers, and signals to a default state.
SERR#	System Error	1	O OD PCI	1V	27	H5	Reports address parity errors or any other system error where the result is catastrophic.
STOP#	Stop	1	O STS PCI	1V	24	H4	Indicates the current Target is requesting that the Master stop the current transaction.
TRDY#	Target Ready	1	O STS PCI	1V	22	G4	Indicates the Target agent (selected device) ability to complete the current Data phase transaction.
Total		51					

Table 11-10. Local Bus Mode Independent Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	μBGA Pin Number	Function
BCLKo	Buffered Clock Out	1	O TP 12 mA	71	K8	Provides a buffered version PCI clock for optional use by the Local Bus. Not in phase with the PCI clock.
CPCISW	CompactPCI Switch	1	I	54	P4	CompactPCI board latch status input.
CS[1:0]#	Chip Selects	2	O TS 12 mA	148, 147	B9, C9	General purpose chip selects. The base and range of each is programmable by Configuration registers.
GPIO0 WAITo#	General Purpose I/O 0 WAIT Out	1	I/O TS 12 mA	154	D8	Can be programmed to a configurable general purpose I/O pin, GPIO0, or Local Bus WAIT out pin, WAITo#. WAITo# is asserted when wait states are caused by the internal wait state generator. Serves as an output to provide ready-out status. Default functionality is GPIO0 input. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[1:0] register bits.
GPIO1 LLOCKo#	General Purpose I/O 1 LLOCK Out	1	I/O TS 12 mA	155	A8	Can be programmed to a configurable general purpose I/O pin, GPIO1, or Local Bus LLOCK out pin, LLOCKo#. LLOCKo# indicates an atomic operation that may require multiple transactions to complete and can be used by the Local Bus to lock resources. Default functionality is GPIO1 input. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[4:3] register bits. The PCI 9030 asserts LLOCKo# during the first clock of an atomic operation (Address cycle), and de-asserts it a minimum of one clock following the last Bus access for the atomic operation. LLOCKo# is de-asserted after the PCI 9030 detects PCI FRAME#, with PCI LOCK# concurrently de-asserted.
GPIO2 CS2#	General Purpose I/O 2 Chip Select 2 Out	1	I/O TS 12 mA	156	D7	Can be programmed to a configurable general purpose I/O pin, GPIO2, or as Chip Select 2 output pin, CS2#. Default functionality is GPIO2 input. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[7:6] register bits.
GPIO3 CS3#	General Purpose I/O 3 Chip Select 3 Out	1	I/O TS 12 mA	157	B7	Can be programmed to a configurable general purpose I/O pin, GPIO3, or as Chip Select 3 output pin, CS3#. Default functionality is GPIO3 input. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[10:9] register bits.

11—Pin Description

Table 11-10. Local Bus Mode Independent Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
GPIO8	General Purpose I/O 8	1	I/O TS 12 mA	94	L12	Configurable general purpose I/O pin.
LCLK	Local Bus Clock	1	I	145	E9	Local clock, up to 60 MHz, and may be asynchronous to PCI clock.
LEDon#	LED On	1	O OD 24 mA	52	K5	Hot Swap board indicator LED. LEDon# is controlled by the LED Software On/Off Switch bit (HS_CSR[3]) and is also asserted during PCI reset.
LGNT	Local Bus Grant	1	O TP 12 mA	150	A9	Asserted by PCI 9030 to grant control of the Local Bus to a Local Bus Master. When the PCI 9030 requires the Local Bus, it can optionally signal a preempt by de-asserting LGNT, if the Disconnect with Flush Read FIFO bit is clear (CNTRL[31]=0) (default).
LINTi1	Local Interrupt Input 1	1	I	152	B8	When enabled (INTCSR[0]=1) and asserted, the LINTi1 status bit sets (INTCSR[2]=1). If the PCI Interrupt Enable bit is set (INTCSR[6]=1), then INTA# asserts. LINTi1 is programmable for active-low or active-high polarity in INTCSR[1] in the default Level-Sensitive mode (INTCSR[8]=0). Can be optionally configured as a positive edge-triggered interrupt (INTCSR[8, 1, 0]=111) *such as* in the case of ISA compatibility. Level-sensitive interrupts are cleared when the interrupt source is no longer active, or LINTi1 is disabled. An edge-triggered interrupt is set and latched by a LINTi1 low-to-high transition, and cleared by setting the LINTi1 Local Edge Triggerable Interrupt Clear bit (INTCSR[10]=1).
LINTi2	Local Interrupt Input 2	1	I	153	C8	When enabled (INTCSR[3]=1) and asserted, the LINTi2 Status bit sets (INTCSR[5]=1). If the PCI Interrupt Enable bit is also set (INTCSR[6]=1), then INTA# asserts. LINTi2 is programmable for active-low or active-high polarity in INTCSR[4] in the default Level-Sensitive mode (INTCSR[9]=0). Can be optionally configured as a positive edge-triggered interrupt (INTCSR[9, 4, 3]=111), *such as* in the case of ISA compatibility. Level-sensitive interrupts are cleared when the interrupt source is no longer active, or LINTi2 is disabled. An edge-triggered interrupt is set and latched by a LINTi2 low-to-high transition, and cleared by setting the LINTi2 Local Edge Triggerable Interrupt Clear bit (INTCSR[11]=1).

Table 11-10. Local Bus Mode Independent Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
LPMESET	Local Power Management Event Set	1	I	103	J12	As an input, the Local Initiator can issue LPMESET to the PCI 9030 in the case of a Power Management Wake-Up event. LPMESET must be asserted to the PCI 9030 no less than one Local Clock pulse. The PCI 9030 latches the LPMESET assertion, sets the PME_Status bit (PMCSR[15]), and asserts PME# to the PCI Bus, if enabled.
LPMINT#	Local Power Management Interrupt	1	O TP 12 mA	126	D13	Could be used for Local Power Management Events. The PCI 9030 drives the interrupt to the external Master to request a Power State Change.
LREQ	Local Bus Request	1	I	151	E8	Asserted by a Local Bus Master to request Local Bus use. The PCI 9030 can be made master of the Local Bus by pulling LREQ low (or by grounding LREQ).
LRESETo#	Local Bus Reset Out	1	O TP 12 mA	149	D9	Asserted when the PCI 9030 chip is reset. Can be used to drive the Local processor's RESET# input.
MODE	Bus Mode	1	I	76	K9	Selects the PCI 9030 Bus Operation mode. Values: 0 = Non-Multiplexed mode 1 = Multiplexed mode **Note:** *The MODE input level must be stable at power-on.*
Total		19				

11—Pin Description

11.4   MULTIPLEXED LOCAL BUS MODE PINOUT

Table 11-11. Multiplexed Bus Mode Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
ADS#	Address Strobe	1	O TS 12 mA	138	C11	Indicates a valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
ALE	Address Latch Enable	1	O TS 12 mA	75	M9	Asserted during the Address phase and de-asserted before the Data phase.
BLAST#	Burst Last	1	O TS 12 mA	139	B11	Driven by the current Local Bus Master to indicate the last transfer in a Bus access.
BTERM#	Burst Terminate	1	I	144	B10	If Bterm mode (continuous burst) and the BTERM# input are disabled (LAS*x*BRD[2]=0 and/or EROMBRD[2]=0), the PCI 9030 also bursts up to four Lwords. If Bterm mode (continuous burst) and the BTERM# input are enabled (LAS*x*BRD[2]=1 and/or EROMBRD[2]=1), the PCI 9030 continues to burst until BTERM# input is asserted or the burst completes. BTERM# is a ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9030 programmable wait state generator. BTERM# is not sampled until external wait states expire [WAITo# de-asserted, provided GPIO0/WAITo# is configured as WAITo# (GPIOC[0]=1)].
GPIO4 LA27	General Purpose I/O 4 Address Bus	1	I/O TS 12 mA O TS 12 mA	137	A12	Can be programmed to a configurable general purpose I/O pin, GPIO4, or as Address Bus output pin, LA27. Default functionality is LA27. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[13:12] register bits.
GPIO5 LA26	General Purpose I/O 5 Address Bus	1	I/O TS 12 mA O TS 12 mA	136	A13	Can be programmed to a configurable general purpose I/O pin, GPIO5, or as Address Bus output pin, LA26. Default functionality is LA26. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[16:15] register bits.
GPIO6 LA25	General Purpose I/O 6 Address Bus	1	I/O TS 12 mA O TS 12 mA	135	B12	Can be programmed to a configurable general purpose I/O pin, GPIO6, or as Address Bus output pin, LA25. Default functionality is LA25. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[19:18] register bits.

Table 11-11. Multiplexed Bus Mode Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
GPIO7 LA24	General Purpose I/O 7 Address Bus	1	I/O TS 12 mA O TS 12 mA	134	C12	Can be programmed to a configurable general purpose I/O pin, GPIO7, or as Address Bus output pin, LA24. Default functionality is LA24. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[22:21] register bits.
LA[23:2]	Address Bus	22	O TS 12 mA	131-127, 125-123, 121-118, 116-114, 111-105	C13, D11, C14, D14, D12, E11, E14, E12, F14, F10, F12, F13, G14, G10, G12, H14, H11, H12, H13, H10, J14, J11	Carries the upper 22 bits of the 28-bit physical Address Bus. Increments during bursts indicate successive Data cycles.
LAD[31:0]	Address/ Data Bus	32	I/O TS 12 mA	61-65, 67-69, 72-74, 77, 79-84, 86-87, 89-93, 95-99, 102, 104	L6, P6, K7, N7, M7, P7, L8, N8, P8, L9, N9, P9, M10, P10, L10, N11, M11, P11, L11, N12, N13, M12, M13, N14, M14, L13, K10, K11, L14, K12, K14, J13	During an Address phase, the bus carries the upper 26 bits of 28-bit physical Address Bus [27:2]. During the Data phase, the Bus carries 32-, 16-, or 8-bit data quantities, depending on bus width configuration: • 8-bit = LAD[7:0] • 16-bit = LAD[15:0] • 32-bit = LAD[31:0] During an ADS# assertion, carries the Local Address Bus (LA[27:2]).
LBE[3:0]#	Byte Enables	4	O TS 12 mA	55, 58-60	M5, P5, M6, N6	Encoded, based on the bus-width configuration: **32-Bit Bus** Four byte enables indicate which of the four bytes are active during a data cycle: • LBE3# Byte Enable 3 = LAD[31:24] • LBE2# Byte Enable 2 = LAD[23:16] • LBE1# Byte Enable 1 = LAD[15:8] • LBE0# Byte Enable 0 = LAD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: • LBE3# Byte High Enable (BHE#) = LAD[15:8] • LBE2# *Unused* • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LAD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0], respectively: • LBE3# *Unused* • LBE2# *Unused* • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)

Table 11-11. Multiplexed Bus Mode Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
LW/R#	Write/Read	1	O TS 12 mA	142	A11	Asserted low for reads and high for writes.
RD#	Read Strobe	1	O TS 12 mA	141	D10	General purpose read strobe. Timing is controlled by current Bus Region Descriptor register. Normally asserted during NRAD wait states, unless Read Strobe Delay clocks are programmed in bits [27:26]. Remains asserted throughout Burst and NRDD wait states.
READY#	Local Ready Input	1	I	143	C10	Local ready input indicates Read data is on the Local Bus, or that Write data is accepted. READY# input is not sampled until internal wait states expire [WAITo# de-asserted, provided GPIO0/WAITo# is configured as WAITo# (GPIOC[0]=1)]. READY# is ignored when BTERM# is enabled and asserted.
WR#	Write Strobe	1	O TS 12 mA	140	E10	General purpose write strobe. Timing is controlled by the current Bus Region Descriptor register. Normally asserted during NWAD wait states, unless Write Strobe Delay clocks are programmed in bits [29:28]. Remains asserted throughout Burst and NWDD wait states. LAD/LD data valid time can be extended beyond WR# de-assertion if Write Cycle Hold clocks are programmed in bits [31:30].
Total		70				

11.5   NON-MULTIPLEXED LOCAL BUS MODE PINOUT

Table 11-12. Non-Multiplexed Bus Mode Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
ADS#	Address Strobe	1	O TS 12 mA	138	C11	Indicates a valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
ALE	Address Latch Enable	1	O TS 12 mA	75	M9	Asserted during the Address phase and de-asserted before the Data phase.
BLAST#	Burst Last	1	O TS 12 mA	139	B11	Driven by the current Local Bus Master to indicate the last transfer in a Bus access.
BTERM#	Burst Terminate	1	I	144	B10	If Bterm mode (continuous burst) and BTERM# input are disabled (LASxBRD[2]=0 and/or EROMBRD[2]=0), the PCI 9030 also bursts up to four Lwords. If enabled, the PCI 9030 continues to burst until BTERM# input is asserted or the burst completes. BTERM# is a Ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9030 programmable wait state generator.
GPIO4 LA27	General Purpose I/O 4 Address Bus	1	I/O TS 12 mA	137	A12	Can be programmed to a configurable general purpose I/O pin, GPIO4, or as Address Bus output pin, LA27. Default functionality is LA27. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[13:12] register bits.
GPIO5 LA26	General Purpose I/O 5 Address Bus	1	I/O TS 12 mA	136	A13	Can be programmed to a configurable general purpose I/O pin, GPIO5, or as Address Bus output pin, LA26. Default functionality is LA26. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[16:15] register bits.
GPIO6 LA25	General Purpose I/O 6 Address Bus	1	I/O TS 12 mA	135	B12	Can be programmed to a configurable general purpose I/O pin, GPIO6, or as Address Bus output pin, LA25. Default functionality is LA25. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[19:18] register bits.
GPIO7 LA24	General Purpose I/O 7 Address Bus	1	I/O TS 12 mA	134	C12	Can be programmed to a configurable general purpose I/O pin, GPIO7, or as Address Bus output pin, LA24. Default functionality is LA24. Pin configuration occurs when the serial EEPROM contents are loaded following PCI reset, or upon subsequent writing to the GPIOC[22:21] register bits.

11—Pin Description

Table 11-12. Non-Multiplexed Bus Mode Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	μBGA Pin Number	Function
LA[23:2]	Address Bus	22	O TS 12 mA	131-127, 125-123, 121-118, 116-114, 111-105	C13, D11, C14, D14, D12, E11, E14, E12, F14, F10, F12, F13, G14, G10, G12, H14, H11, H12, H13, H10, J14, J11	Carries the upper 22 bits of the 28-bit physical Address Bus. Increments during bursts indicate successive Data cycles.
LBE[3:0]#	Byte Enables	4	O TS 12 mA	55, 58-60	M5, P5, M6, N6	Encoded, based on the bus-width configuration: **32-Bit Bus** Four byte enables indicate which of the four bytes are active during a data cycle: • LBE3# Byte Enable 3 = LD[31:24] • LBE2# Byte Enable 2 = LD[23:16] • LBE1# Byte Enable 1 = LD[15:8] • LBE0# Byte Enable 0 = LD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: • LBE3# Byte High Enable (BHE#) = LD[15:8] • LBE2# *Unused* • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) = LD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0], respectively: • LBE3# *Unused* • LBE2# *Unused* • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)
LD[31:0]	Data Bus	32	I/O TS 12 mA	61-65, 67-69, 72-74, 77, 79-84, 86-87, 89-93, 95-99, 102, 104	L6, P6, K7, N7, M7, P7, L8, N8, P8, L9, N9, P9, M10, P10, L10, N11, M11, P11, L11, N12, N13, M12, M13, N14, M14, L13, K10, K11, L14, K12, K14, J13	Carries 8-, 16-, or 32-bit data quantities, depending upon a Target bus-width configuration: • 8-bit = LD[7:0] • 16-bit = LD[15:0] • 32-bit = LD[31:0]
LW/R#	Write/Read	1	O TS 12 mA	142	A11	Asserted low for reads and high for writes.

Table 11-12. Non-Multiplexed Bus Mode Interface Pins (Continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	µBGA Pin Number	Function
RD#	Read Strobe	1	O TS 12 mA	141	D10	General purpose read strobe. Timing is controlled by current Bus Region Descriptor register. Normally asserted during NRAD wait states, unless Read Strobe Delay clocks are programmed in bits [27:26]. Remains asserted throughout Burst and NRDD wait states.
READY#	Local Ready Input	1	I	143	C10	Local ready input indicates Read data on the bus is valid or a Write Data transfer is complete. READY# input is not sampled until the internal wait state counter expires (WAITo# de-asserted).
WR#	Write Strobe	1	O TS 12 mA	140	E10	General purpose write strobe. Timing is controlled by the current Bus Region Descriptor register. Normally asserted during NWAD wait states, unless Write Strobe Delay clocks are programmed in bits [29:28]. Remains asserted throughout Burst and NWDD wait states. LAD/LD data valid time can be extended beyond WR# de-assertion if Write Cycle Hold clocks are programmed in bits [31:30].
Total		70				

11—Pin Description

11.6   DEBUG INTERFACE

The PCI 9030 provides a JTAG Boundary Scan interface which can be utilized to debug a pin's connectivity to the board.

11.6.1   IEEE 1149.1 Test Access Port (JTAG Debug Port)

The IEEE 1149.1 Test Access Port (TAP), commonly called the JTAG (Joint Test Action Group) debug port, is an architectural standard described in IEEE Standard 1149.1-1990. This standard describes a method for accessing internal chip facilities using a four- or five-signal interface.

The JTAG debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with IEEE Standard 1149.1-1990 for vendor-specific extensions, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals**—JTAG debug port implements the four required JTAG signals—TCK, TMS, TDI, TDO—and the optional TRST# signal.
- **JTAG Clock Requirements**—The TCK signal frequency can range from DC to one-half of the internal chip clock frequency.
- **JTAG Reset Requirements**—JTAG debug port logic is reset at the same time as a system reset. Upon receiving TRST#, the JTAG TAP controller returns to the Test-Logic Reset state.

11.6.2   JTAG Instructions

The JTAG debug port provides the standard **extest, sample/preload,** and **bypass** instructions. Invalid instructions behave as the **bypass** instruction. There are three private instructions. (Refer to Table 11-13.) The Instruction register length is 236 bits, and instruction length is 4 bits. The PCI 9030 does not have an IDCODE register.

Table 11-13. JTAG Instructions

Instruction	Input Code	Comments
Extest	0000	IEEE Standard 1149.1-1990
Sample/Preload	0100	
Bypass	1111	

11.6.3   JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to IEEE Standard 1149.1-1990. BSDL, a subset of the IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL), allows a rigorous description of testability features in components which comply with the standard. It is used by automated test pattern generation tools for package interconnect tests and electronic design automation (EDA) tools for synthesized test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical port description, physical pin map, instruction set, and boundary register description.

The logical port description assigns symbolic names to the pins of a chip. Each pin has a logical type of in, out, inout, buffer, or linkage that defines the logical direction of signal flow.

The physical pin map correlates the logical ports of the chip to the physical pins of a specific package. A BSDL description can have several physical pin maps; each map is given a unique name.

Instruction set statements describe the bit patterns that must be shifted into the Instruction register to place the chip in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the chip.

The boundary register description lists each cell or shift stage of the Boundary register. Each cell has a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) pin and the cell with the highest number is closest to the Test Data In (TDI) pin. Each cell contains additional information, including: cell type, logical port associated with the cell, logical function of the cell, safe value, control cell number, disable value, and result value.

Notes: The PCI 9030 BSDL files for the PQFP and µBGA packages may be downloaded from the PCI 9030 toolbox at http://www.plxtech.com/products/9030.htm

Refer to PCI 9030 Errata #5, #6, and #8 for information regarding specific JTAG issues.

12   ELECTRICAL SPECIFICATIONS

12.1   GENERAL ELECTRICAL SPECIFICATIONS

Table 12-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage Temperature	-55 to +125 °C
Ambient Temperature with Power Applied	-40 to +85 °C
Supply Voltage to Ground	-0.5 to +4.6V
Input Voltage (V_{IN})	V_{SS} -0.5 to 11.0V
Output Voltage (V_{OUT})	V_{SS} -0.5V to V_{DD} +0.5
Maximum Package Power Dissipation	
176-Pin PQFP	1W
180-Pin µBGA	0.5W

Note: *Package Power Dissipation derived with assumption that 1.0m/s air flow is available.*

Table 12-2. Operating Ranges

Ambient Temperature	Supply Voltage (V_{DD})	Input Voltage (V_{IN})	
		Min	Max
-40 to +85 °C	3.0 to 3.6V	VSS	11.0V

Table 12-3. Capacitance (Sample Tested Only)

Parameter	Test Conditions	Pin Type	Value		Units
			Typical	Maximum	
C_{IN}	V_{IN} = 0V	Input	4	6	pF
C_{OUT}	V_{OUT} = 0V	Output	6	10	pF

The following table lists the package thermal resistance (Θ_{j-a}).

Table 12-4. Package Thermal Resistance

Package Type	Air Flow			
	0m/s	1m/s	2m/s	3m/s
176-Pin PQFP	65 (°C/W)	45	35	30
180-Pin µBGA	48 (°C/W)	34	26	22

Table 12-5. Electrical Characteristics over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}[1]	Output High Voltage	V_{DD} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -12.0 mA	2.4	—	V
V_{OL}[1]	Output Low Voltage		I_{OL} = 12 mA	—	0.4	V
V_{IH}	Input High Level	—	—	2.0	11.0	V
V_{IL}	Input Low Level	—	—	-0.5	0.8	V
V_{OH3}	PCI 3.3V Output High Voltage	V_{DD} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -500 µA	0.9 V_{DD}	—	V
V_{OL3}	PCI 3.3V Output Low Voltage		I_{OL} = 1500 µA	—	0.1 V_{DD}	V
V_{IH3}	PCI 3.3V Input High Level	—	—	0.5 V_{DD}	V_{DD} +0.5	V
V_{IL3}	PCI 3.3V Input Low Level	—	—	-0.5	0.3 V_{DD}	V
I_{IL}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$, V_{DD} = Max		-10	+10	µA
I_{LPC}[2]	DC Current Per Pin during Precharge	V_P = 0.8 to 1.2V[3]		—	1.0	mA
I_{OZ}	Three-State Output Leakage Current	V_{DD} = Max		-10	+10	µA
I_{CC}	Power Supply Current	V_{DD} = 3.6V, PCLK = 33 MHz, LCLK = 60 MHz 80 outputs switching simultaneously		—	150	mA
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max V_{IN} = GND or V_{CC}		—	50	µA

Notes:

[1]   *Except in the case of EECS, EEDI, EESK, and LEDon# pins.*

[2]   *I_{LPC} is the DC current flowing from V_{DD} to Ground during precharge, as both PMOS and NMOS devices remain on during precharge. It is not the leakage current flowing into or out of the pin under precharge.*

[3]   *V_P is precharge bias voltage.*

12.2   LOCAL INPUTS

Definitions:

- **T$_{HOLD}$**—Time that an input signal is stable after the rising edge of the Local Clock.

- **T$_{SETUP}$**—Setup time. The time that an input signal is stable before the rising edge of the Local Clock.
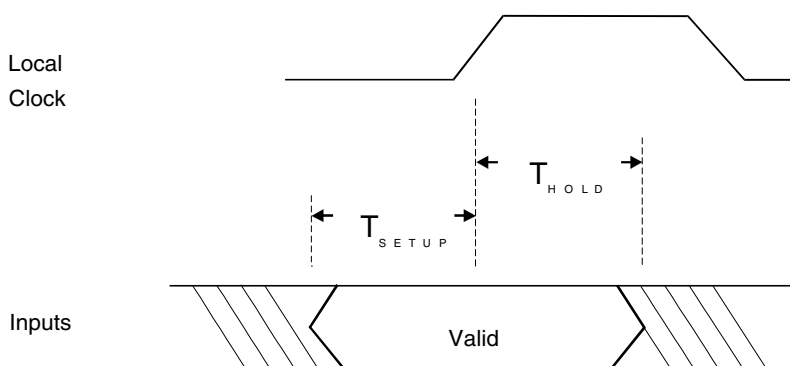
Figure 12-1. PCI 9030 Local Input Setup and Hold Waveform

Table 12-6. AC Electrical Characteristics (Local Inputs) over Operating Range

Signals (Synchronous Inputs) C$_L$ = 50 pF, V$_{CC}$ = 3.0V, Ta = 85 °C	Bus Mode	T$_{SETUP}$ (ns) (Worst Case)	T$_{HOLD}$ (ns) (Worst Case)
BTERM#	All	7.0	1
LAD[31:0] (Data)	Multiplexed	5.0	1
LD[31:0]	Non-Multiplexed	5.0	1
LPMESET	All	5.0	1
LREQ	All	5.0	1
READY#	All	7.0	1
Input Clocks	**Bus Mode**	**Min**	**Max**
Local Clock Input Frequency	All	0	60 MHz
PCI Clock Input Frequency	All	0	33 MHz

Note: *These values are provided as an example and are only representative of PLX PCI device general performance characteristics.*

12—Electrical Specs

12.3   LOCAL OUTPUTS

Definition:

- **T$_{VALID}$**—Output valid (clock-to-out). The time after the rising edge of the Local Clock until the output is stable.
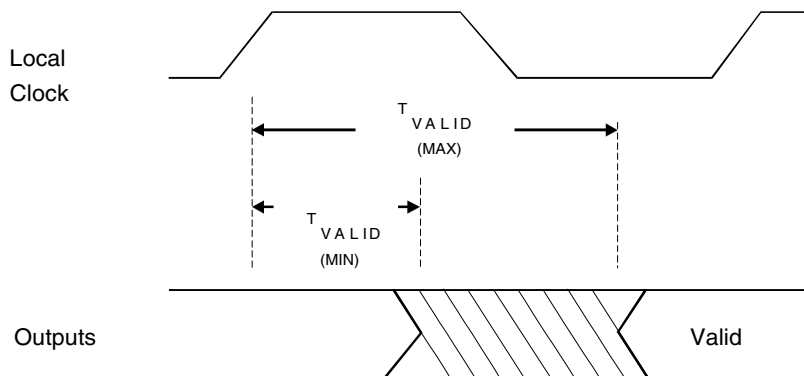
Figure 12-2. PCI 9030 Local Output Delay

Table 12-7. AC Electrical Characteristics (Local Outputs) over Operating Range

Signals (Synchronous Outputs) V$_{CC}$ = 3.0V, Ta = 85 °C	Bus Mode	Output T$_{VALID}$ (Max)
ADS#	All	10.0
BLAST#	All	10.0
CS[3:0]#	All	10.0
LA[27:2]	All	10.0
LAD[31:0] (Data)	Multiplexed	10.0
LBE[3:0]#	All	10.0
LD[31:0]	Non-Multiplexed	10.0
LGNT	All	11.0
LLOCKo#	All	10.0
LPMINT#	All	10.0
LW/R#	All	10.0
RD#	All	10.0
WAITo#	All	10.0
WR#	All	10.0

Notes: All T$_{VALID}$ (Min) values are greater than 5 ns.

Timing derating for loading is ±35 PS/PF.

These values are provided as an example and are representative only of PLX PCI device general performance characteristics.
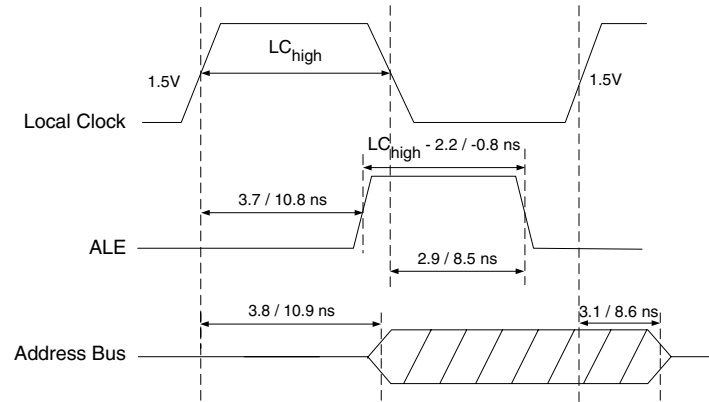
Figure 12-3. PCI 9030 ALE Output Delay (Min/Max) to the Local Clock

13   PHYSICAL SPECIFICATIONS

13.1   176-PIN PQFP
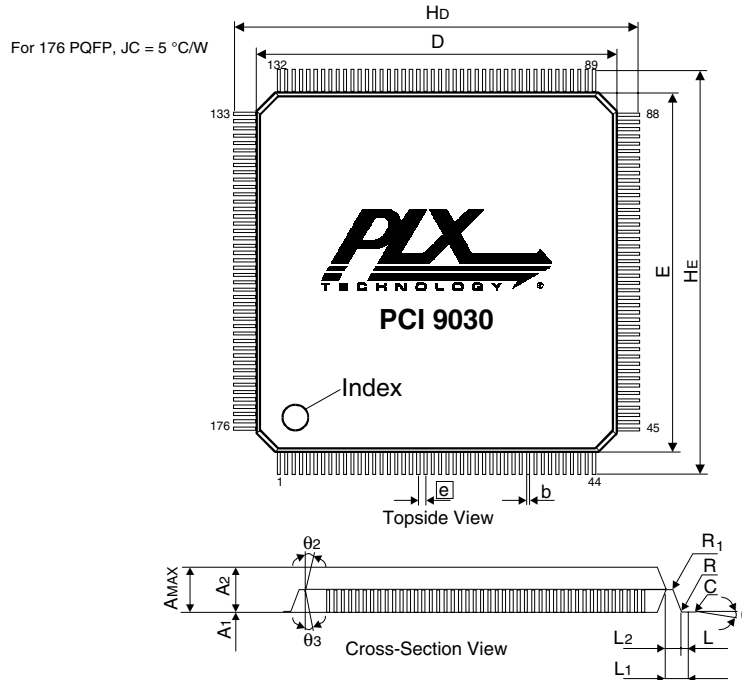
Figure 13-1. 176-Pin PQFP Package Mechanical Dimensions—Topside and Cross-Section Views

Note: *PLX Technology, Inc., has standardized the top side marking for all PCI products. Marking content has changed and affects inspection, pattern recognition, and tray and board loading equipment.*

Table 13-1. 176-Pin PQFP Package Mechanical Dimensions (Legend for Figure 13-1)

Lead Type STD (QFP18-176 Pin STD)							
Symbol[1]	Dimensions (mm)			Symbol[1]	Dimensions (mm)		
	Min.	Nom.	Max.		Min.	Nom.	Max.
E	23.9	24	24.1	L	0.3	0.5	0.7
D	23.9	24	24.1	L_1	—	1	—
A	—	—	3	L_2	—	0.5	—
A_1	—	0.1	—	H_E	25.6	26	26.4
A_2	2.6	2.7	2.8	H_D	25.6	26	26.4
e	—	0.5	—	$\theta 2$	—	15°	—
b	0.15	0.2	0.3	$\theta 3$	—	15°	—
C	0.1	0.15	0.2	R	—	0.2	—
θ	0°	—	10°	R_1	—	0.2	—

[1] Refer to Table 13-2 for an explanation of these symbols.

Table 13-2. Symbol Definitions—PQFP Package

Symbol	Term	Definition	Symbol	Term	Definition
E	Package width	Width of package	C	Lead thickness	Thickness of lead (excluding surface plating)
D	Package length	Length of package	θ	Lead angle	Angle of leads versus seating plane
A	Mounting height	Height from the ground plane to the top of the package	$\theta 2, \theta 3$	Chamfer angle	Package chamfer angle
A_1	Standoff height	Height from the ground plane to the bottom edge of the package (PGA)	L, L_1, L_2	Lead length or length of flat lead section	Lead length or length of flat lead section
A_2	Package height	Height of the package (excluding warp of package)	H_E	Overall width	Width including leads
e	Linear lead pitch	Theoretical lead pitch	H_D	Overall length	Length
b	Lead width	Lead width or diameter (excluding surface plating)	R, R_1	Reverse bending	Reverse bending type
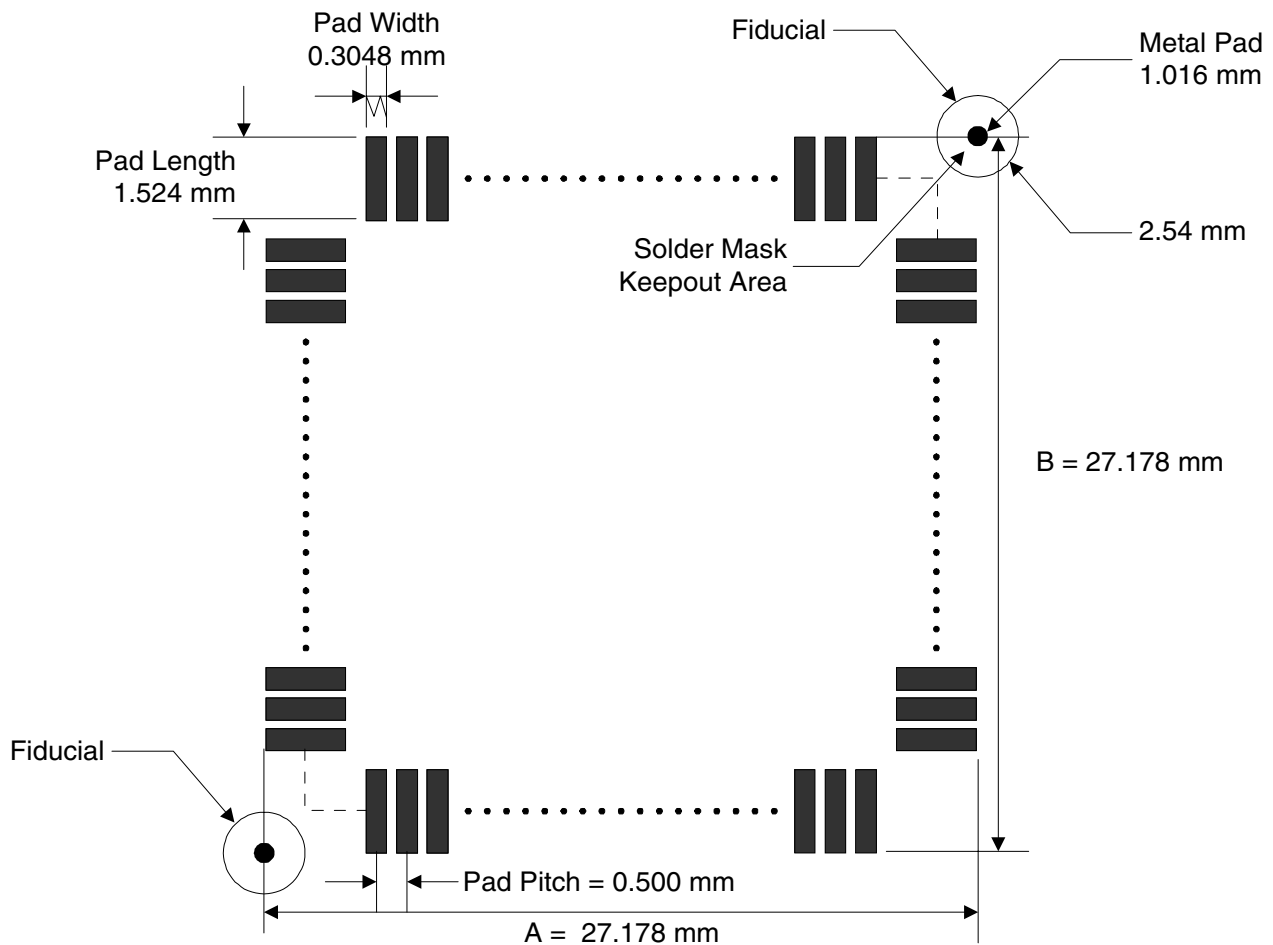
Figure 13-2. 176-Pin PQFP PCB Layout Suggested Land Pattern

Figure 13-3. 176-Pin PQFP Pinout

13—Physical Specs

13.2   180-PIN µBGA
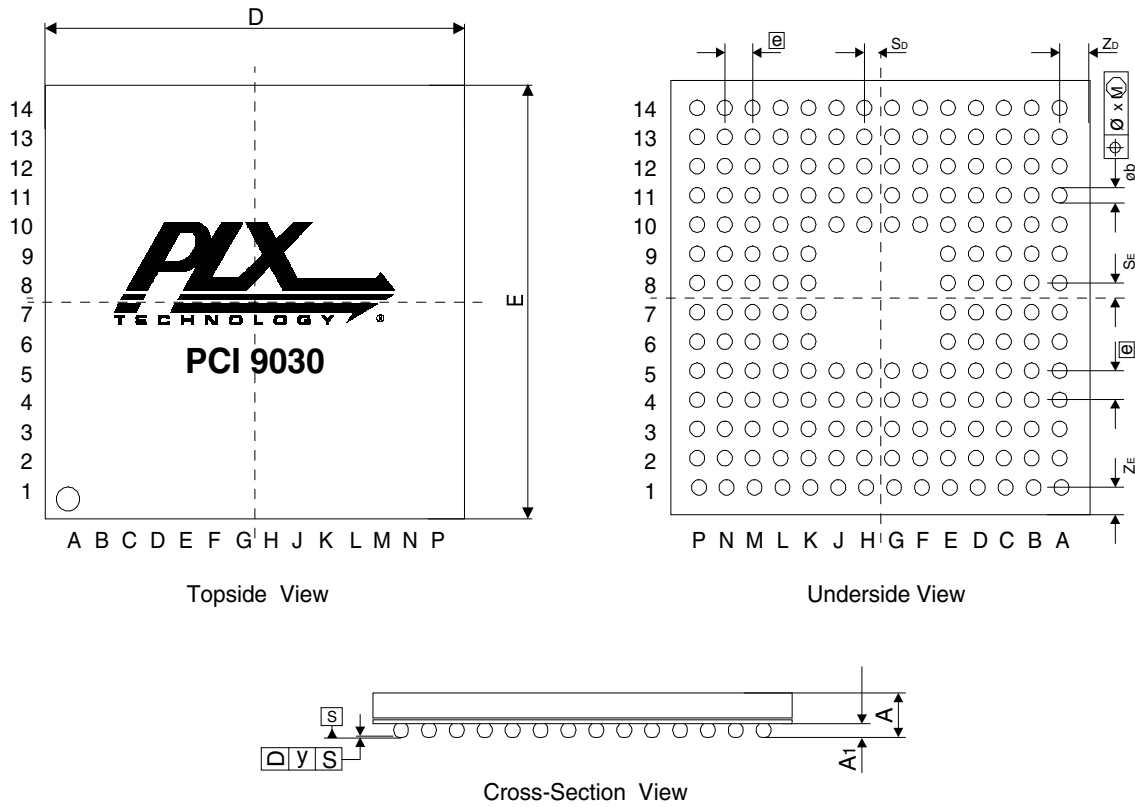
Figure 13-4. 180-Pin µBGA Package Mechanical Dimensions—Topside, Underside, and Cross-Section Views

Note: *PLX Technology, Inc., has standardized the top side marking for all PCI products. Marking content has changed and affects inspection, pattern recognition, and tray and board loading equipment.*

Table 13-3. 180-Pin µBGA Package Mechanical Dimensions (Legend for Figure 13-4)

Symbol[1]	Dimensions (mm)			Symbol[1]	Dimensions (mm)		
	Min.	Nom.	Max.		Min.	Nom.	Max.
D	11.85	12.0	12.3	x	—	—	0.08
E	11.85	12.0	12.3	y	—	—	0.10
A	—	—	1.20	S_D	—	0.40	—
A_1	0.30	0.35	0.45	S_E	—	0.40	—
e	—	0.80	—	Z_D	—	0.80	—
øb	0.40	0.45	0.55	Z_E	—	0.80	—

[1] Refer to Table 13-4 for an explanation of these symbols.

Table 13-4. Symbol Definitions—µBGA Package

Symbol	Term	Definition	Symbol	Term	Definition
E	Package width	Width of package	A₁	Ball height	Height from the ground plane to the bottom edge of the package (PGA)
D	Package length	Length of package	e	Ball pitch	Theoretical lead pitch
A	Height	Height from the ground plane to the top of the package	b	Ball width	Ball width or diameter (excluding surface plating)

Topside View
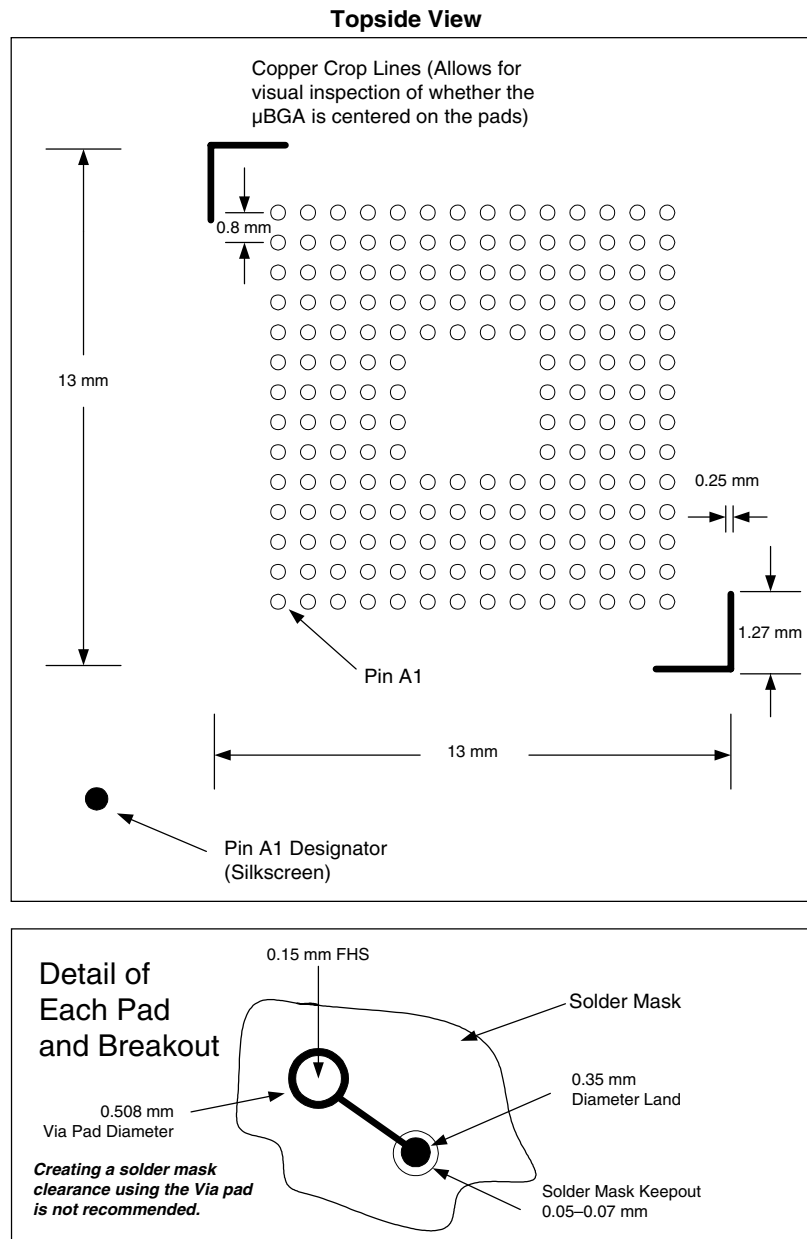
Figure 13-5. 180-Pin µBGA PCB Layout Suggested Land Pattern

13—Physical Specs

	14	13	12	11	10	9	8	7	6	5	4	3	2	1
P	NC	VSS	VDD	LAD14 (M) LD14 (NM)	LAD18 (M) LD18 (NM)	LAD20 (M) LD20 (NM)	LAD23 (M) LD23 (NM)	LAD26 (M) LD26 (NM)	LAD30 (M) LD30 (NM)	LBE2#	CPCISW	AD1	AD2	NC
N	LAD8 (M) LD8 (NM)	LAD11 (M) LD11 (NM)	LAD12 (M) LD12 (NM)	LAD16 (M) LD16 (NM)	VSS	LAD21 (M) LD21 (NM)	LAD24 (M) LD24 (NM)	LAD28 (M) LD28 (NM)	LBE0#	VDD	ENUM#	AD3	VDD	VSS
M	LAD7 (M) LD7 (NM)	LAD9 (M) LD9 (NM)	LAD10 (M) LD10 (NM)	LAD15 (M) LD15 (NM)	LAD19 (M) LD19 (NM)	ALE	VDD	LAD27 (M) LD27 (NM)	LBE1#	LBE3#	AD0	AD4	AD5	AD7
L	LAD3 (M) LD3 (NM)	LAD6 (M) LD6 (NM)	GPIO8	LAD13 (M) LD13 (NM)	LAD17 (M) LD17 (NM)	LAD22 (M) LD22 (NM)	LAD25 (M) LD25 (NM)	VSS	LAD31 (M) LD31 (NM)	VI/O	AD6	AD8	AD9	C/BE0#
K	LAD1 (M) LD1 (NM)	VDD	LAD2 (M) LD2 (NM)	LAD4 (M) LD4 (NM)	LAD5 (M) LD5 (NM)	MODE	BCLKo	LAD29 (M) LD29 (NM)	VSS	LEDon#	AD10	AD12	AD13	AD11
J	LA3	LAD0 (M) LD0 (NM)	LPMESET	LA2	VSS				VDD	C/BE1#	VSS	AD15	AD14	
H	LA8	LA5	LA6	LA7	LA4				SERR#	STOP#	PERR#	LOCK#	PAR	
G	LA11	VSS	LA9	BD_SEL# TEST	LA10				C/BE2#	TRDY#	IRDY#	FRAME#	DEVSEL#	
F	LA15	LA12	LA13	VDD	LA14				VSS	AD17	AD19	AD18	AD16	
E	LA17	VSS	LA16	LA18	WR#	LCLK	LREQ	EEDO	TRST#	IDSEL	AD23	AD21	AD20	VDD
D	LA20	LPMINT#	LA19	LA22	RD#	LRESETo#	GPIO0 WAITo#	GPIO2 CS2#	EEDI	PME#	AD30	AD24	C/BE3#	AD22
C	LA21	LA23	GPIO7 LA24	ADS#	READY#	CS0#	LINTi2	EECS	VSS	TDO	RST#	AD28	AD27	AD25
B	VSS	VDD	GPIO6 LA25	BLAST#	BTERM#	CS1#	LINTi1	GPIO3 CS3#	VDD	TMS	INTA#	AD29	VDD	AD26
A	NC	GPIO5 LA26	GPIO4 LA27	LW/R#	VSS	LGNT	GPIO1 LLOCKo#	EESK	TCK	TDI	PCLK	AD31	VSS	NC

Figure 13-6. 180-Pin µBGA Physical Layout with Pinout—Topside View

Table 13-5. 180-Pin µBGA Six-Layer Board Routing Example (Four Routing Layers)—Sample Parameters

Routing Layer Parameters	Via Size (mm)	Other Parameters	Via Size (mm)
Component Side	0.509	Land Pad Side	0.350
First Inside Layer	0.634	Solder Mask Opening	0.549
Second Inside Layer	0.634	Trace Width	0.127
Solder Side	0.634	Drill Size for the Via	0.254
		Hole Side for the Via	0.152

13—Physical Specs

Via

Solder Trace

Solder Pad
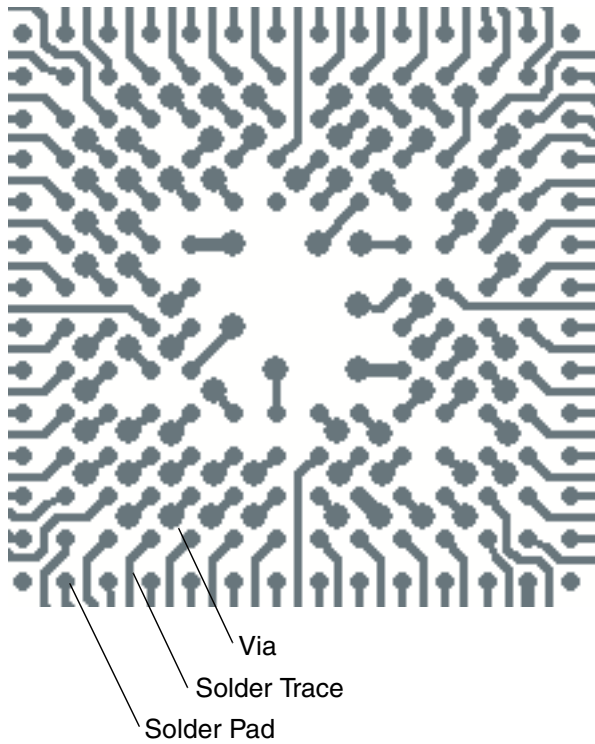
**Figure 13-7. 180-Pin µBGA Six-Layer Board Routing
Example (Four Routing Layers)—Component Side**
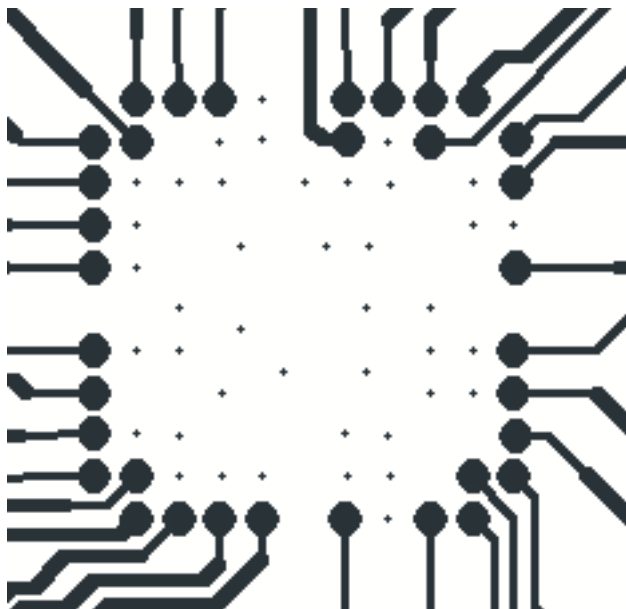
**Figure 13-8. 180-Pin µBGA Six-Layer Board Routing
Example (Four Routing Layers)—First Inside Layer**
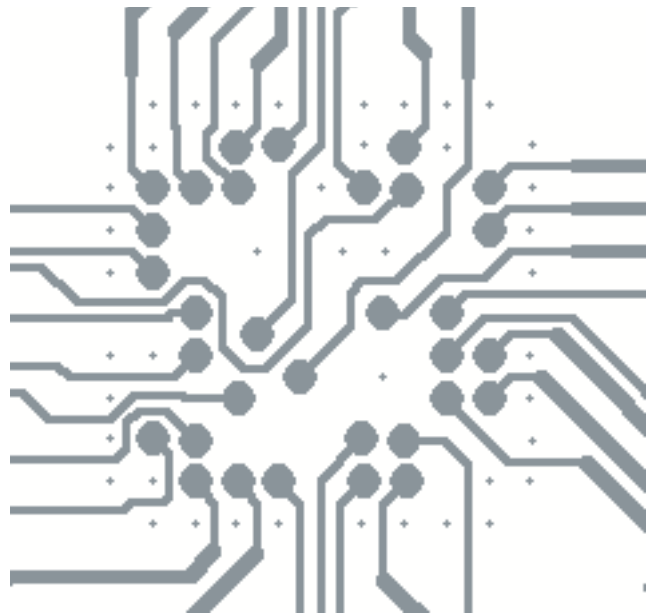
**Figure 13-9. 180-Pin µBGA Six-Layer Board
Routing Example (Four Routing Layers)—
Second Inside Layer**
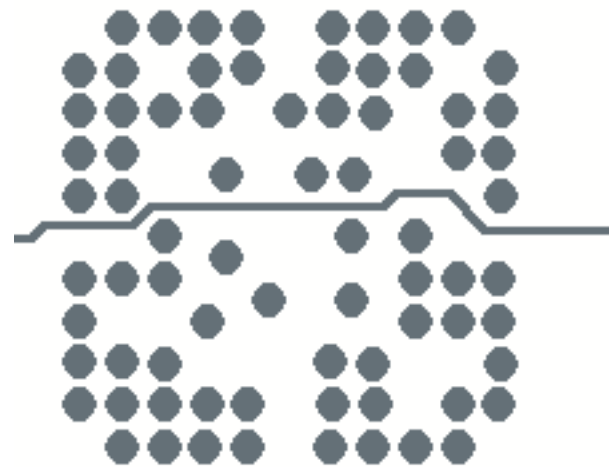
**Figure 13-10. 180-Pin µBGA Six-Layer Board Routing
Example (Four Routing Layers)—Solder Side**

A   GENERAL INFORMATION

The PCI 9030 is a 32-bit, 33-MHz PCI Bus Target Interface Device featuring advanced SMARTarget technology, which includes a programmable Target interface. The PCI 9030 offers 3.3, 5V tolerant PCI and Local signaling, supports Universal PCI Adapter designs, 3.3V core, low-power CMOS offered in two package options—176-pin PQFP and 180-pin (ball) µBGA. The device is designed to operate at Industrial Temperature range.

A.1   ORDERING INSTRUCTIONS

Continuing its drive to provide single-chip PCI interfaces for every market, PLX offers to designers its PCI 9030 PCI SMARTarget *PICMG 2.1, R2.0* PI = 0 compliant, I/O accelerator for adapters and embedded systems.

Table A-1. Available Packages

Package	Ordering Part Number
176-pin PQFP	PCI 9030-AA60PI
180-pin µBGA	PCI 9030-AA60BI

A.2   UNITED STATES AND INTERNATIONAL REPRESENTATIVES, AND DISTRIBUTORS

A list of PLX Technology, Inc., representatives and distributors can be found at http:⁄ ⁄ www.plxtech.com.

A.3   TECHNICAL SUPPORT

PLX Technology, Inc., technical support information is listed at http:⁄ ⁄ www.plxtech.com, or call 408 774-9060 or 800 759-3735.

A—General Info

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A

B