CM-A510 CoM

Reference Guide

CompuLab

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Table 1 Revision Notes

Date	Description
November 2010	First release

Please check for a newer revision of this manual at CompuLab's web site – http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site to those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab's CM-A510 Computer-on-Module.

1.2 CM-A510 Part Number Legend

For CM-A510 part number legend, please refer to the 'Prices' section at CompuLab website: http://www.compulab.co.il/a510/html/a510-cm-price.htm.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CM-A510 Product Developer Resources	http://www.compulab.co.il/
88AP510 Functional Specifications	
88AP510 Hardware Specifications	

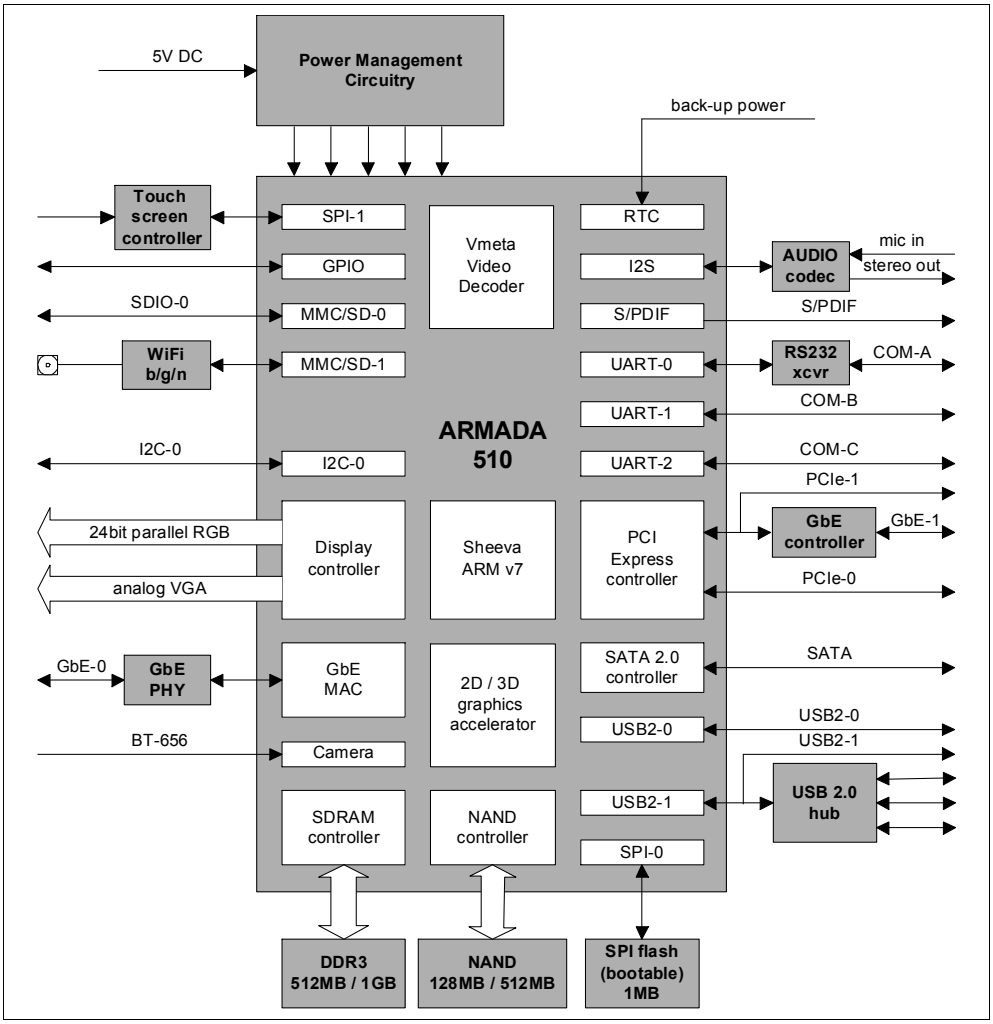
2 OVERVIEW

2.1 Highlights

• Marvell® ARMADA™ 510 CPU, dual issue ARMv7, up to 1000 MHz • Up to 1024 Mbyte DDR3 • Up to 512 Mbyte Flash Disk, including file-system protection • WLAN / WiFi 802.11b/g/n Interface • Graphics controller supporting parallel RGB and VGA interfaces with HD 1080p maximum resolution and dual-head operation • H.264, MPEG-4, MPEG-2, VC-1and additional video codecs implemented by the VMeta subsystem • Integrated GPU providing 2D / 3D graphics acceleration with OpenGL-ES support • SATA-II hard disk interface • 2 x 1000 BaseT Ethernet ports • 4 x high-speed USB ports • PCI Express interface • SDIO / MMC interface • Camera Interface port • Audio sub-system with speaker, microphone and S/PDIF support • Touch-screen Controller • Serial ports, I2C, GPIO • Low standby and active power consumption • Small size: 75 x 65 x 8 mm	The CM-A510 is a small Computer-on-Module board designed to serve as a building block in embedded applications. The CM-A510 has all the components required to run most up to date Linux-based operating systems. Ready-to-run packages are available from CompuLab. The small size and low power consumption of the CM-A510 allows its integration into portable and space-constrained designs, while its low price makes it an ideal selection for cost-sensitive applications. The CM-A510 delivers fast processing and a rich multimedia user experience, in a low-power design that offers fast Internet browsing, HD video playback, 3D graphics and high-speed connectivity. CM-A510 is based on a high-performance, low-power Marvell® ARMADA™ 510 system-on-chip with an ARM v6/v7-compliant superscalar processor core, hardware graphics processing unit, video decoding acceleration hardware and a broad range of peripherals. For embedded applications, the CM-A510 provides a variety of display interfaces, PCI Express bus, two Gigabit Ethernet ports, high-speed USB ports, SATA interface, serial ports, general-purpose I/O lines and many other essential functions. The user interface is supported by an enhanced graphics controller, USB interface for keyboard/mouse and audio sub-system.

2.2 Block Diagram

Figure 1 CM-A510 Block Diagram



2.3 CM-A510 Features

The "Option" column specifies the configuration code required to have the particular feature. "+" means that the feature is always available.

Table 3 CPU, Memory and Busses

Feature	Specifications	Option
CPU	Marvell Armada 510 CPU, 800 / 1000 MHz ARMv7 architecture, integrated FPU, WMMX2 L1 cache: 32 KB (I-Cache), 32 KB (D-Cache) L2 cache: 512 KB DMA, Interrupt controller, Timers	C
RAM	512 - 1024 MB, DDR3, 533 MHz, 32-bit	D
NAND Flash Disk	128 - 512 Mbytes	N
Boot Flash	1 MB, bootable	+
PCI Express bus	PCI Express Base Specification, Revision 1.1. One or two lanes. Note: second lane is shared with optional second Ethernet controller	+

Table 4 Peripherals

Feature	Specifications	Option
Graphics Controller	16/18/24 bit color, resolution up to 1920 x 1080, frame buffer in system DDR. Display types support: TFT (parallel RGB), analog VGA. Dual-head support.	+
Video acceleration	VMeta video decode subsystem running at rate up to 500 MHz. Supporting H.264, MPEG-4, MPEG-2 and VC-1. Part of Armada 510 SoC.	+
2D / 3D graphics	Integrated GPU providing 2D / 3D graphics acceleration with OpenGL-ES support. Part of Armada 510 SoC.	+
USB	Two Host / Slave USB2 high-speed port, 480 Mbps	U2
	Additional 2 x USB2 high-speed host ports, 480 Mbps	U4
Gigabit Ethernet	Armada 510 integrated MAC + RTL8211D PHY, 10/100/1000BaseT, activity LED's	E1
	Realtek RTL8111 controller, 10/100/1000BaseT, activity LED's	E2
SATA interface	Armada 510 integrated SATA-II controller + PHY, 3Gb/s speed	+
Serial Ports (UARTs)	3 UART ports, 16550 compatible: COM-A – RS232 interface, partial modem controls, 250 Kbps COM-B – 3.3V interface, Rx / Tx only, 900 Kbps COM-C – 3.3V interface, partial modem controls, 900 Kbps	+
Camera Interface	Direct camera sensor support, max resolution 1920 x 1080, pixel clock up to 50MHz. ITU BT.656, digital RGB/YCbCr interface.	+
General Purpose I/O	Up to 38 lines shared with other functions. Can also be used as interrupt inputs.	+
Keyboard & mouse	USB or redirection from COM port	+
MMC / SD	MMC / SD / SDIO support including SDHC up to 32GB	+
Audio	I2S compliant audio codec, stereo output, stereo line-in, differential mic input.	A
	S/PDIF output, consumer mode IEC 60958-3	+
Touchscreen ctrl.	TSC2046 touchscreen controller. Supports 4-wire resistive panels	I
RTC	Real Time Clock, powered by external lithium battery	+
WiFi Interface	Implements 802.11b/g/n wireless connectivity standard. Broadcom 4319 802.11b/g/n chipset. On-board connector for external antenna.	W

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	Single 5V DC
Active power consumption	2 – 5 W, depending on configuration and CPU speed
Standby/Sleep consumption	50 - 200 mW, depending on configuration and mode
Dimensions	75 x 65 x 8 mm
Weight	31 gram
MTBF	> 100,000 hours

Operation temperature (case)	Commercial: 0º to 70º C Extended: -20º to 70º C Industrial: -40º to 85º C
Storage temperature	-40º to 85º C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm
Connector insertion / removal	50 cycles

3 CORE SYSTEM COMPONENTS

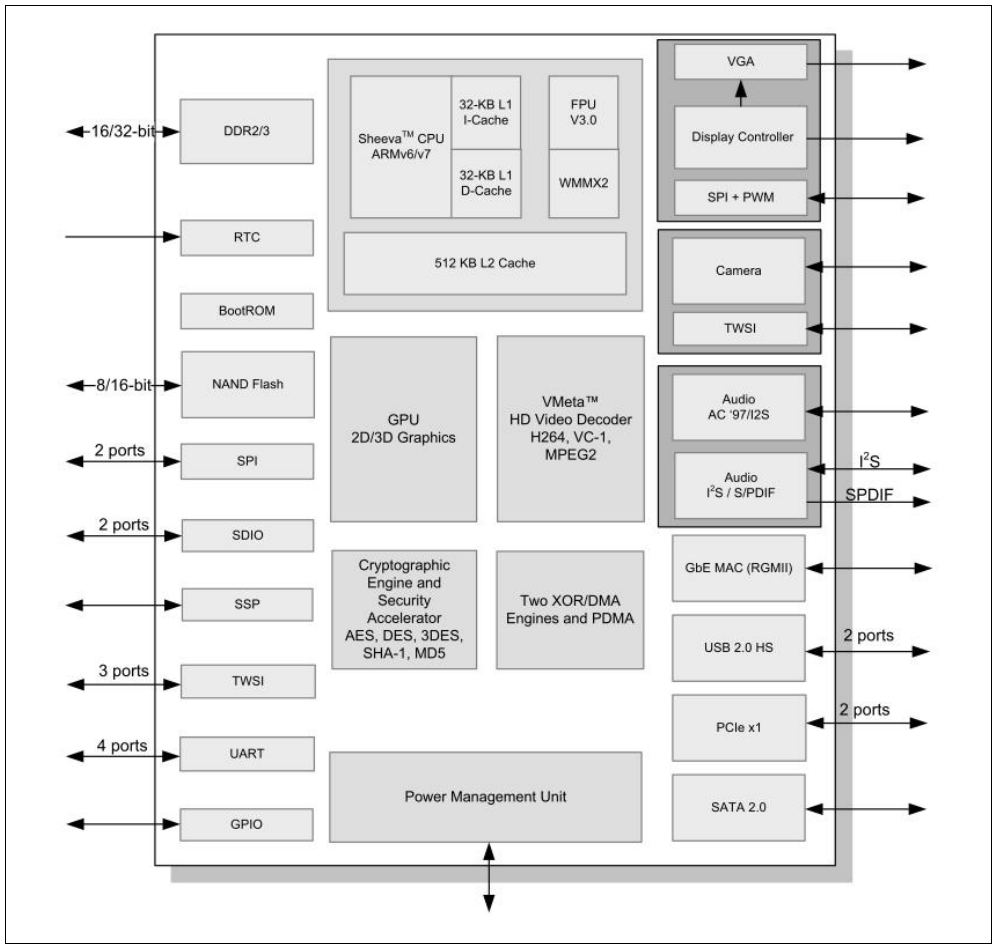
3.1 Armada 510 SoC

The Marvell Armada 510 is a high-performance, highly integrated, low-power SoC with a high-end ARM-compatible processor, a graphics processing unit, high definition video decoding acceleration hardware and a broad range of peripherals. The Armada 510 integrates an ARMv6/v7-compliant, high-speed, dual-issue Sheeva CPU core with double precision integrated Floating Point Unit (FPU) and WMMX2 coprocessor, 32-KB L1 Data cache, 32-KB instruction cache and 512-KB L2 cache. It also includes an advanced power management unit, an advanced 2D/3D graphics processing unit, display controllers and a high-definition video decoder.

The Armada 510 integrates the following hardware engines to enhance performance:

- High-definition Video Decoding Unit (VMeta)
- 2D/3D Graphics Processing Unit (GPU)
- Power Management Unit supporting SoC low power states, Dynamic Frequency Scaling (DFS) and Dynamic Voltage Scaling (DVS)
- Two XOR DMA engines and 16-channel peripheral DMA controller

Figure 2 Armada 510 Block Diagram



3.2 Multimedia System

3.2.1 Video Decode Unit (VMeta)

The Video Decode unit decodes the compressed video elementary stream to produce the reconstructed video frames for display or further processing.

VMeta supports the following video formats:

- H.264 MP/HP @L4.1 with arbitrary slice order
- VC1 AP @L3, MP @HL
- MPEG2 MP @HL
- DivX HD Compliant MPEG4
- AVS

For additional details, please refer to section 9 of the "88AP510 Functional Specifications".

3.2.2 Graphics Processing Unit

The Graphics Processing Unit (GPU) is a low-power, high-performance 2D/3D graphics core designed to support the OpenGL-ES 2.0 Graphics Processing standards.

The Armada 510 GPU provides support for the following imaging and video features:

3D Features:

- OpenGL ES 1.1/2.0 compliant
- 32-bit floating point pipeline including shaders
- Up to eight programmable elements per vertex
- Unified vertex and pixel shaders
- Dependent texture operation with high-performance
- Alpha blend
- Support for eight simultaneous pixel textures and four simultaneous vertex textures
- Point sampling, bi-linear sampling, tri-linear sampling, and cubic textures
- Multi-sample Anti-aliasing

2D Features:

- Bit, stretch, pattern blits and fast clear
- Line drawing
- Rectangle fill
- Mono expansion for text rendering
- ROP2, ROP3, ROP4
- Alpha blending
- 90-/180-/270-degree rotation
- Video data format conversion
- High-quality scaling

For additional details, please refer to section 10 of "88AP510 Functional Specifications".

3.3 Memory

3.3.1 DRAM

The CM-A510 board is assembled with 512 or 1024 Mbytes of DDR3. The DRAM interface is 32-bits wide and runs with a 533 MHz clock.

3.3.2 SPI Flash

The CM-A510 is assembled with 1 Mbyte of SPI NOR flash.

The SPI NOR flash is the primary non-volatile memory device of the CM-A510, used for the boot-loader and configuration blocks storage.

3.3.3 NAND Flash

The CM-A510 is assembled with 128 or 512 Mbytes of SLC NAND Flash.

The NAND Flash is the secondary non-volatile memory device of the CM-A510, used for OS storage and flash drive implementation.

4 PERIPHERAL INTERFACES

The CM-A510 implements a number of peripheral interfaces through the interface connectors (P1 and P2). The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options. Each signal's availability is noted in the "Signal description" table of each interface.
- Certain interface pins can be configured as one of several signals. For pin multiplexing characteristics, please refer to chapter 5.5.
- Certain signals are available on more than one interface pin. Only one interface pin can be used for each signal.
- All of the CM-A510 digital interfaces operate at 3.3V CMOS voltage levels, unless otherwise noted.
- Certain software-configurable multi-purpose signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Signals within a group cannot be configured separately for different functions. Signal configuration grouping is noted in the "Signal description" table of each interface.

The signals for each interface are described in the "Signal description" tables. The following notes summarize the column headers for these tables:

- **"Signal name"** – The symbolic name of each signal.
- **"Pin#" –** The pin number on the interface connector.
- **"Type" –** Signal type.
- **"Description" –** Signal description.
- **"Availability" –** Certain signals are not available with/without certain configuration options. This column summarizes configuration requirements for each signal.

Each interface signal can be one of the following types. Signal type is noted in the "Signal description" tables for each signal

- **"O"** – Digital output.
- **"I"** – Digital input.
- **"IO"** – Digital Input/Output.
- **"AO"** – Analog Output.
- **"AI"** – Analog Input.
- **"OD"** – Open Drain Signal (not pulled up on the CM-A510 unless otherwise noted).
- **"IPU"** – Open Drain Signal (pulled up on the CM-A510 unless otherwise noted).

4.1 Display Interface

The CM-A510 display sub-system is based on the display controller of the Armada 510 SoC.

The display sub-system incorporates two independent display controllers supporting dual-head operation and features two separate display interfaces:

- 24-bit parallel RGB
- Analog VGA.

The display subsystem supports the following main features:

Display controller

- Programmable pixel display modes (12, 16, 18 and 24 bits-per-pixel)
- Programmable resolution of up to 1920 x 1080
- Overlay and image scaling for video and graphics
- Hardware cursor
- Rotation of 90-, 180- and 270-degrees

For additional details, please refer to section 11 of the "88AP510 Functional Specifications".

Table 6 Display interface signals

Signal Name	Pin #	Type	Description				
Parallel RGB							
LCD_PCLK	P1-108	O	Pixel clock				
LCD_HSYNC	P1-109	O	Horizontal synchronization				
LCD_VSYNC	P1-107	O	Vertical synchronization				
LCD_E	P1-105	O	Pixel data enable				
				RGB444 mode	RGB565 mode	RGB666 mode	RGB888 mode
LCD_D0	P1-75	O	Pixel data bit 0	Red[4]	Red[3]	Red[2]	Red[0]
LCD_D1	P1-76	O	Pixel data bit 1	Red[5]	Red[4]	Red[3]	Red[1]
LCD_D2	P1-77	O	Pixel data bit 2	Red[6]	Red[5]	Red[4]	Red[2]
LCD_D3	P1-78	O	Pixel data bit 3	Red[7]	Red[6]	Red[5]	Red[3]
LCD_D4	P1-81	O	Pixel data bit 4	Green[4]	Red[7]	Red[6]	Red[4]
LCD_D5	P1-82	O	Pixel data bit 5	Green[5]	Green[2]	Red[7]	Red[5]
LCD_D6	P1-83	O	Pixel data bit 6	Green[6]	Green[3]	Green[2]	Red[6]
LCD_D7	P1-84	O	Pixel data bit 7	Green[7]	Green[4]	Green[3]	Red[7]
LCD_D8	P1-85	O	Pixel data bit 8	Blue[4]	Green[5]	Green[4]	Green[0]
LCD_D9	P1-87	O	Pixel data bit 9	Blue[5]	Green[6]	Green[5]	Green[1]
LCD_D10	P1-88	O	Pixel data bit 10	Blue[6]	Green[7]	Green[6]	Green[2]
LCD_D11	P1-89	O	Pixel data bit 11	Blue[7]	Blue[3]	Green[7]	Green[3]
LCD_D12	P1-90	O	Pixel data bit 12	-	Blue[4]	Blue[2]	Green[4]
LCD_D13	P1-92	O	Pixel data bit 13	-	Blue[5]	Blue[3]	Green[5]
LCD_D14	P1-93	O	Pixel data bit 14	-	Blue[6]	Blue[4]	Green[6]
LCD_D15	P1-94	O	Pixel data bit 15	-	Blue[7]	Blue[5]	Green[7]
LCD_D16	P1-95	O	Pixel data bit 16	-	-	Blue[6]	Blue[0]
LCD_D17	P1-96	O	Pixel data bit 17	-	-	Blue[7]	Blue[1]
LCD_D18	P1-97	O	Pixel data bit 18	-	-	-	Blue[2]
LCD_D19	P1-99	O	Pixel data bit 19	-	-	-	Blue[3]
LCD_D20	P1-100	O	Pixel data bit 20	-	-	-	Blue[4]
LCD_D21	P1-101	O	Pixel data bit 21	-	-	-	Blue[5]
LCD_D22	P1-102	O	Pixel data bit 22	-	-	-	Blue[6]
LCD_D23	P1-104	O	Pixel data bit 23	-	-	-	Blue[7]
VGA							
VGA_R	P1-28	AO	Red video signal				
VGA_G	P1-30	AO	Green video signal				
VGA_B	P1-32	AO	Blue video signal				
VGA_HSYNC	P1-34	O	Horizontal synchronization				
VGA_VSYNC	P1-36	O	Vertical synchronization				

4.2 Gigabit Ethernet

The CM-A510 incorporates up to two full-featured Gigabit Ethernet interfaces.

4.2.1 Primary Gigabit Ethernet

The CM-A510 primary Gigabit Ethernet interface is implemented with the Armada 510 Gigabit Ethernet controller and an on-board RTL8211D Realtek PHY. The interface supports the following main features:

- Fully compliant with IEEE 802.3 standard
- 1000 Mbps operation – full duplex
- 10 / 100 Mbps operation – half and full duplex
- Crossover Detection and Auto-Correction
- Auto-negotiation
- Activity and speed indicator LED controls

Table 7 Primary Gigabit Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
LAN0_MDIP0	P1-2	IO	First pair in 1000Base-T / transmit pair in 10Base-T and 100Base-T.	Only available **with** either 'E1' or 'E2' configuration options.
LAN0_MDIN0	P1-4	IO		
LAN0_MDIP1	P1-1	IO	Second pair in 1000Base-T / receive pair in 10Base-T and 100Base-T.	
LAN0_MDIN1	P1-3	IO		
LAN0_MDIP2	P1-10	IO	Third pair in 1000Base-T.	
LAN0_MDIN2	P1-12	IO		
LAN0_MDIP3	P1-9	IO	Forth pair in 1000Base-T.	
LAN0_MDIN3	P1-11	IO		
LAN0_LED0	P1-6	O	Activity LED output. Active low.	
LAN0_LED1	P1-5	O	10 / 100 / 1000 LED output.	
LAN0_LED2	P1-13	O	10 / 100 / 1000 + activity LED output.	

NOTE: The primary Gigabit Ethernet interface is available only with either 'E1' or 'E2' configuration options.

NOTE: For magnetics' selection recommendations, please refer to section 8.3 of this document.

4.2.2 Secondary Gigabit Ethernet

The CM-A510 secondary Gigabit Ethernet interface is implemented with the RTL8111D Realtek Gigabit Ethernet controller. The controller is connected to the PCIe-1 interface of the Armada 510 SoC. The interface supports the following main features:

- Fully compliant with IEEE 802.3 standard
- Crossover Detection and Auto-Correction
- Auto-negotiation
- Activity and speed indicator LED controls

Table 8 Secondary Gigabit Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
LAN1_MDIP0	P2-2	IO	First pair in 1000Base-T / transmit pair in 10Base-T and 100Base-T	Only available **with** the 'E2' configuration option.
LAN1_MDIN0	P2-4	IO		
LAN1_MDIP1	P2-1	IO	Second pair in 1000Base-T / receive pair in 10Base-T and 100Base-T	
LAN1_MDIN1	P2-3	IO		
LAN1_MDIP2	P2-10	IO	Third pair in 1000Base-T	
LAN1_MDIN2	P2-12	IO		
LAN1_MDIP3	P2-9	IO	Forth pair in 1000Base-T	
LAN1_MDIN3	P2-11	IO		
LAN1_LED0	P2-6	O	Link 10 + activity LED output	
LAN1_LED1	P2-5	O	Link 100 + activity LED output	
LAN1_LED2	P2-13	O	Link 10 / 100 / 1000 + activity LED output.	

NOTE: The primary Gigabit Ethernet interface is available only with the 'E2' configuration option.

NOTE: For magnetics' selection recommendations, please refer to section 8.3 of this document.

4.3 PCI Express

The CM-A510 features up to two PCI Express ports implemented with the Armada 510 PCI Express controller. PCIe-0 port is always available. PCIe-1 port is multiplexed with the secondary Gigabit Ethernet interface. The PCI Express interface provides the following features:

- PCI Express Base 1.1 compatible
- Root complex port
- 2.5 GHz signaling

For additional details, please refer to section 20 of "88AP510 Functional Specifications".

Table 9 PCI Express interface signals

Signal Name	Pin #	Type	Description	Availability
PCIe-0 Interface				
PCIE0_TX_P	P2-114	O	PCI Express transmit data pair	Always available.
PCIE0_TX_N	P2-112	O		
PCIE0_RX_P	P2-108	I	PCI Express receive data pair	
PCIE0_RX_N	P2-106	I		
PCIE0_CLK_P	P2-101	O	PCI Express reference clock pair	
PCIE0_CLK_N	P2-99	O		
PCIE0_nCLKREQ	P2-17	IO	PCI Express clock request input	
PCIe-1 Interface				
PCIE1_TX_P	P2-113	O	PCI Express transmit data pair	Only available **without** the 'E2' configuration option.
PCIE1_TX_N	P2-111	O		
PCIE1_RX_P	P2-107	I	PCI Express receive data pair	
PCIE1_RX_N	P2-105	I		
PCIE1_CLK_P	P2-83	O	PCI Express reference clock pair	
PCIE1_CLK_N	P2-81	O		
PCIE1_nCLKREQ	P2-15	IO	PCI Express clock request input	

NOTE: PCIe-1 interface is available only without the 'E2' configuration option.

4.4 SATA

The CM-A510 incorporates a single SATA-II port implemented with the Armada 510 SATA-II controller. The interface supports the following main features:

- Fully compatible with the SATA-II phase 1.0 specification
- SATA-II 3 Gb/s data rate
- SATA-II power management compliant
- SATA-II device hot-swap compliant
- SATA-II Native Command Queuing (NCQ)

For additional details, please refer to section 21 of the "88AP510 Functional Specifications".

Table 10 SATA-II interface signals

Signal Name	Pin #	Type	Description	Availability
SATA_TX+	P2-126	O	SATA-II transmit data pair.	Always available.
SATA_TX-	P2-124	O		
SATA_RX+	P2-120	I	SATA-II receive data pair.	
SATA_RX-	P2-118	I		

4.5 USB 2.0

The CM-A510 provides up to four USB 2.0 ports implemented with the Armada 510 USB sub-system and an optional on-board USB 2.0 hub. The USB 2.0 interface provides the following features:

- Complies with EHCI (high-speed host controller)
- Complies with OHCI (low-speed/full-speed host controller)
- Complies with the USB 2.0 standard for high-speed (480M bit/s) functions

Table 11 USB 2.0 Host interface signals

Signal Name	Pin #	Type	Description	Availability
USB0 interface				
USB0_DP	P2-132	AOI	USB port 0 positive data	Only available **with** either 'U2' or 'U4' configuration options.
USB0_DN	P2-130	AOI	USB port 0 negative data	
USB1 interface				
USB1_DP	P2-138	AOI	USB port 1 positive data	Only available **with** either 'U2' or 'U4' configuration options.
USB1_DN	P2-136	AOI	USB port 1 negative data	
USB1_CPEN	P1-128	O	USB port 1 external 5V supply enable. Active high.	Only available **with** 'U4' configuration option.
USB1_nOVC	P2-140	IPU	USB port 1 over current sense.	
USB2 interface				
USB2_DP	P1-131	AOI	USB port 2 positive data	Only available **with** the 'U4' configuration option.
USB2_DN	P1-129	AOI	USB port 2 negative data	
USB2_CPEN	P1-126	O	USB port 2 external 5V supply enable. Active high.	
USB2_nOVC	P2-138	IPU	USB port 2 over current sense.	
USB3 interface				
USB3_DP	P1-137	AOI	USB port 3 positive data	Only available **with** the 'U4' configuration option.
USB3_DN	P1-135	AOI	USB port 3 negative data	
USB3_CPEN	P1-133	O	USB port 3 external 5V supply enable. Active high.	
USB3_nOVC	P2-136	IPU	USB port 3 over current sense.	

NOTE: Four USB ports are available only with the 'U4' configuration option.

4.6 WLAN

The CM-A510 incorporates full-featured 802.11 b/g/n capabilities, implemented with the USI WM-N-BM-01 WLAN controller module. The WM-N-BM-01 is a complete IEEE 802.11b/g/n solution based on the Broadcom 4319 chipset.

The CM-A510 WLAN interface supports the following security features:

- WEP (64 bit/128 bit)
- WPA TKIP
- WPA2

The WM-N-BM-01 is connected to the Armada SoC via the SD-1 port.

Antenna Connection

The WM-N-BM-01 requires a single 2.45GHz antenna. The antenna is connected via the onboard UFL high frequency connector J1. Any type of 2.45GHz WLAN antenna can be used. Please refer to section 6.3 for connector location.

Table 12 J1 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

Table 13 802.11b/g/n RF system specifications

Parameter	Test Condition	Typical Value	Units
Frequency Band		2.400 – 2.497	GHz
Maximum receive level	PER < 8%	-10	dBm
Transmit Power Output	1, 2, 5.5, 11 Mbps	17	dBm
	6, 9 Mbps	15	dBm
	11n (HT20)	14	dBm
	11n (HT40)	14	dBm
Wide-band Noise	@ 869MHz ~ 960MHz	-160	dBm/Hz
	@ 1800MHz ~ 1990MHz	-160	dBm/Hz
	@ 2110MHz ~ 2170MHz	-150	dBm/Hz
Error Vector Magnitude	@ 1 Mbps	-13	dB
	@ 6 Mbps	-30	dB
	@ 11 Mbps	-13	dB
	@ 54 Mbps	-30	dB
	@ MCS7	-30	dB
	@ MCS0	-30	dB
Receive Sensitivity	1 Mbps, 8% PER	-94	dBm
	6 Mbps, 10% PER	-86	dBm
	11 Mbps, 8% PER	-87	dBm
	54 Mbps, 10% PER	-73	dBm
	65 Mbps, 10% PER	-72	dBm
	135 Mbps, 10% PER	-68	dBm

4.7 Audio

4.7.1 Analog Audio

The CM-A510 analog audio subsystem is implemented with Texas Instruments TLV320AIC23b audio codec. The analog audio subsystem supports the following features:

- Single ended stereo-line output
- Single ended stereo-line input
- Integrated electret-microphone biasing and buffering solution
- 8-kHz – 96-kHz Sampling-Frequency Support
- 100-dB SNR Multibit Sigma-Delta DAC (A-weighted at 48 kHz)
- 90-dB SNR Multibit Sigma-Delta ADC (A-weighted at 48 kHz)

Table 14 Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		
	Rload = 16Ω			40		
Signal-to-noise ratio, A-weighted (see Note 2)			90	97		dB
Total harmonic distortion	1kHz output	Pout = 10mW			0.1	%
		Pout = 20mW			1.0	%
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
Programmable gain	1 kHz output		-73		6	
Programmable-gain step size				1		
Mute attenuation	1 kHz output			80		
Line Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 1 and 2)	Fsample = 48 kHz.		85	90		dB
Dynamic range, A-weighted, −60-dB full-scale input (see Note 2)			85	90		dB
Total harmonic distortion, −1-dB input, 0-dB gain				-80		dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
ADC Channel Separation	1 kHz input tone			90		dB
Programmable-gain step size	Monotonic			1.5		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance	12 dB input gain		10		20	kΩ
	0 dB input gain		30	35		
Input capacitance				10		pF
Microphone Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 1 and 2)			80	85		dB
Dynamic range, A-weighted, −60-dB full-scale input (see Note 2)			80	85		dB
Total harmonic distortion, −1-dB input, 0-dB gain				-60		dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
Mute attenuation	0dB, 1 kHz input tone		60	80		dB
Input resistance			8		14	kΩ
Input capacitance				10		pF

Microphone Bias					
Bias voltage		2.375	2.475	2.575	V
Bias-current source				3	mA

For additional details, please refer to the TLV320AIC23B datasheet, available from Texas Instruments.

Table 15 Analog audio signals

Signal Name	Pin #	Type	Description	Availability
AUDIO_OUT_R	P2-139	AO	Right stereo mixer-channel amplified headphone output	Only available **with** the 'A' configuration option.
AUDIO_OUT_L	P2-137	AO	Left stereo mixer-channel amplified headphone output	
AUDIO_IN_R	P2-131	AI	Right stereo line input	
AUDIO_IN_L	P2-133	AI	Left stereo line input	
MIC_IN	P2-129	AI	Buffered amplifier input suitable for use with electret-microphone	
MIC_BIAS	P2-125	O	Microphone bias output, suitable for electret-microphone biasing, 2.475V nominal voltage.	
AUDIO_GND	P2-123	P	Dedicated analog audio ground	

NOTE: The analog audio interface is available only with the 'A' configuration option.

4.7.2 I2S

The CM-A510 I2S interface is implemented with the Armada 510 I2S controller. The interface supports the following main features:

- Plain I2S, right-justified and left-justified formats
- An audio sample rate of 44.1/48/96 kHz
- Sample sizes of 16-bit, 20-bit, 24-bit and 32-bit.

For additional details, please refer to section 12 of "88AP510 Functional Specifications".

Table 16 I2S signals

Signal Name	Pin #	Type	Description	Availability	Configuration Group
I2S1_BCLK	P2-45	O	Bit clock	Always available.	Digital Audio
I2S1_DI	P2-47	I	Receiver data in		
I2S1_DO	P2-49	O	Transmitter data out		
I2S1_LRCLK	P2-51	O	Left/right clock		
I2S1_MCLK	P2-53	O	Master clock		

NOTE: I2S signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

NOTE: I2S signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Individual I2S signals cannot be configured separately for different functions.

4.7.3 S/PDIF

The CM-A510 features an S/PDIF interface implemented with the Armada 510 S/PDIF controller. The interface supports the following main features:

- Compliant with the IEC60958-1, IEC60958-3 and IEC61937 specifications
- An audio sample rate of 44.1/48/96 kHz
- Sample sizes of 16-bit, 20-bit, 24-bit and 32-bit.

For additional details, please refer to section 12 of the "88AP510 Functional Specifications".

Table 17 S/PDIF signals

Signal Name	Pin #	Type	Description	Availability
S/PDIF	P2-41	O	S/PDIF transmitter data out	Always available.

NOTE: S/PDIF signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

4.8 UART's

The CM-A510 incorporates three general purpose UART's. The following features are supported:

- 16550 compatibility
- 16-byte FIFO for receiver and 16-byte FIFO for transmitter
- Programmable baud rate of up to 900 Kbps
- Configurable data format

Table 18 UART signals

Signal Name	Pin #	Type	Description	Availability	Configuration Group
UART-1					
UART1_TXD	P1-114	O	UART serial data out	Always available.	UART1
UART1_RXD	P1-112	I	UART serial data in		
UART-2					
UART2_TXD	P1-64	O	UART serial data out	Always available.	Each pin is configured separately.
UART2_RXD	P1-66	I	UART serial data in		
UART-3					
UART3_TXD	P1-72	O	UART serial data out	Always available.	Each pin is configured separately.
UART3_RXD	P1-61	I	UART serial data in		
UART3_CTS	P1-70	O	UART clear to send		
UART3_RTS	P1-68	I	UART request to send		

NOTE: UART signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

NOTE: UART-1 signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Individual UART-1 signals cannot be configured separately for different functions.

4.9 RS232

The CM-A510 incorporates a single RS232 port. The following features are supported:

- 16550 compatibility
- 16-byte FIFO for receiver and 16-byte FIFO for transmitter
- Programmable baud rate of up to 250 Kbps
- Configurable data format
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from UART-0 of the Armada 510 SoC.

NOTE: The RS232 port operates at RS232 voltage levels.

Table 19 RS232 signals

Signal Name	Pin #	Type	Description	Availability
RS232_TXD	P1-119	O	RS232 serial data out	Always available.
RS232_RXD	P1-117	I	RS232 serial data in	
RS232_CTS	P1-123	I	RS232 clear to send	
RS232_RTS	P1-121	O	RS232 request to send	

4.10 MMC / SD / SDIO

The CM-A510 features two multimedia card high-speed/secure data/secure digital I/O (MMC / SD / SDIO) host interfaces. The following main features are supported:

- 1-bit/4-bit SD memory, SDIO and MMC cards
- Up to 50MHz (SD PHY rev 1.1 high speed)
- SDHC (SD PHY rev 2.0)
- DMA and PIO operation

For additional details, please refer to section 23 of "88AP510 Functional Specifications".

NOTE: MMC/SD/SDIO signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

NOTE: MMC/SD/SDIO signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Individual signals cannot be configured separately for different functions.

Table 20 MMC/SD/SDIO signals

Signal Name	Pin #	Type	Description	Availability	Configuration Group
SD-0					
SD0_DATA0	P2-54	IO	Data signal 0	Always available.	SD-0
SD0_DATA1	P2-56	IO	Data signal 1		
SD0_DATA2	P2-58	IO	Data signal 2		
SD0_DATA3	P2-60	IO	Data signal 3		
SD0_CMD	P2-78	IO	Command signal		
SD0_CLK	P2-76	O	Clock output		
SD0_CD	P1-68	I	Card detection input	Always available.	Each pin is configured separately.
SD0_WP	P1-70	I	Card write protection input		
SD-1					
SD1_DATA0	P2-61	IO	Data signal 0	Only available **without** the 'W' configuration option.	SD-1
SD1_DATA1	P2-63	IO	Data signal 1		
SD1_DATA2	P2-65	IO	Data signal 2		
SD1_DATA3	P2-69	IO	Data signal 3		
SD1_CMD	P2-75	IO	Command signal		
SD1_CLK	P2-73	O	Clock output		

4.11 Touch-Screen

The CM-A510 features a resistive touch-screen interface. The interface supports 4-wire touch panels. The touch-screen controller is connected to the SPI-1 interface of the Armada 510 SoC.

Table 21 Touch-screen signals

Signal Name	Pin #	Type	Description	Availability
TS_X+	P1-23	AI	Touch screen X+ (right)	Only available **with** the 'I' configuration option.
TS_X-	P1-21	AI	Touch screen X- (left)	
TS_Y+	P1-29	AI	Touch screen Y+ (top)	
TS_Y-	P1-27	AI	Touch screen Y- (bottom)	

4.12 GPIO

The CM-A510 provides up to 44 GPIO signals. These signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to section 28 of "88AP510 Functional Specifications".

NOTE: GPIO signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

NOTE: Certain GPIO signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Individual signals cannot be configured separately for different functions.

Table 22 GPIO signals

CM-A510 signal	Armada 510 signal	Availability	Configuration Group
P1-64	GPIO_14	Available with all configurations. Muxed with UART-2, SSP.	Each pin is configured separately.
P1-66	GPIO_15	Available with all configurations. Muxed with UART-2.	
P1-68	GPIO_16	Available with all configurations. Muxed with UART-3, SD-0.	
P1-70	GPIO_17	Available with all configurations. Muxed with UART-3, SD-0, I2C-2.	
P1-72	GPIO_18	Available with all configurations. Muxed with UART-3, SD-0.	
P1-61	GPIO_19	Available with all configurations. Muxed with UART-3, I2C-2.	
P1-63	GPIO_20	Only available **without** 'I' option. Muxed with SPI-1, SD-0.	
P1-65	GPIO_21	Only available **without** 'I' option. Muxed with SPI-1, SD-0, SSP.	
P1-69	GPIO_22	Only available **without** 'I' option. Muxed with SPI-1, SSP.	
P1-71	GPIO_23	Only available **without** 'I' option. Muxed with SPI-1, SSP.	
P1-40	GPIO_24	Available with all configurations. Muxed with camera interface.	Camera
P1-42	GPIO_25	Available with all configurations. Muxed with camera interface.	
P1-44	GPIO_26	Available with all configurations. Muxed with camera interface.	
P1-46	GPIO_27	Available with all configurations. Muxed with camera interface.	
P1-48	GPIO_28	Available with all configurations. Muxed with camera interface.	
P1-45	GPIO_29	Available with all configurations. Muxed with camera interface.	
P1-47	GPIO_30	Available with all configurations. Muxed with camera interface.	
P1-49	GPIO_31	Available with all configurations. Muxed with camera interface.	
P1-52	GPIO_32	Available with all configurations. Muxed with camera interface.	
P1-51	GPIO_33	Available with all configurations. Muxed with camera interface.	
P1-53	GPIO_34	Available with all configurations. Muxed with camera interface.	
P1-57	GPIO_35	Available with all configurations. Muxed with camera interface.	
P1-54	GPIO_38	Available with all configurations. Muxed with camera interface.	
P1-56	GPIO_39	Available with all configurations. Muxed with camera interface.	
P2-46	GPIO_40	Available with all configurations. Muxed with SD-0.	SD-0
P2-78	GPIO_41	Available with all configurations. Muxed with SD-0.	
P2-54	GPIO_42	Available with all configurations. Muxed with SD-0.	
P2-56	GPIO_43	Available with all configurations. Muxed with SD-0.	
P2-58	GPIO_44	Available with all configurations. Muxed with SD-0.	
P2-60	GPIO_45	Available with all configurations. Muxed with SD-0.	
P2-73	GPIO_46	Only available **without** 'W' option. Muxed with SD-1.	SD-1
P2-75	GPIO_47	Only available **without** 'W' option. Muxed with SD-1.	
P2-61	GPIO_48	Only available **without** 'W' option. Muxed with SD-1.	
P2-63	GPIO_49	Only available **without** 'W' option. Muxed with SD-1.	
P2-65	GPIO_50	Only available **without** 'W' option. Muxed with SD-1.	
P2-69	GPIO_51	Only available **without** 'W' option. Muxed with SD-1.	

CM-A510 signal	Armada 510 signal	Availability	Configuration Group
P2-47	GPIO_52	Available with all configurations. Muxed with I2S.	Digital Audio
P2-45	GPIO_53	Available with all configurations. Muxed with I2S.	
P2-53	GPIO_54	Available with all configurations. Muxed with I2S.	
P2-49	GPIO_55	Available with all configurations. Muxed with I2S.	
P2-51	GPIO_56	Available with all configurations. Muxed with I2S, I2C-2.	
P2-41	GPIO_57	Available with all configurations. Muxed with S/PDIF, I2C-2.	
P1-112	GPIO_62	Available with all configurations. Muxed with UART-1.	UART-1
P1-114	GPIO_63	Available with all configurations. Muxed with UART-1.	

4.13 Camera Interface

The CM-A510 camera interface is implemented with the camera sub-system of the Armada 510 SoC. The camera interface provides the system interface and the processing capability to connect RAW image-sensor modules to the CM-A510. For additional details, please refer to section 17 of the "88AP510 Functional Specifications".

NOTE: Camera signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Individual signals cannot be configured separately for different functions.

Table 23 Camera interface signals

Signal Name	Pin #	Type	Description	Availability	Configuration Group
CAM_CLK	P1-57	I	Pixel clock	Always available.	Camera
CAM_HSYNC	P1-51	I	Horizontal sync input		
CAM_VSYNC	P1-53	I	Vertical sync input		
CAM_SNR_CTL0	P1-54	O	Sensor control 0		
CAM_SNR_CTL1	P1-56	O	Sensor control 1		
CAM_MCLK	P1-52	O	Pixel master clock		
CAM_D0	P1-40	I	Pixel input data line 0		
CAM_D1	P1-42	I	Pixel input data line 1		
CAM_D2	P1-44	I	Pixel input data line 2		
CAM_D3	P1-46	I	Pixel input data line 3		
CAM_D4	P1-48	I	Pixel input data line 4		
CAM_D5	P1-45	I	Pixel input data line 5		
CAM_D6	P1-47	I	Pixel input data line 6		
CAM_D7	P1-49	I	Pixel input data line 7		

4.14 I²C

The CM-A510 features up to three general-purpose I²C interfaces. The following features are supported:

- Master / slave operation
- Standard mode (up to 100K bits/s)

For additional details, please refer to section 25 of "88AP510 Functional Specifications".

NOTE: I2C signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

NOTE: Certain I2C signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Individual signals cannot be configured separately for different functions.

Table 24 I²C signals

Signal Name	Pin #	Type	Description	Availability	Configuration Group
I2C-0					
I2C0_SDA	P2-25	IOD	I2C serial data line. Open drain buffer. Pulled up to 3.3V	Always available.	Not configurable. Dedicated to I2C.
I2C0_SCL	P2-27	IOD	I2C serial clock line. Open drain buffer. Pulled up to 3.3V		
I2C-1					
I2C1_SDA	P1-70	IOD	I2C serial data line. Open drain buffer. Pulled up to 3.3V	Always available.	Each pin is configured separately.
I2C1_SCL	P1-61	IOD	I2C serial clock line. Open drain buffer. Pulled up to 3.3V		
I2C-2					
I2C2_SDA	P2-51	IOD	I2C serial data line. Open drain buffer. Pulled up to 3.3V	Always available.	Digital Audio
I2C2_SCL	P2-41	IOD	I2C serial clock line. Open drain buffer. Pulled up to 3.3V		

4.15 SPI

The CM-A510 features an SPI interface implemented with the Armada 510 SPI controller.

For additional details, please refer to section 24 of "88AP510 Functional Specifications".

NOTE: SPI signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

Table 25 SPI signals

Signal Name	Pin #	Type	Description	Availability	Configuration Group
SPI1_CLK	P1-71	O	SPI clock	Only available **without** the 'I' configuration option.	Each pin is configured separately.
SPI1_CS	P1-65	O	SPI chip select		
SPI1_MISO	P1-63	I	SPI data input		
SPI1_MOSI	P1-69	O	SPI data output		

4.16 SSP

The CM-A510 features an SSP interface implemented with the Armada 510 SSP controller. The interface supports the following features:

- Compliant with Texas Instruments' Synchronous Serial Protocol
- Programmable data sample sizes of 8, 16, 18 and 32-bits
- Up to 24MHz serial clock rate
- Master and slave operation modes

For additional details, please refer to section 27 of "88AP510 Functional Specifications".

NOTE: SSP signals are multiplexed with signals used for other interfaces. For multiplexing characteristics, please refer to section 5.5 of this document.

Table 26 SSP signals

Signal Name	Pin #	Type	Description	Availability	Configuration Group
SSP_SFRM	P1-65	IO	Serial frame indicator	Only available **without** the 'I' configuration option.	Each pin is configured separately.
SSP_RXD	P1-64	I	Serial receive data		
SSP_TXD	P1-69	O	Serial transmit data		
SSP_SCLK	P1-71	IO	Serial clock		

4.17 JTAG

The CM-A510 JTAG interface is derived from the Armada 510 SoC JTAG port.

The Armada 510 target debug interface uses the five standard IEEE 1149.1 (JTAG) signals (nTRST, TCK, TMS, TDI and TDO).

For additional details, please refer to section 8 of "88AP510 Hardware Specifications".

Table 27 JTAG signals

Signal Name	Pin #	Type	Description
JTAG_CLK	P2-90	I	Test clock
JTAG_TDO	P2-94	O	Test data output
JTAG_TDI	P2-92	I	Test data input
JTAG_TMS	P2-96	IO	Test mode select
JTAG_nTRST	P2-88	I	Test logic reset

5 SYSTEM LOGIC

5.1 Power Management

5.1.1 Power Rails

The CM-A510 is powered by a single 5V power rail.

Table 28 Power signals

Signal Name	Type	Description
VIN_5V	P	Main power supply. Typical voltage – 5V.
VCC_RTC	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Leave unconnected if RTC back-up is not required.
GND	P	Common ground.

5.1.2 Low Power Mode

To be added in a future revision of this document.

5.2 Reset

The nRST_IN signal is the main system reset that invokes a global reset that affects every module on the CM-A510.

The SYSRST_nOUT is a dedicated system reset out signal that can be used to reset baseboard peripheral devices. SYSRST_nOUT is asserted low for 20ms on power-on-reset and nRST_IN de-assertion.

Table 29 Reset signals

Signal Name	Pin #	Type	Description
nRST_IN	P2-33	IPU	Main system reset input. Pulled up to 3.3V
SYSRST_nOUT	P2-20	O	System reset output. Leave disconnected if not used.

5.3 Boot Options

The CM-A510 supports the following boot options:

- Boot from onboard SPI NOR flash
- Boot from external hard drive connected to the SATA interface

The boot device is selected with the BOOT_SOURCE signal. The standard boot option is designed for normal system operation with the on-board SPI NOR flash acting as the boot media. The alternate boot option is intended mainly for system debug and production. It can also be used for normal operation with an external SATA hard drive acting as the boot media.

Table 30 Boot options

Boot option	BOOT_SOURCE signal input	Boot device
Standard	Unconnected.	On-board flash
Alternate	Pulled to 3.3V with 1k resistance.	External SATA hard drive

Table 31 Boot selection signals

Signal Name	Pin #	Type	Description
BOOT_SOURCE	P2-117	I	Boot selection. Pulled down with 8.2k. Leave disconnected for standard boot sequence.

5.4 System and Miscellaneous Signals

Table 32 System signals

Signal Name	Pin #	Type	Description
FLASH_nWP	P2-46	I	SPI NOR flash write protection. Active low.
RESERVED	P2-35	I	Reserved for future use. Leave unconnected.
RESERVED	P2-37	O	Reserved for future use. Leave unconnected.
RESERVED	P2-39	I	Reserved for future use. Leave unconnected.
RESERVED	P2-119	I	Reserved for future use. Leave unconnected.
RESERVED	P2-121	I	Reserved for future use. Leave unconnected.
RESERVED	P2-28	-	Reserved for debug and production. Leave unconnected.
RESERVED	P2-30	-	Reserved for debug and production. Leave unconnected.
RESERVED	P2-32	-	Reserved for debug and production. Leave unconnected.
RESERVED	P2-34	-	Reserved for debug and production. Leave unconnected.

5.5 Signal Multiplexing Characteristics

Armada 510 pins have up to six alternate function modes. The table below provides a description of signal multiplexing. Function names marked with gray shading denote the default function intended in the CM-A510 design.

NOTE: Certain software-configurable multi-purpose signals can only be configured on a group basis. Only the entire group may be assigned with a specific function. Signals within a group cannot be configured separately for different functions.

Table 33 Signal multiplexing

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Config. Group
P1-40	GPIO24	CAM_D0	-	-	-	-	-	Camera
P1-42	GPIO25	CAM_D1	-	-	-	-	-	
P1-44	GPIO26	CAM_D2	-	-	-	-	-	
P1-45	GPIO29	CAM_D5	-	-	-	-	-	
P1-46	GPIO27	CAM_D3	-	-	-	-	-	
P1-47	GPIO30	CAM_D6	-	-	-	-	-	
P1-48	GPIO28	CAM_D4	-	-	-	-	-	
P1-49	GPIO31	CAM_D7	-	-	-	-	-	
P1-51	GPIO33	CAM_HSYNC	-	-	-	-	-	
P1-52	GPIO32	CAM_MCLK	-	-	-	-	-	
P1-53	GPIO34	CAM_VSYNC	-	-	-	-	-	
P1-54	GPIO38	CAM_SNR_CTL0	-	-	-	-	-	
P1-56	GPIO39	CAM_SNR_CTL1	-	-	-	-	-	
P1-57	GPIO35	CAM_CLK	-	-	-	-	-	
P1-61	GPIO19	-	UART3_RXD	-	I2C1_SCK	-	-	None
P1-63	GPIO20	-	-	SD1_CD	-	SD0_CD	SPI1_MISO	None
P1-64	GPIO14	-	UART2_TXD	-	SD1_PWREN	SSP_RXD	-	None
P1-65	GPIO21	UART1_RTS	-	SD1_WP	SSP_SFRM	SD0_WP	SPI1_CS	None
P1-66	GPIO15	-	UART2_RXD	-	-	-	-	None
P1-68	GPIO16	-	UART3_RTS	SD0_CD	-	-	-	None
P1-69	GPIO22	UART1_CTS	-	SD1_PWREN	SSP_TXD	SD0_PWREN	SPI1_MOSI	None
P1-70	GPIO17	-	UART3_CTS	SD0_WP	I2C1_SDA	-	-	None
P1-71	GPIO23	-	-	-	SSP_SCLK	-	SPI1_CLK	None

Pin #	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Config. Group
P1-72	GPIO18	-	UART3_TXD	SD0_PWREN	-	-	-	None
P1-112	GPIO62	UART1_RXD	-	-	-	-	-	UART-1
P1-114	GPIO63	UART1_TXD	-	-	-	-	-	
P2-41	GPIO57	SPDIFO	I2C2_SCK	-	-	-	-	Digital Audio
P2-45	GPIO53	I2S1_BCLK	-	-	-	-	-	
P2-47	GPIO52	I2S1_DI	-	-	-	-	-	
P2-49	GPIO55	I2S1_DO	-	-	-	-	-	
P2-51	GPIO56	I2S1_LRCLK	I2C2_SDA	-	-	-	-	
P2-53	GPIO54	I2S1_MCLK	-	-	-	-	-	
P2-54	GPIO42	SD0_DATA0	-	-	-	-	-	SDIO-0
P2-56	GPIO43	SD0_DATA1	-	-	-	-	-	
P2-58	GPIO44	SD0_DATA2	-	-	-	-	-	
P2-60	GPIO45	SD0_DATA3	-	-	-	-	-	
P2-61	GPIO48	SD1_DATA0	-	-	-	-	-	SDIO-1
P2-63	GPIO49	SD1_DATA1	-	-	-	-	-	
P2-65	GPIO50	SD1_DATA2	-	-	-	-	-	
P2-69	GPIO51	SD1_DATA3	-	-	-	-	-	
P2-73	GPIO46	SD1_CLK	-	-	-	-	-	
P2-75	GPIO47	SD1_CMD	-	-	-	-	-	
P2-76	GPIO40	SD0_CLK	-	-	-	-	-	SDIO-0
P2-78	GPIO41	SD0_CMD	-	-	-	-	-	

5.6 RTC

The CM-A510 RTC is implemented with the internal RTC of the Armada 510 SoC. The RTC provides time and calendar information, timed interrupt generation and alarm wake-up event functionality.

Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. The backup battery should be connected to the VCC_RTC power input.

For additional details, please refer to section 29 of “88AP510 Functional Specifications”.

5.7 LED

The CM-A510 features a single general purpose green LED controlled by GPIO65 of the Armada 510 SoC. The LED is ON when GPIO65 is set high.

6 BASEBOARD INTERFACE

The CM-A510 connects to the baseboard through P1 and P2 - 0.6 mm pitch 140-pin connectors.

6.1 Connector Pin-out

Table 34 Connector P1

Pin #	CM-A510 Signal Name	Reference Section		Pin #	CM-A510 Signal Name	Reference Section
P1-1	LAN0_MDIP1	4.2.1		P1-2	LAN0_MDIP0	4.2.1
P1-3	LAN0_MDIN1	4.2.1		P1-4	LAN0_MDIN0	4.2.1
P1-5	LAN0_LED1	4.2.1		P1-6	LAN0_LED0	4.2.1
P1-7	VIN_5V	5.1.1		P1-8	GND	5.1.1
P1-9	LAN0_MDIP3	4.2.1		P1-10	LAN0_MDIP2	4.2.1
P1-11	LAN0_MDIN3	4.2.1		P1-12	LAN0_MDIN2	4.2.1
P1-13	LAN0_LED2	4.2.1		P1-14	GND	5.1.1
P1-15	N.C.			P1-16	N.C.	
P1-17	N.C.			P1-18	N.C.	
P1-19	VIN_5V	5.1.1		P1-20	N.C.	
P1-21	TS_X-	4.11		P1-22	N.C.	
P1-23	TS_X+	4.11		P1-24	N.C.	
P1-25	N.C.			P1-26	GND	5.1.1
P1-27	TS_Y-	4.11		P1-28	VGA_R	4.1
P1-29	TS_Y+	4.11		P1-30	VGA_G	4.1
P1-31	VIN_5V	5.1.1		P1-32	VGA_B	4.1
P1-33	N.C.			P1-34	VGA_HSYNC	4.1
P1-35	N.C.			P1-36	VGA_VSYNC	4.1
P1-37	VCC_RTC	5.1.1		P1-38	GND	5.1.1
P1-39	N.C.			P1-40	CAM_D0 GPIO24	4.13 4.12
P1-41	N.C.			P1-42	CAM_D1 GPIO25	4.13 4.12
P1-43	VIN_5V	5.1.1		P1-44	CAM_D2 GPIO26	4.13 4.12
P1-45	CAM_D5 GPIO29	4.13 4.12		P1-46	CAM_D3 GPIO27	4.13 4.12
P1-47	CAM_D6 GPIO30	4.13 4.12		P1-48	CAM_D4 GPIO28	4.13 4.12
P1-49	CAM_D7 GPIO31	4.13 4.12		P1-50	GND	5.1.1
P1-51	CAM_HSYNC GPIO33	4.13 4.12		P1-52	CAM_MCLK GPIO32	4.13 4.12
P1-53	CAM_VSYNC GPIO34	4.13 4.12		P1-54	CAM_SNR_CTL0 GPIO38	4.13 4.12
P1-55	VIN_5V	5.1.1		P1-56	CAM_SNR_CTL1 GPIO39	4.13 4.12
P1-57	CAM_CLK GPIO35	4.13 4.12		P1-58	CAM_TW_SCK	4.13
P1-59	N.C.			P1-60	CAM_TW_SDA	4.13
P1-61	UART3_RXD I2C1_SCL GPIO19	4.8 4.14 4.12		P1-62	GND	5.1.1
P1-63	SPI1_MISO SD0_CD GPIO20	4.15 4.10 4.12		P1-64	UART2_TXD SSP_RXD GPIO14	4.8 4.16 4.12
P1-65	SPI1_CS SD0_WP SSP_SFRM GPIO21	4.15 4.10 4.16 4.12		P1-66	UART2_RXD GPIO15	4.8 4.12
P1-67	VIN_5V	5.1.1		P1-68	UART3_RTS SD0_CD GPIO16	4.8 4.10 4.12

Pin #	CM-A510 Signal Name	Reference Section		Pin #	CM-A510 Signal Name	Reference Section
P1-69	SPI1_MOSI SD0_PWREN SSP_TXD GPIO22	4.15 4.10 4.16 4.12		P1-70	UART3_CTS SD0_WP I2C1_SDA GPIO17	4.8 4.10 4.14 4.12
P1-71	SPI1_CLK SSP_SCLK GPIO23	4.15 4.16 4.12		P1-72	UART3_TXD SD0_PWREN GPIO18	4.8 4.10 4.12
P1-73	N.C.			P1-74	GND	5.1.1
P1-75	LCD_D0	4.1		P1-76	LCD_D1	4.1
P1-77	LCD_D2	4.1		P1-78	LCD_D3	4.1
P1-79	VIN_5V	5.1.1		P1-80	N.C.	
P1-81	LCD_D4	4.1		P1-82	LCD_D5	4.1
P1-83	LCD_D6	4.1		P1-84	LCD_D7	4.1
P1-85	LCD_D8	4.1		P1-86	GND	5.1.1
P1-87	LCD_D9	4.1		P1-88	LCD_D10	4.1
P1-89	LCD_D11	4.1		P1-90	LCD_D12	4.1
P1-91	VIN_5V	5.1.1		P1-92	LCD_D13	4.1
P1-93	LCD_D14	4.1		P1-94	LCD_D15	4.1
P1-95	LCD_D16	4.1		P1-96	LCD_D17	4.1
P1-97	LCD_D18	4.1		P1-98	GND	5.1.1
P1-99	LCD_D19	4.1		P1-100	LCD_D20	4.1
P1-101	LCD_D21	4.1		P1-102	LCD_D22	4.1
P1-103	VIN_5V	5.1.1		P1-104	LCD_D23	4.1
P1-105	LCD_E	4.1		P1-106	N.C.	
P1-107	LCD_VSYNC	4.1		P1-108	LCD_CLK	4.1
P1-109	LCD_HSYNC	4.1		P1-110	GND	5.1.1
P1-111	N.C.			P1-112	UART1_RXD GPIO62	4.8 4.12
P1-113	N.C.			P1-114	UART1_TXD GPIO63	4.8 4.12
P1-115	VIN_5V	5.1.1		P1-116	N.C.	
P1-117	RS232_RXD	4.9		P1-118	N.C.	
P1-119	RS232_TXD	4.9		P1-120	N.C.	
P1-121	RS232_RTS	4.9		P1-122	GND	5.1.1
P1-123	RS232_CTS	4.9		P1-124	N.C	
P1-125	N.C.			P1-126	USB2_CPEN	4.5
P1-127	VIN_5V	5.1.1		P1-128	USB1_CPEN	4.5
P1-129	USB2_DN	4.5		P1-130	USB0_DN	4.5
P1-131	USB2_DP	4.5		P1-132	USB0_DP	4.5
P1-133	USB3_CPEN	4.5		P1-134	GND	5.1.1
P1-135	USB3_DN	4.5		P1-136	USB1_DN	4.5
P1-137	USB3_DP	4.5		P1-138	USB1_DP	4.5
P1-139	VIN_5V	5.1.1		P1-140	N.C	

Table 35 Connector P2

Pin #	CM-A510 Signal Name	Reference Section		Pin #	CM-A510 Signal Name	Reference Section
P2-1	LAN1_MDIP1	4.2.2		P2-2	LAN1_MDIP0	4.2.2
P2-3	LAN1_MDIN1	4.2.2		P2-4	LAN1_MDIN0	4.2.2
P2-5	LAN1_LED1	4.2.2		P2-6	LAN1_LED0	4.2.2
P2-7	GND	5.1.1		P2-8	GND	5.1.1
P2-9	LAN1_MDIP3	4.2.2		P2-10	LAN1_MDIP2	4.2.2
P2-11	LAN1_MDIN3	4.2.2		P2-12	LAN1_MDIN2	4.2.2
P2-13	LAN1_LED2	4.2.2		P2-14	GND	5.1.1
P2-15	PCIE1_CLKREQ	4.3		P2-16	N.C.	
P2-17	PCIE0_CLKREQ	4.3		P2-18	N.C.	
P2-19	VIN_5V	5.1.1		P2-20	SYSRST_OUTn	
P2-21	N.C.			P2-22	N.C.	
P2-23	N.C.			P2-24	N.C.	
P2-25	I2C0_SDA	4.14		P2-26	GND	5.1.1
P2-27	I2C0_SCL	4.14		P2-28	RESERVED	5.4
P2-29	N.C.			P2-30	RESERVED	5.4
P2-31	VIN_5V	5.1.1		P2-32	RESERVED	5.4
P2-33	nRST_IN	5.2		P2-34	RESERVED	5.4
P2-35	RESERVED	5.4		P2-36	N.C.	

Pin #	CM-A510 Signal Name	Reference Section		Pin #	CM-A510 Signal Name	Reference Section
P2-37	RESERVED	5.4		P2-38	GND	5.1.1
P2-39	RESERVED	5.4		P2-40	N.C.	
P2-41	SPDIF I2C2_SCL GPIO57	4.7.3 4.14 4.12		P2-42	N.C.	
P2-43	VIN_5V	5.1.1		P2-44	N.C.	
P2-45	I2S1_BCLK GPIO53	4.7.2 4.12		P2-46	FLASH_nWP	5.4
P2-47	I2S1_SDI GPIO52	4.7.2 4.12		P2-48	N.C.	
P2-49	I2S1_SDO GPIO55	4.7.2 4.12		P2-50	N.C.	
P2-51	I2S1_LRCLK I2C2_SDA GPIO56	4.7.2 4.14 4.12		P2-52	GND	5.1.1
P2-53	I2S1_MCLK GPIO54	4.7.2 4.12		P2-54	SD0_DATA0 GPIO42	4.10 4.12
P2-55	VIN_5V	5.1.1		P2-56	SD0_DATA1 GPIO43	4.10 4.12
P2-57	N.C.			P2-58	SD0_DATA2 GPIO44	4.10 4.12
P2-59	N.C.			P2-60	SD0_DATA3 GPIO45	4.10 4.12
P2-61	SD1_DATA0 GPIO48	4.10 4.12		P2-62	GND	5.1.1
P2-63	SD1_DATA1 GPIO49	4.10 4.12		P2-64	N.C.	
P2-65	SD1_DATA2 GPIO50	4.10 4.12		P2-66	N.C.	
P2-67	VIN_5V	5.1.1		P2-68	N.C.	
P2-69	SD1_DATA3 GPIO51	4.10 4.12		P2-70	N.C.	
P2-71	N.C.			P2-72	N.C.	
P2-73	SD1_CLK GPIO46	4.10 4.12		P2-74	GND	5.1.1
P2-75	SD1_CMD GPIO47	4.10 4.12		P2-76	SD0_CLK GPIO40	4.10 4.12
P2-77	N.C.			P2-78	SD0_CMD GPIO41	4.10 4.12
P2-79	VIN_5V	5.1.1		P2-80	N.C.	
P2-81	PCIE1_CLK_N	4.3		P2-82	N.C.	
P2-83	PCIE1_CLK_P	4.3		P2-84	N.C.	
P2-85	N.C.			P2-86	GND	5.1.1
P2-87	N.C.			P2-88	JTAG_nTRST	0
P2-89	SYSRST_INn	5.2		P2-90	JTAG_CLK	0
P2-91	VIN_5V	5.1.1		P2-92	JTAG_TDI	0
P2-93	N.C.			P2-94	JTAG_TDO	0
P2-95	N.C.			P2-96	JTAG_TMS	0
P2-97	N.C.			P2-98	GND	5.1.1
P2-99	PCIE0_CLK_N	4.3		P2-100	N.C.	
P2-101	PCIE0_CLK_P	4.3		P2-102	N.C.	
P2-103	VIN_5V	5.1.1		P2-104	N.C.	
P2-105	PCIE1_RX_N	4.3		P2-106	PCIE0_RX_N	4.3
P2-107	PCIE1_RX_P	4.3		P2-108	PCIE0_RX_P	4.3
P2-109	N.C.			P2-110	GND	5.1.1
P2-111	PCIE1_TX_N	4.3		P2-112	PCIE0_TX_N	4.3
P2-113	PCIE1_TX_P	4.3		P2-114	PCIE0_TX_P	4.3
P2-115	VIN_5V	5.1.1		P2-116	N.C.	
P2-117	BOOT_SCR0	5.3		P2-118	SATA_RX-	4.4
P2-119	RESERVED	5.4		P2-120	SATA_RX+	4.4
P2-121	RESERVED	5.4		P2-122	GND	5.1.1
P2-123	AUDIO_GND	4.7.1		P2-124	SATA_TX-	4.4
P2-125	MIC_BIAS	4.7.1		P2-126	SATA_TX+	4.4
P2-127	VIN_5V	5.1.1		P2-128	N.C.	
P2-129	MIC_IN	4.7.1		P2-130	N.C.	
P2-131	AUDIO_IN_R	4.7.1		P2-132	N.C.	
P2-133	AUDIO_IN_L	4.7.1		P2-134	GND	5.1.1

Pin #	CM-A510 Signal Name	Reference Section		Pin #	CM-A510 Signal Name	Reference Section
P2-135	VIN_5V	5.1.1		P2-136	USB3_nOVC	4.5
P2-137	AUDIO_OUT_L	4.7.1		P2-138	USB2_nOVC	4.5
P2-139	AUDIO_OUT_R	4.7.1		P2-140	USB1_nOVC	4.5

6.2 Connector Type

Table 36 Connector type

Part Reference	Mfg.	CM-A510 connector P/N	Baseboard (mating) connector P/N
P1, P2	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab, see [prices] >> [accessories] links at CompuLab's website.

CompuLab's P/N for the AMP 1-5353190-0 connector is "CON140".

6.3 Mechanical Drawings

Figure 3 CM-A510 top

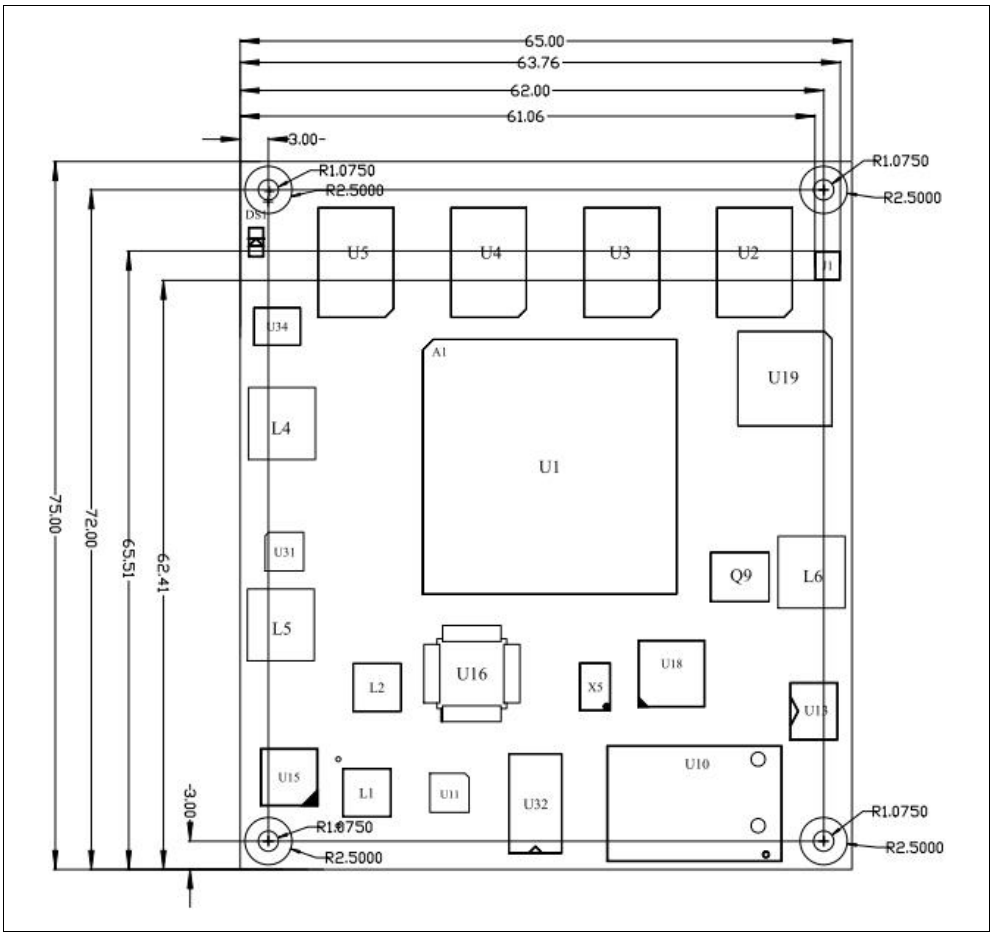
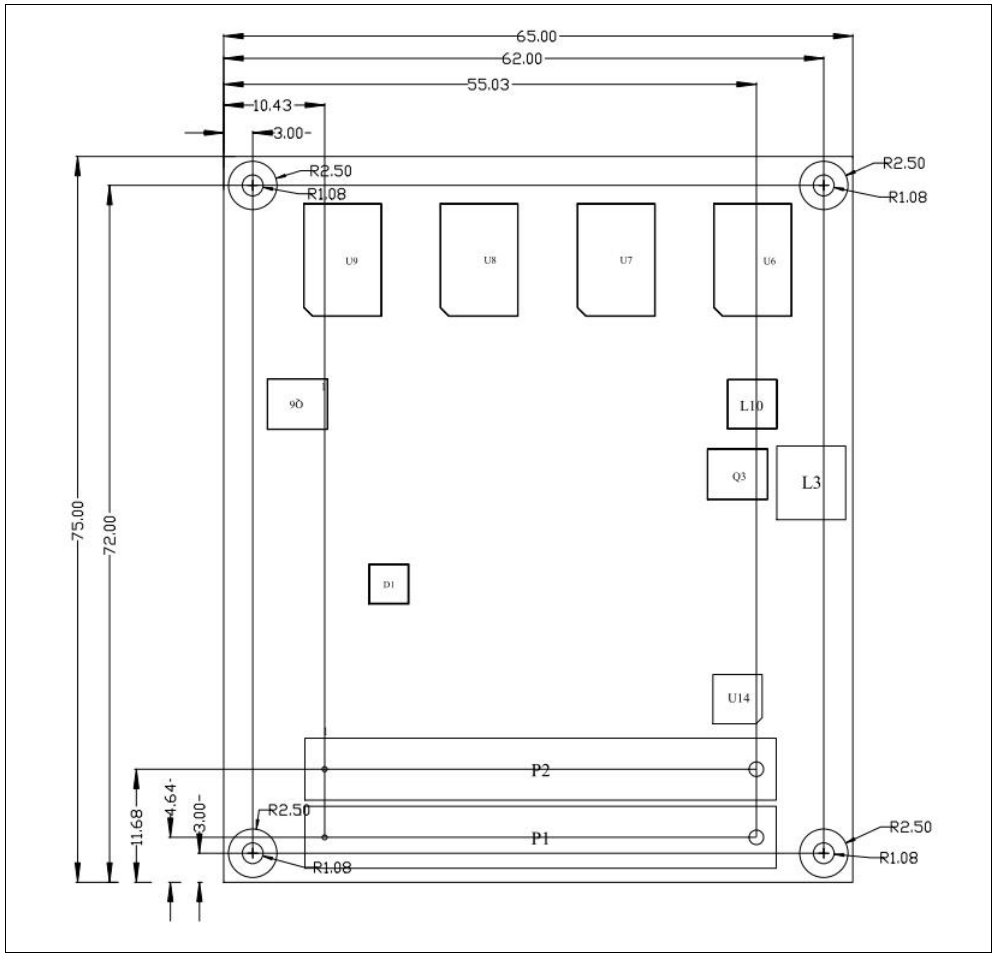


Figure 4 CM-A510 bottom (X-Ray view - as seen from top side)



1. All dimensions are in millimeters.
2. Height of all components is <3mm.
3. Baseboard connectors provide 4mm board-to-board clearance.
4. Board thickness is 1.6mm.

Mechanical drawings are available in DXF format from CompuLab's website, following [Developer] >> [CM-A510] >> [CM-A510 - Dimensions and Connectors Location] links.

6.4 Standoffs

The CM-A510 has four mounting holes for standoffs. Standoffs are implemented with three parts: screw, spacer and nut.

Table 37 Standoffs

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	• FCI 95121-005 • Acton InoxPro BF22102010 • World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	• Hirosugi ASU-2004 • MAC8 2SP-4 • World Bridge Machinery M2, L=4.2 mm
Nut	M2, 1.6-2.0mm width	• FCI 92869-001 (or 002) • Acton InoxPro BG12102000 • Bossard 1241397 (DIN934-A2 M2) • World Bridge Machinery 381A52000

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 38 Absolute Maximum ratings

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VIN_5V)	-0.3		6.0	V
VCC_RTC	-0.3		4.0	V

7.2 Recommended Operating Conditions

Table 39 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VIN_5V)	4.75	5.0	5.25	V
RTC backup battery voltage (VCC_RTC)	2.2	3.3	3.45	V

7.3 DC Electrical Characteristics

Table 40 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
3.3V Digital I/O					
V_{IH}		2		3.6	V
V_{IL}		-0.3		0.8	V
V_{OH}		2.4			V
V_{OL}				0.4	V
I^2C (open drain with internal pull up to 3.3V)					
V_{IH}		2.3		3.8	V
V_{IL}		-0.5		1.0	V
V_{OL}	IOL = 3 mA	-		0.4	V
IRS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing			±25		V

7.4 Power Consumption

To be added in a future revision of this document.

7.5 ESD Performance

Table 41 ESD Performance

Interface	ESD Performance
USB host	±8 kV ESD using HBM
RS232	±15 kV ESD using HBM

7.6 Thermal Characteristics

Power dissipation characteristics vary depending on Armada SoC operating frequency and average workload.

Table 42 Thermal Characteristics

SoC operating frequency	Operational workload	Thermal conditions	ΔT between SoC case and ambient temperature
1GHz	Full	Operating in open-air, no heat-plate. Ambient temperature - 25°C.	60°C
	Idle		45°C
800MHz	Full		45°C
	Idle		35°C

When ambient temperature exceeds 35°C or when ΔT > 45°C, the CM-A510 should be provided with a heat dissipation solution. The following solutions may be used:

- Heat-plate supplied by CompuLab. For further details, please refer to section 8.4 of this document.
- Heat extruder integrated into customer designed enclosure
- Enforced airflow

7.7 Operating Temperature Ranges

The CM-A510 is available with three options of operating temperature range.

Table 43 CM-A510 Temperature Range Options

Range	Temp.	Description
Commercial	0° to 70° C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20° to 70° C	Every board undergoes a short test for the lower limit (-20° C) qualification.
Industrial	-40° to 85° C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Baseboard Design Guidelines

- Ensure that all VIN_5V and GND power pins are connected.
- Major power rails - VIN_5V and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system's signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VIN_5V and GND near the mating connectors.
- It is recommended to connect the standoff holes of the baseboard to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CM-A510 operation. All power-up circuitry and all required pull-ups/pull-downs are present on the module.
- If for some reason you decide to place an external pull-up or pull-down resistor on a certain signal (for example - on the GPIO's), first check the documentation of that signal provided in this manual. Certain signals have on-board pull-up/pull-down resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - PCI Express, SATA, Ethernet and USB signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of baseboard noise.
- Be careful when placing components under the CM-A510 module. The baseboard interface connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-A510. Maximum allowable height for components placed under the CM-A510 is 1mm.
- Refer to the SB-A510 baseboard reference design schematics.

8.2 Baseboard Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the baseboard. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VIN_5V power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
  - Devices improperly driving the local bus

- External pull-up/pull-down resistors overriding the module's on-board values, or any other component creating the same "overriding" effect
- Faulty power supply

- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the baseboard, shorting them on the connectors can disable the module. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often, solder bridges are deep beneath the connector's body. Note that solder shorts are the most frequent factor disabling module operation.
- Check possible signal shorts due to errors of baseboard PCB design or assembly.
- Improper functioning of a custom baseboard can accidentally delete the CM-A510 boot-up code or even damage the module hardware permanently. Before each activation attempt, check that your module is still functional with a CompuLab SB-A510 baseboard.
- It is recommended to assemble more than one baseboard for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics' Implementation

8.3.1 Magnetics' Selection

Refer to the table below for compatible magnetic modules. Designers should test and qualify magnetic modules before using them in an application.

Table 44 Compatible Magnetics

Vendor	P/N	Package
UDE	RB1-125BAK1A	Integrated RJ45
Speed Tech	P65-101-[1|2]AK9	Integrated RJ45
Pulse Engineering	H5007	16-pin SOIC
Pulse Engineering	H1251	16-pin SOIC

8.3.2 Magnetics' Connection

For magnetic modules connection, please refer to the SB-A510 reference design schematics.

8.4 Heat-plate Integration

To be added in a future revision of this document.