SPECIFICATION

DVB-T　Diversity Receiver

1.SCOPE

　The DY-9080F is intended for the reception of DVB-T compliant MPEG2 signals
　(full TES 300 744 compliant)
　in combination with the tuner ,all functions are integrated to deliver a corrected stream given
　DVB-T encoded signal(2k or 8k mode)with 6,7,8 MHz bandwidth.
　The Receiver for mobile application.

2.GENERAL SPECIFICATIONS

　　2-1. RECEIVING FREQUENCY RANGE　　:VHF 174~227MHz
　　　　　　　　　　　　　　　　　　　　　　 UHF 474~858MHz

　　2-2. SUPPLY VOLTAGE　　　　　　　　:B1　 3.3V +/- 0.1V　　　Ripple < 10mV

　　2-3. CONSUMPTION CURRENT　　　　　:B1　 3.3V　492 mA typ

　　2-4. OPERATION AND STORAGE　　　　TEMPERATURE 0~50°C
　　　　　CONDITIONS FOR GUARANTEE　　HUMIDITY 85% OR LESS

3.TEST CONDITIONS

　　3-1. TESTING AMBIENT CONDITIONS
　　　　　DEFINED AS TEMPERATURE OF 25+/-2°C AND HUMIDITY OF 65+/-5% RH.
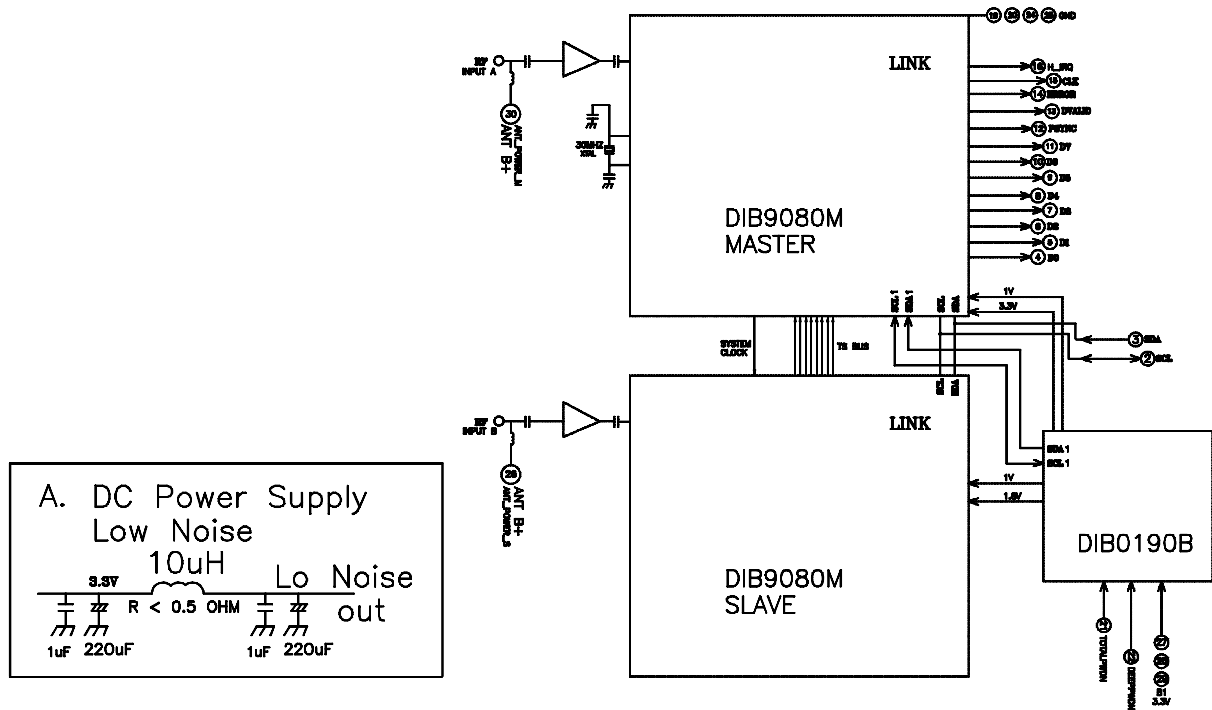　　　　　NOTE : THAT TEMPERATURES OF 5~30°C AND HUMIDITY OF 45~85% MAY BE
　　　　　　　　　REGARDED AS STANDARD.

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4.Electrical Specifications

Electrical Characteristics Control refer to DiBcom 9080M date sheet,and MT2266 data sheet

Circuit block diagram

A. DC Power Supply
Low Noise
10uH   Lo Noise
out
3.3V
R < 0.5 OHM
1uF 220uF   1uF 220uF

NO	ITEM	CONDITION	MIN	TYP	MAX	NOTES
4.1	Input sensitivity	Band width 8MHz FET mode 8K Guard interval 1/8 FEC code rate 2/3 RS uncorrected error=0 Constellation64QAM 16 QAM QPSK	-78 -83 -88	-81 -86 -91		dBm dBm dBm
4.2	Performance with AWGN	C/N at antenna input		20		dB
4.3	protection from co-channel PAL	PAL-I 75% bars,fm sound 1KHz		4		dB
4.4	protection from adjacent channel PAL	PAL-i 75% bars,FM sound 1KHz		-35		dB
4.5	protection from adjacent DVB-T			-25		dB
4.6	protection from image Channel PAL	PAL-I 75% color bars,FM sound 1KHz		-46		dB
4.7	Pecformance with single echo inside the interval 2K mode	Te=Tg included (7.2us) Delay phase=0°		1.5		dB
4.8	Performance with single echo inside the interval	Te-Tsymbo 1/2 Delay phase=0°		19.5		dB
4.9	Typical multi-path channel	Additional END		4.0		dB

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5. Electrical Specification (Doppler Performance)

Fading and Doppler Test Equipment Setup
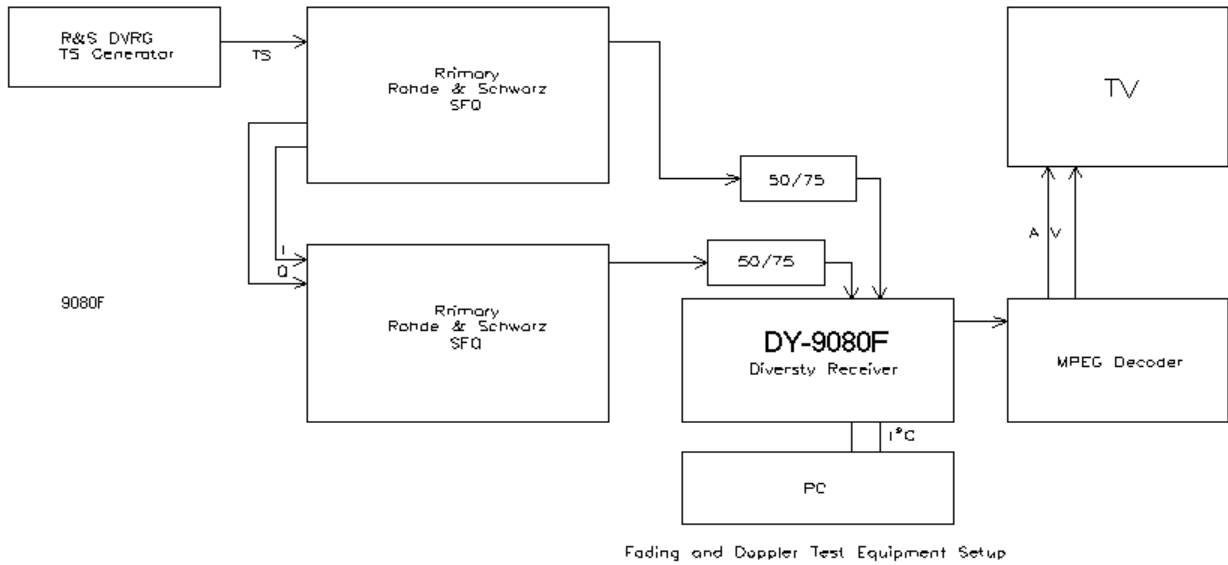
Typical Urban reception (TU6)

This profile reproduces the terrestrial propagation in an urban area. It has been defined by COST207 as a Typical Urban (TU6) profile and is made of 6 paths having wide dispersion in delay and relatively strong power. **[Reference 1]**

Tap number	Delay (us)	Power (dB)	Doppler spectrum
1	0.0	-3	Rayleigh
2	0.2	0	Rayleigh
3	0.5	-2	Rayleigh
4	1.6	-6	Rayleigh
5	2.3	-8	Rayleigh
6	5.0	-10	Rayleigh

Typical Urban profile (TU6) constitution

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Rural Area reception (RA6)

This profile reproduces the terrestrial propagation in a rural area. It has been defined by COST207 as a Rural Area (RA6) profile and is made of 6 paths having relatively short delay and small power. **[Reference 1]**

Tap number	Delay (us)	Power (dB)	Doppler spectrum
1	0.0	0	Rice
2	0.1	-4	Rayleigh
3	0.2	-8	Rayleigh
4	0.3	-12	Rayleigh
5	0.4	-16	Rayleigh
6	0.5	-20	Rayleigh

Table 2: Rural Area profile (RA6) constitution

0dB Echo with Doppler

This profile has been defined by member of the Motivate group. The 0dB echo profile is then made of two rays having the same power, delayed from half the Guard Interval value and presenting a pure Doppler characteristic. The Doppler frequency f_d is defined to be half the frequency separation of the two paths. **[Reference 1]**

Tap number	Delay (us)	Power (dB)	Doppler spectrum	Frequency ratio
1	0	0	Pure Doppler	-1
2	1/2 Tg	0	Pure Doppler	+1

Table 3: 0 dB echo with Doppler profile constitution

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Results

Typical Urban Reception (TU6) Results

The following results are the Doppler Frequency to achieve the point of failure of 1 picture artefact or error in a 20 second time period.

Modulation Mode	typ
8K 64QAM, FEC 1/2 and Guard Band 1/8	45Hz
8K 64QAM, FEC 2/3 and Guard Band 1/8	26Hz
2K 64QAM, FEC 2/3 and Guard Band 1/32	128Hz
2K 16QAM, FEC 3/4 and Guard Band 1/32	195Hz

Rural Area Reception (RA6) Results

The following results are the Doppler Frequency to achieve the point of failure of 1 picture artefact or error in a 20 second time period.

Modulation Mode	typ
8K 64QAM, FEC 1/2 and Guard Band 1/8	30Hz
8K 64QAM, FEC 2/3 and Guard Band 1/8	20Hz
2K 64QAM, FEC 2/3 and Guard Band 1/32	86Hz
2K 16QAM, FEC 3/4 and Guard Band 1/32	119Hz

0dB Echo With Doppler Reception (0dB) Results

The following results are the Doppler Frequency to achieve the point of failure of 1 picture artefact or error in a 20 second time period.

Modulation Mode	typ
8K 64QAM, FEC 1/2 and Guard Band 1/8	50Hz
8K 64QAM, FEC 2/3 and Guard Band 1/8	43Hz
2K 64QAM, FEC 2/3 and Guard Band 1/32	160Hz
2K 16QAM, FEC 3/4 and Guard Band 1/32	233Hz

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6.   **Electrostatic discharge**

6.1   **Test**

Each front-end must be capable of normal performance following its subjection to the following tests:

<u>MIL STD 883C HBM</u>

Test is performed with a voltage discharge from a 100**PF** capacitor over a 1500 **OHM** series resistance in the discharge path. There is a direct contact between the test probe head and the unit under test, using the test points and conditions detailed below:

o   Test to pins 1 through 30:
   3 successive ESD discharges of**+/-2 KVDC** between each pin and the front-end frame.

IEC 1000-4-2

Test is performed with a voltage discharge from a 150**PF** capacitor over a 330 **OHM** series resistance in the discharge path. There is a direct contact between the test probe head and the unit under test, using the test points and conditions detailed below:

o   Test for antenna input socket +/-8 **KVDC**

6.2   **Handling**

Anyone handling a front-end must wear a properly grounded anti-static discharge bracelet to minimize **ESD** damage.

After each front-end is aligned and tested, it will be packed with anti-static poly foam or material prior to transportation and storage. This protective foam is to remain in place until the front-end is assembled and soldered onto the receiver main board.

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7   **Reliability test procedure & conditions**

Note:Room remperature = 25°C +/- 2°C

7.1 **Heat load test**

o   Measure the DUTs at room temperature

o   Load the DUTs into chamber of the following conditions:

   Temperature = 60 °C
   Period   = 500 hrs
   Cycle   = 1.5 hrs on; 0.5 hrs off
   Quantity   = 10 pcs

o   Cool-down 0,5 hr at room temperature, then measured the DUTs within 1 hr

o   The test shall be continued to 1000 cycles for information only

7.2 **Humidity load test**

o   Measure the DUTs at room temperature

o   Load the DUTs into chamber of the following conditions:

   Temperature = 40 +/- 5 °C
   Period   = 24 hrs
   Cycle   = constantly on
   Quantity   = 24 pcs

o   Cool-down 0.5 hr at room temperature, then measured the DUTs within 1 hr

o   Load the DUTs again into chamber of following conditions:

   Temperature = 40+/-5°C
   Humidity   = 90 to 95%
   Period   = 500 hrs
   Cycle   = 1.5 hrs on; 0.5 hrs off
   Quantity   = 20 pcs

o   Cool down 0.5hr at room temperature, then measured the DUTs within 1 hr

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7.3 **Cold test**
   o Measure the DUTs at room temperature
   o Load the DUTs into chamber of the following conditions:

        Temperature = -2 +/-5 ^{o}C
        Period   = 500 hrs
        Cycle   = constantly on
        Quantity   = 10 pcs

   o Warm up for 2 hrs at room temperature, then measured the DUT within 1 hr

7.4 **Thermal shock**
   o Measure the DUTs at room temperature
   o Load the DUTs into chamber of the following conditions:

        Temperature = -25°C for 60 min
                            ↓   ↑
                      80°C for 60 min
        Period   = 200 cycles
        Power   = power off
        Quantity   = 10 pcs

   o Cool-down 0.5 hr at room temperature then measured the DUST within 1 hr

7.5 **Temperature cycle test**
   o Measure the DUTs at room temperature
   o Load the DUTs into chamber of the following conditions:

        Temperature = -5°C for 16 hrs then 60°C for 8 hrs
        Period   = 500 hrs
        Cycle   = constantly on
        Quantity   = 10pcs

   o Cool down 0.5 hr at room temperature, then measured the DUST within 1 hr
   o Load the DUTs again into chamber of the following conditions:

        Temperature = 40 +/- 5°C
        Humidity   = 90 to 95%
        Period   = 500 hrs
        Cycle   = 1.5 hrs on; 0.5 hrs off
        Quantity   = 10 pcs

   o Cool down 0.5 hr at room temperature, then measured the DUST within 1hr

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7.6 **Vibration test**
- o Frequency: 3.5 Hz
- o Vertical amplitude: 15 to 25 mm
- o Duration: 1 hr
- o Quantity: 1 carton

7.7 **Drop test**
- o Packaged apparatus: <or = 50 kg
- o Height: depend on weight
- o 1 corner + 3 edger + 6 faces

>   Drop on the weakest corner (point G)
>   Drop on the shortest edge on contact with point G
>   Drop on average edge in contact with point G
>   Drop on the longest edge in contact with point G
>   Drop flat wise on the side of minimum surface
>   Drop flat wise on the side of opposite minimum surface
>   Drop flat wise on the side of average surface
>   Drop flat wise on the side of opposite average surface
>   Drop flat wise on the side of maximum surface
>   Drop flat wise on the side of opposite maximum surface

- o Quantity :1 carton

7.8 Life test
- o Measure the DUTs at room temperature
- o Load the DUTs into chamber of the following conditions:

>   Temperature = 60 ^{o}C
>   Period   = 500 hrs
>   Cycle   = constantly on
>   Quantity   = 20 pcs

- o Cool down 0.5 hr at room temperature, then measured the DUTs within 1hr

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Power On   Power Off

Clock

Reset

Core 1.2V

I/O banks

T1 T2   T3   T4

power on and off sequence
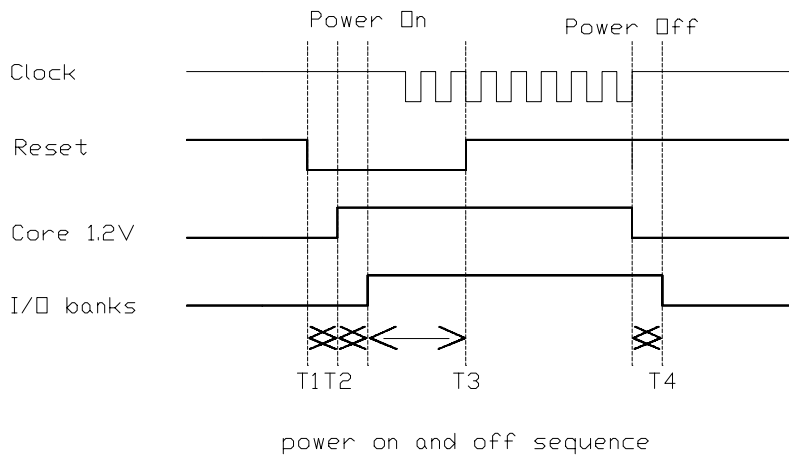
1. DiB IC can support I2C clock up to 1MHZ

2. After reset release,you can send immediatly I2C messages.Maybe wait 1-2 clock cycle
   before sending I2C message,just to be sure.

3. The only limit is T3 > 10ms.

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8.0 SPI interface

SPI signals	Description	Signal
CS	Host DiB9080M chip select(active low)	HOST_BUS12
VDD_SD	Power Flag	HOST_BUS7
CLK	Host clock to DiB9080M	HOST_BUS8
DATAIN	Host to DiB9080M data	HOST_BUS13
DATAOUT	DiB9080M to host data	HOST_BUS9
IRQ	DiB9080M to host	HOST_BUS10

8.1 SDIO interface

SD 1 bit	Description	Signal
VDD_SD	Power Flag	HOST_BUS7
CLK	Host clock to DiB9080M	HOST_BUS8
CMD	Bidirectional command / response signal	HOST_BUS13
DATA_0	Bidirectional data	HOST_BUS9
IRQ	DiB9080M to host	HOST_BUS10

SD 4 bit	Description	Signal
VDD_SD	Power Flag	HOST_BUS7
CLK	Host clock to DiB9080M	HOST_BUS8
CMD	Bidirectional command / response signal	HOST_BUS13
DATA_0	Bidirectional data	HOST_BUS9
DATA_1	Bidirectional data	HOST_BUS10
DATA_2	Bidirectional data	HOST_BUS11
DATA_3	Bidirectional data	HOST_BUS12
IRQ	DiB9080M to host	HOST_BUS14

8.2 Transport stream serial output

MPDATA [0]:MPEG2-TS data bits (msb first)

MPDATA [1]:bit-envelope of the 204 bytes

MPDATA [2]:bit-envelope of the 188 bytes

MPDATA [3]:msb position of the 204 bytes

MPDATA [4]:msb position of the 188 bytes

MPDATA [5]:clock gated with MPDATA [1]

MPDATA [6]:clock gated with MPDATA [2]

MPDATA [7]:60 MHz clock (not gated reference clock of the circuit)

MPSTR: envelope of the start byte

MPFRM: envelope of the 188 bytes

MPCLK: byte pseudo-clock (high jitter)

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8.3 DVB-T parallel output

All DVB-T output signals mapped on HOST_BUS as depicted in the table below:

I²C + DVB-T output Siganl	HOUS_BUS
SDA	HOUS_BUS0
SCL	HOUS_BUS1
DATA [0]	HOUS_BUS2
DATA [1]	HOUS_BUS3
DATA [2]	HOUS_BUS4
DATA [3]	HOUS_BUS5
DATA [4]	HOUS_BUS6
DATA [5]	HOUS_BUS7
DATA [6]	HOUS_BUS8
DATA [7]	HOUS_BUS9
CTRL[0]	HOUS_BUS10
CTRL[1]	HOUS_BUS11
CTRL[2]	HOUS_BUS12
CTRL[3]	HOUS_BUS13
IRQ	HOUS_BUS14

8.4   DVB-T output with the following options:

I²C + DVB-T output Signal	HOST_BUS
SDA	HOST_BUS0
SCL	HOST_BUS1
MPDATA[0]	HOST_BUS2
MPDATA[1]	HOST_BUS3
MPDATA[2]	HOST_BUS4
MPDATA[3]	HOST_BUS5
MPDATA[4]	HOST_BUS6
MPDATA[5]	HOST_BUS7
MPDATA[6]	HOST_BUS8
MPDATA[7]	HOST_BUS9
VAUD	HOST_BUS10
SYNC	HOST_BUS11
CLK	HOST_BUS12
ERROR	HOST_BUS13
IRQ	HOST_BUS14
REVERED	HOST_BUS15

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NOTE 1.TOLERANCES ARE ±0.5.
UNLESS OTHERWISE SPECIFIED.

RF INPUT B

RF INPUT A

NARROW—PITCH CONNECTORS
Header:1000—F30E—02R
(Socket:1001—F30E—03R)

E & T
http://www.entery.com.tw

Pin No	Connection	Pin No	Connection
1	NC	16	H_IRQ
2	SCL	17	NC
3	SDA	18	NC
4	D0	19	GND
5	D1	20	GND
6	D2	21	TOTALPWDN
7	D3	22	DEEPPWDN
8	D4	23	NC
9	D5	24	GND
10	D6	25	GND
11	D7	26	ANT_POWER_S
12	PSYNC	27	B1(3.3V)
13	DVALID	28	B1(3.3V)
14	ERROR	29	B1(3.3V)
15	CLK	30	ANT_POWER_M

PIN NO. LIST

2 SCL I2C CLOCK
3 SDA I2C DATA
4~11 D0~D7 BIT DATA OUT
12 PSYNC
13 DVALID
14 ERROR DATA ERROR SIGNAL
15 CLK BIT CLOCK OUT
16 H_IRQ INTERUPT OUTPUT
19,20 GND
21 TOTALPWDN TOTAL POWER DOWN
22 DEEPPWDN DEEP POWER DOWN
24,25 GND
26 ANT_POWER_S ANT POWER SLAVE
27~29 POWER INPUT B1 +3.3V
30 ANT_POWER_M ANT POWER MASTER

DEEPPWDN	Active low, disable all chip functions
TOTALPWDN	

					comtech COMTECH TECHNOLOGY CO., LTD
				DESGN.	SCALE
				CHKD.	TITLE
				APPD.	
ZONE SYM	DATE OR NO.	APPD	CHKD	DESGN	UNIT mm	DOCUMENT NO.