Single Rail Low Voltage 3.0 V CODEC

Description

7541 (μ-law) and 7542 (A - law) are CMOS devices containing a companding CODEC And PCM voice filters on a single chip.

The most featured point is to operate with a single power supply, which provides cost effective design espacially for digital portable equipments like an advanced cordless telephone.

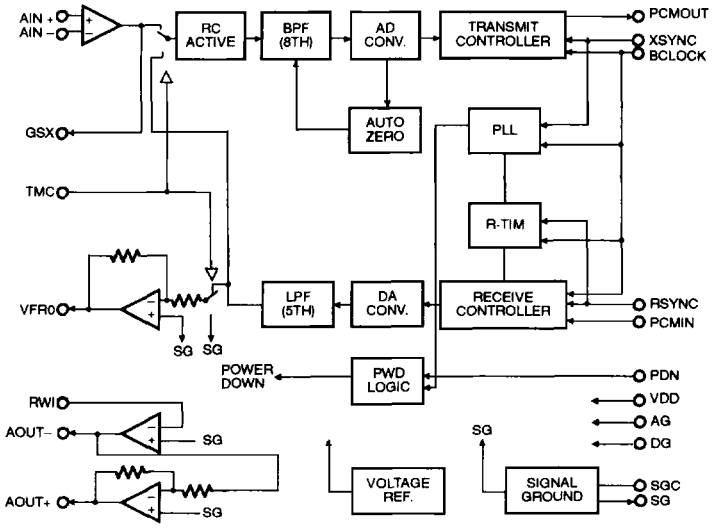
Features

- Single Power Supply : + 3 V ~ +3.8 V
- Low Power Dissipation Operating Mode :
  Typ 23 mW, Max 45.0 mW
  Power Save Mode :
  Typ 1 mW, Max 3.88 mW
  Power Down Mode :
  Typ 0.04 mW, Max 0.4 mW
- Companding Law
  7541 : μ-law
  7542 : A-law
- Transmit/Receive Synchronous Mode Only
- Serial Data Rate : 64/96/128/192/256/384/ 512/768/1024/1536/1544/2048 kbps
- Transmit/Receive Gain Adjustable
- Analog Loop Back Test Mode
- On-chip Precision Voltage Reference
- Ceramic Resonator Direct Drive : 1.2 kΩ + 55 nF
- Package
  20 Pin Skinny DIP :
  24 Pin SOIC :

5

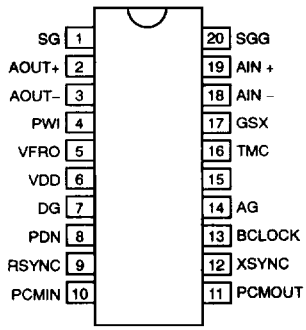
Interface

Block Diagram

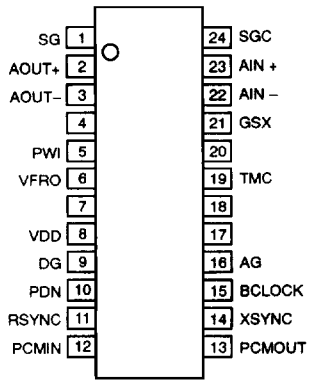


Pin Assignment

DIL 20 pin
Top view



SOIC 24 pin
Top view



Pin Description

AIN+, AIN-, GSX

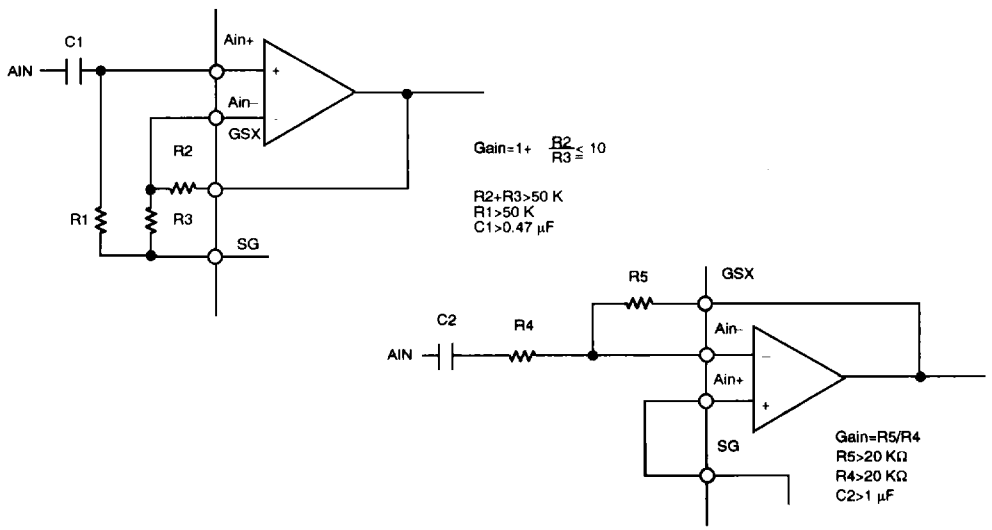
These three pins are used for the transmit gain adjustment.

AIN+ is a non-inverting input of the transmit amplifier.

AIN-is an inverting input of the transmit amplifier.

GSX is transmit amplifier output pin.

Gain adjustment should be refered to the following figure.



AG

AG is the analog ground pin (0 V).

AG is separated from DG on the chip, but should be connected to DG on a printed board.

VFR0

VFR0 is the receive filter output pin.

The maximum voltage swing is 2.0 Vp-p and the signal ground level is at around the potential of SG (on-chip signal ground VDD/2). Minimum load resistance is 20 kΩ

PWI, AOUT+, AOUT−

PWI is connected to the internal inverting input of the receive power amplifier.

AOUT− is the inverted output of the receive power amplifier.

AOUT+ is the inverted output of the another receive power amplifier.

Receive signal level can be adjusted by using PWI, AOUT− and VFR0 refer to Block diagram.

VDD

VDD is the positive power supply pin (+3 V ~ +3.8 V) : TYP 3.3 V.

PCMIN

PCM signal input pin.

This signal is serial data and converted to the analog signal under control of RSYNC and BCLOCK.

The recommended PCM data is 64/96/128/192/256/384/512/768/1024/1536/1544/2048 kbps.

PCM serial data is shifted at the falling edge of BCLOCK.

When total 8 bits data are shifted, all 8 bits data are latched to the internal control register.

MSD (the first bit) is indicated at the rising edge of RSINC.

BCLOCK

BCLOCK is the shift clock input pin.

The clock frequency is same to the data transmission speed and is recommended to be 64/96/128/192/256/384/512/768/1024/1536/1544/2048 kHz.

When BCLOCK is continuously at digital "0" or "1" level both transmit and receive sections become the power save mode.

RSYNC

Receive synchronizing signal input pin.

This signal should be synchronous to BCLOCK and is used for taking in the required 8 bits data from the input serial PCM data stream.

At the same time this signal makes the whole receive operation timing to be synchronous.

XSYNC

Transmit synchronizing signal input pin.

This signal should be synchronous to BCLOCK and is used for taking out the required 8 bits serial PCM data from PCMOUT. At the same time, this signal makes the whole transmit operation timing to be synchronous when XSYNC is continuously at digital "0" or "1" level, both transmit and receive sections enter into power save mode automatically.

Both RSYNC and XSYNC should be within 8 kHz ± 50 ppm.

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DG

DG is the digital ground (0 V) pin.

DG is separated from AG on the chip, but should be connected to AG on a printed board.

TMC

This is a control input pin for operating mode selection, such as normal operating mode and analog loop back mode.

The operating mode are as follows.

TMC Input	Mode
< 0.16*VDD	normal mode
> 0.45*VDD	analog-loop back

PDN

Power down control signal input pin.

By putting PDN on digital "0" state, the whole transmit and receive sections enter to the power down mode.

PCMOUT

PCM signal output pin.

This pin is open drain output. PCM signal is output from this pin. PCM signal is output being synchronized to the rising edge of BCLOCK with MSD first.

This pin shows the high output impedance except the 8 bit PCM data duration, including the case of the power down mode and power save mode.

The companding law and coding pattern conform to CCITT recommendation. In case of 7542 (A-law), the even bits are reversed except MSD.

PCMIN/PCMOUT		
	MSD7541	**MSD7542**
+ Full scale	MSD ↓ 1000 0000	MSD ↓ 1010 1010
+ 0	1111 1111	1101 0101
− 0	0111 1111	0101 0101
− Fulls scale	0000 0000	0010 1010

SG

On-chip signal ground output pin.

The potential is about a half of the supply voltage (VDD/2) and its forcing/sinking capability is 200 µA.

SGC

The bypass capacitor for the signal ground should be put between SGC and AG 0.1 µF low inductance capacitor, such as multilayer ceramic component is recommended.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating	Unit
V_{DD}	Supply voltage	-	0 ~ 7	V
V_{AIN}	Analog input voltage	-	-0.3 ~ V_{DD} + 0.3	V
V_{DIN}	Digital input voltage	-	-0.3 ~ V_{DD} + 0.3	V
T_{OP}	Operating temperature	-	-30 ~ + 85	°C
T_{stg}	Storage temperature	-	-55 ~ + 150	°C

Recommended Operating Conditions

Symbol	Parameter		Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage			+ 3.0	+ 3.3	+ 3.8	V
V_{AIN}	Analog input voltage		connect AIN - and GSX	-	-	1.4	VPP
V_{IH}	Digital input high voltage		XSYNC, RSYNC, BCLOCK, PCMIN, PDN, TMC	0.45*V_{DD}	-	V_{DD}	V
V_{IL}	Digital input low voltage			0	-	+ 0.16*V_{DD}	V
F_C	Bit clock frequency		BCLOCK	64, 128, 256, 288, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544			kHz
F_C	Sync pulse frequency		XSYNC, RSYNC	-	8.0	-	kHz
D_C	Clock duty cycle		BCLOCK	40	50	60	%
T_{IR}	Digital	Rise time	XSYNC, RSYNC, BCLOCK, PCMIN, PDN, TMC	-	-	50	ns
T_{IF}	Input	Fall time		-	-	50	ns
T_{XS}	Transmit sync timing		BCLOCK → XSYNC Ref Figl	100	-	-	ns
T_{SX}			XSYNC → BCLOCK Ref Figl	100	-	-	ns
T_{RS}	Receive sync timing		BCLOCK → RSYNC Ref Figl	100	-	-	ns
T_{SR}			RSYNC → BCLOCK Ref Figl	100	-	-	ns
T_{WS}	Sync pulse width		XSYNC, RSYNC	1BCLK	-	100	µs
T_{DS}	PCMIN set-up time		Ref Figl	100			ns
T_{DH}	PCMIN hold time		Ref Figl	100			ns
R_{DL}	Digital output load		Pull up resister	0.5	-	-	kΩ
C_{DL}				-	-	100	pF
V_{off}	Analog input allowable		Transmit gain : 0 dB	-100	-	+100	mV
	DC offset		Transmit gain : 20 dB	-10	-	+10	mV
	Allowable jitter		XSYNC, RSYNC			1000	ns

DC Characteristics (V_{DD} = +3.0 V ~ +3.8 V, T: −30 ~ 85°C)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{DD1}	Supply current	Operating mode	V_{DD} = 3.8 V	–	10.0	12.0	mA
			V_{DD} = 3.3 V	–	7.0	9.0	
IDD_2		Power down mode (PDN = 1) XSYNC or BCLOCK off		–	0.3	1.0	mA
IDD_3		Power down mode PDN = 0			0.01	0.1	mA
V_{IH}	Input high voltage			0.45*V	–	V_{DD}	V
V_{IL}	Input low voltage			0.0	–	0.16*V	V
I_{IH}	Input leakage current	VI = V_{DD}		–	–	2.0	µA
I_{IL}		VI=0V		–	–	0.5	µA
V_{OL}	Output low voltage	Pull-up : 0.5 kΩ		0.0	0.2	0.4	V
I_O	Output leakage current	PCMOUT		–	–	10	µA
C_{IN}	Input capacitance	All pins		–	5	–	pF

AC Characteristics (V_{DD} = +3.0 V ~ +3.8 V, T: −30 ~ 85°C)

Symbol	Parameter	Freq (Hz)	Level (dBm0)	Condition	Min	Typ	Max	Unit
Loss T1	Transmit frequency	60	0		20	26	–	dB
Loss T2	response	300			–0.15	0.00	0.20	dB
Loss T3		1 020			reference			dB
Loss T4		2 020			–0.15	–0.04	0.20	dB
Loss T5		3 000			–0.15	0.06	0.20	dB
Loss T6		3 400			0	0.40	0.80	dB
Loss R1	Receive frequency	300	0		–0.15	–0.03	0.20	dB
Loss R2	response	1 020			reference			dB
Loss R3		2 020			–0.15	–0.02	0.20	dB
Loss R4		3 000			–0.15	–0.15	0.20	dB
Loss R5		3 400			0.0	0.56	0.80	dB
SD T1	Transmit signal to		3	*1	35	43	–	
SD T2	distortion ratio		0		35	42	–	
SD T3		1 020	–30		35	39	–	dB
SD T4			–40		28	30.5	–	
SD T5			–45		23	25	–	
SD R1	Receive signal to		3	*1	36	43	–	
SD R2	distortion ratio		0		36	41	–	
SD R3		1 020	–30		36	41	–	dB
SD R4			–40		30	33	–	
SD R5			–45		24	27	–	

Note : *1 P-message filter.

Transmit Analog Interface (V_{DD} = +3.0 V ~ +3.8 V, T: −30 ~ 85°C)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
R_{INX}	Input resistance	AIN+, AIN−		10	–	–	MΩ
R_{LGX}	Output load resistance	GSX to SG		20	–	–	kΩ
C_{LGX}	Output load capacitance			–	–	50	pF
V_{OGX}	Output voltage			−0.7	–	+0.7	V
V_{OSGX}	Offset voltage		Gain=1	−20	–	20	mV

Receive Analog Interface (V_{DD} = +3.0 V ~ +3.8 V, T: −30 ~ 85°C)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
R_{INPW}	Input resistance	PWI		10	–	–	MΩ
R_{LVF}	Output load resistance	VFRO	to SG	20	–	–	kΩ
R_{LAO}		AOUT+, AOUT−	to SG	1.2	–	–	kΩ
C_{LVF}	Output load capacitance	VFRO		–	–	100	pF
C_{LAO}		AOUT+, AOUT−		–	–	50	pF
V_{OVF}	Output voltage	VFRO, RL=20KΩ	to SG	−1.0	–	1.0	V
V_{OAO}		AOUT+, AOUT−, RL=1.2KΩ	to SG	−1.3	–	1.3	V
V_{OSVF}	Offset voltage	VFRO	to SG	−100	–	100	mV
V_{OSAO}		AOUT+, AOUT− Gain=1	to SG	−100	–	100	mV

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AC Characteristics (V_{DD} = +3.0 V ~ +3.8 V, T: −30 ~ 85°C)

Symbol	Parameter	Freq (Hz)	Level (dBm0)	Condition	Min	Typ	Max	Unit
GT T1	Transmit gain tracking	1 020	3		−0.2		0.2	dB
GT T2			−10		reference			
GT T3			−40		−0.2		0.2	
GT T4			−50		−0.5		0.5	
GT T5			−55		−1.2		1.2	
GT R1	Receive gain tracking	1 020	3		−0.2		0.2	dB
GT R2			−10		reference			
GT R3			−40		−0.2		0.2	
GT R4			−50		−1.0		1.0	
GT R5			−55		−1.5		1.5	
Nidel T	Idle channel noise	–	–	AIN SG *2	–	−70	−68	dBm0
Nidel R		–	–	*2 *3	–	−76	−74	p
AV T	Absolute level	1 020	0	VDD=3.3 V	0.338	0.35	0.362	Vrms
AV R				T=25 °C *4	0.483	0.50	0.518	
AV Tt	Absolute level variation	1 020	0	VDD= +3 ~ 3.8 V	−0.2		0.2	dB
AV Rt	with temp and supply			T=−30 ~ 85 °C *4	−0.2		0.2	
Td	Absolute delay	1 020	0	A to A BCLOCK=64kHz	–	–	0.60	ms
Tgd T1	Transmit group delay	500	0	*5	–	0.19	0.75	ms
Tgd T2		600			–	0.11	0.35	
Tgd T3		1 000			–	0.02	0.125	
Tgd T4		2 600			–	0.05	0.125	
Tgd T5		2 800			–	0.07	0.75	

Notes : *2 P-message filter
*3 PCM input data : code "0"
*4 AVR defined at VFR0
*5 The minimum value of the group delay distortion should be refered as 0 ms

AC Characteristics (V_{DD} = +3.0 V ~ +3.8 V, T: −30 ~ 85°C)

Symbol	Parameter	Freq (Hz)	Level (dBm0)	Condition	Min	Typ	Max	Unit
Tgd R1	Receive group delay	500	0	*6	–	0.00	0.75	ms
Tgd R2		600			–	0.00	0.35	
Tgd R3		1 000			–	0.00	0.125	
Tgd R4		2 600			–	0.09	0.125	
Tgd R5		2 800			–	0.12	0.75	
CR T	Crosstalk attenuation	1 020	0	TRANS →RECV	75	85	–	dB
CR R				RECV → TRANS	65	70	–	
DIS	Discrimination	4.6K ~ 72K	0	0 ~ 4000Hz	30	32	–	dB
S	Out-of-band spurious	300 ~ 3 400	0	4.6K ~ 100kHz	–	–37.5	–35	dBm0
IMD	Intermodulation distortion	fa=470 fa=320	–4	2fa–fb	–	–52	–35	dBm0
	D to D mode gain	1 020	0	TMC=1 PCNIN to PCMOUT	–1.0		1.0	dB
PSR T	PSRR	0 ~ 50K	30 mVpp	Inband	–	30	–	dB
PSR R								
Tsd	Digital output delay time	CL=100pF			50		200	ns
Txd1					50		200	
Txd2					50		200	
Txd3					50		200	

Notes: *6 The minimum value of the group delay should be referred as 0ms.

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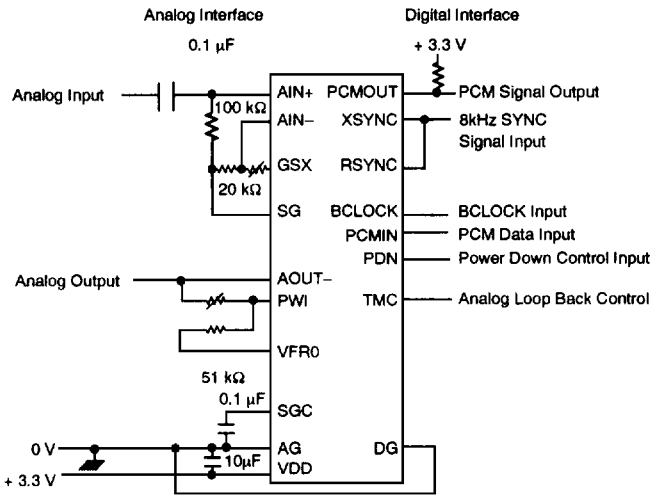
Application



Frequency Response Adjustement

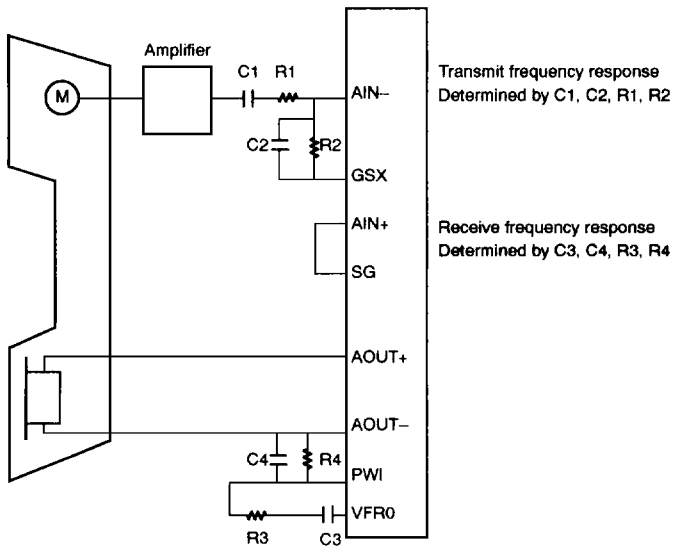
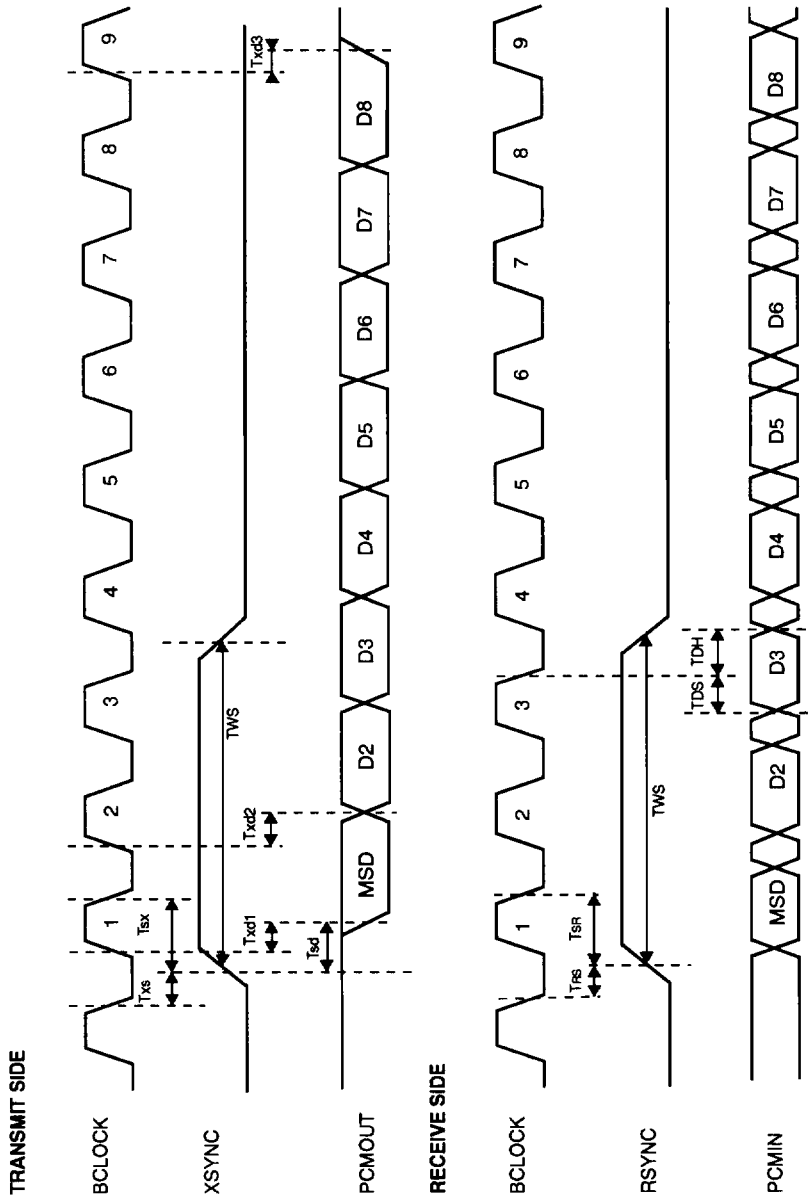


Figure 1.


TRANSMIT SIDE
BCLOCK
XSYNC
PCMOUT
RECEIVE SIDE
BCLOCK
RSYNC
PCMIN
Txd3
TWS
Txd2
Txd1
Tsx
Txs
Tsd
TSR
Trs
TDH
TDS
MSD
D2
D3
D4
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Ordering Information