DI CMOS Protected Analog Switches

AD7510DI/AD7511DI/AD7512DI

FEATURES
Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Monolithic Dielectrically Isolated CMOS
Standard 14-/16-Pin DIPs and
20-Terminal Surface Mount Packages

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (500pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged either in a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

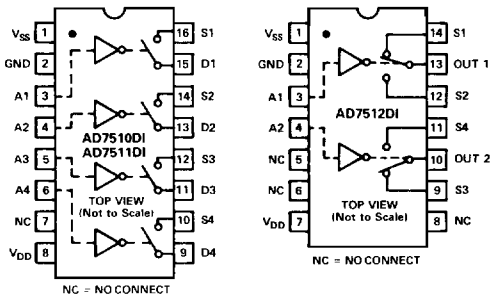
ORDERING INFORMATION[1]

Temperature Range and Package[2]		
0 to +70°C	−25°C to +85°C	−55°C to +125°C
Plastic DIP[3]	**Hermetic[4]**	**Hermetic[4]**
AD7510DIJN	AD7510DIJQ	AD7510DISQ
AD7510DIKN	AD7510DIKQ	AD7510DITQ
AD7511DIJN	AD7511DIJQ	AD7511DITQ
AD7511DIKN	AD7511DIKQ	AD7512DISQ
AD7512DIJN	AD7512DIJQ	AD7512DITQ
AD7512DIKN	AD7512DIKQ	
PLCC[5] (P-20A)		**LCCC[6] (E-20A)**
AD7510DIJP		AD7510DISE
AD7510DIKP		AD7511DISE
AD7511DIJP		AD7511DITE
AD7511DIKP		AD7512DISE
AD7512DIJP		AD7512DITE
AD7512DIKP		

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[2]See Section 14 for package outline information.
[3]For AD7510DIJN/KN and AD7511DIJN/KN package outline N-16; for AD7512DIJN/KN package outline N-14.
[4]For AD7510DIJQ/KQ/SQ and AD7511DIJQ/KQ/SQ/TQ package outline Q-16; for AD7512DIJQ/KQ/SQ/TQ package outline Q-14.
[5]PLCC: Plastic Leaded Chip Carrier.
[6]LCCC: Leadless Ceramic Chip Carrier.

AD7510DI/AD7511DI/AD7512DI FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

DIP



CONTROL LOGIC

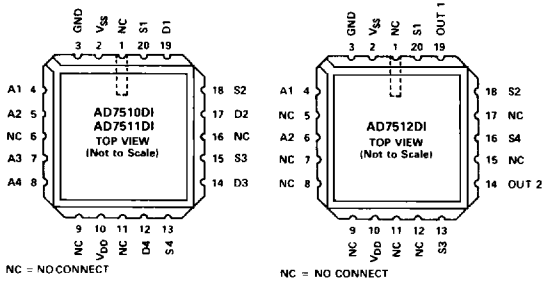
AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

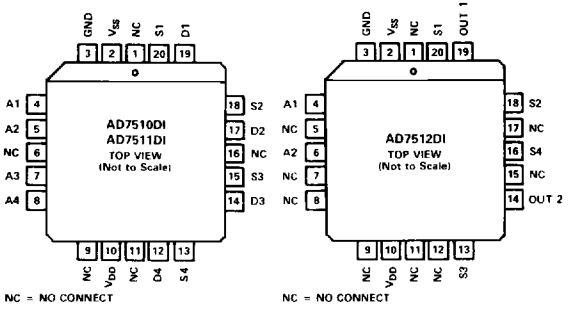
AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

PIN CONFIGURATIONS

LCCC



PLCC



SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V unless otherwise noted)

COMMERCIAL AND INDUSTRIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C (N, P, Q, E)	0 to +70°C (N, P) -25°C to +85°C (Q)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	J, K	75Ω typ, 100Ω max	175Ω max	−10V ≤ V_D ≤ +10V
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		
R_{ON} Match	All	J, K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S)$_{OFF}$[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = −10V, V_S = +10V and V_D = +10V, V_S = −10V
I_D (I_S)$_{ON}$[1]	All	J, K	10nA max		V_S = V_D = +10V V_S = V_D = −10V
I_{OUT}[1]	AD7512DI	J, K	15nA max	1500nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
DIGITAL CONTROL					
V_{INL}[1]	All	J, K		0.8V max	
V_{INH}[1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	7pF typ		
I_{INH}[1]	All	J, K	10nA max		V_{IN} = V_{DD}
I_{INL}[1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		
	AD7511DI	J, K	350ns typ		V_{IN} = 0 to +3.0V
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)$_{OFF}$	All	J, K	8pF typ		
C_S (C_D)$_{ON}$	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to −10V
POWER SUPPLY					
I_{DD}[1]	All	J, K	800µA max	800µA max	All digital inputs = V_{INH}
I_{SS}	All	J, K	800µA max	800µA max	
I_{DD}[1]	All	J, K	500µA max	500µA max	All digital inputs = V_{INL}
I_{SS}[1]	All	J, K	500µA max	500µA max	

PACKAGE OPTIONS[2]

Plastic (N-14)	AD7512DIJN/KN	✓
Plastic (N-16)	AD7510DIJN/KN	✓
	AD7511DIJN/KN	
Cerdip (Q-14)	AD7512DIJQ/KQ	✓
Cerdip (Q-16)	AD7510DIJQ/KQ	✓
	AD7511DIJQ/KQ	✓
PLCC (P-20A)	AD7510DIJP/KP	✓
	AD7511DIJP/KP	
	AD7512DIJP/KP	

NOTES
[1] 100% tested.
[2] See Section 14 for package outline information.

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

EXTENDED VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ I_{DS} = 1mA
I_D $(I_S)_{OFF}$[1]	All	S, T	3nA max	200nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D $(I_S)ON$[1]	All	S, T	10		$V_S = V_D$ = +10V and $V_S = V_D$ = -10V
I_{OUT}[1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}[1]	All	S, T		0.8V max	
V_{INH}[1,2]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH}[1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL}[1]	All	S, T	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}[3]	AD7510DI	S,	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF}[3]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$[3]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD}[1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS}[1]	All	S, T		800μA max	
I_{DD}[1]	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS}[1]	All	S, T		500μA max	
PACKAGE OPTIONS[4]					
Cerdip (Q-16)	AD7510DISQ				
	AD7511DISQ/TQ				
Cerdip (Q-14)	AD7512DISQ/TQ				
LCCC (E-20A)	AD7510DISE				
	AD7511DISE/TE				
	AD7512DISE/TE				

NOTES
[1] 100% tested.
[2] A pullup resistor, typically 1-2kΩ is required to make AD7511DISQ and AD7512DISQ TTL compatible.
[3] Guaranteed, not production tested.
[4] See Section 14 for package outline information.
Specifications subject to change without notice.

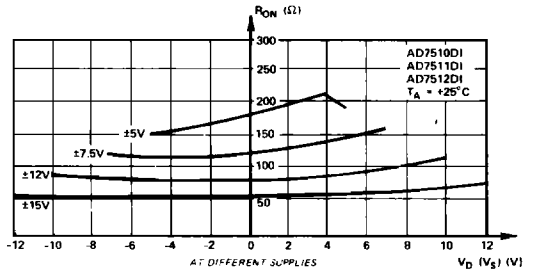
ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . −17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . . V_{DD} +25V
or V_{SS} −25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} −20V
or 20mA, Whichever Occurs First
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . 0V to V_{DD} +0.3V
Power Dissipation (Any Package)
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

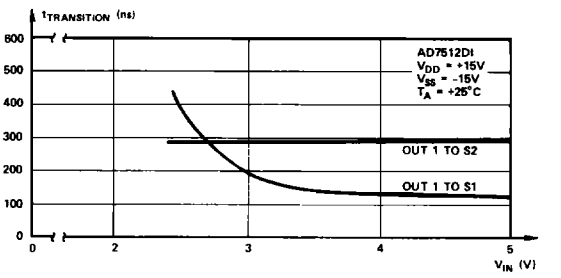
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature
Commercial (JN, KN, JP, KP Versions) . . . . 0 to +70°C
Industrial (JQ, KQ Versions) . . . . . −25°C to +85°C
Extended (SQ, TQ, SE, TE Versions) . . −55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

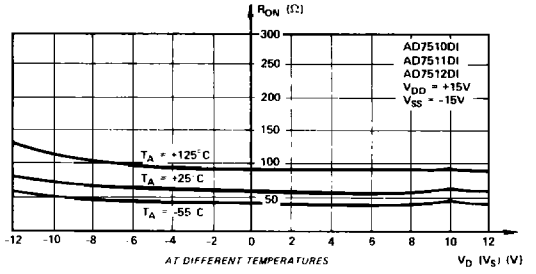
Typical Performance Characteristics



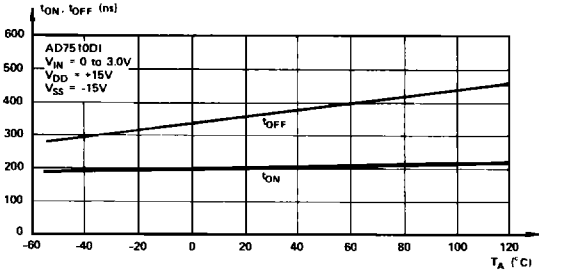
R_{ON} as a Function of V_D (V_S)



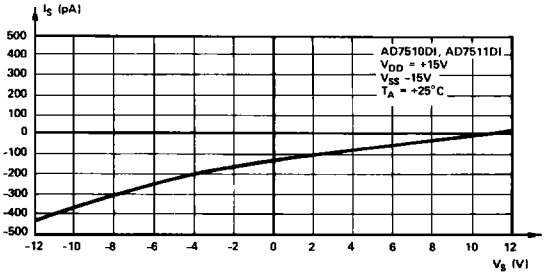
$t_{TRANSITION}$ as a Function of Digital Input Voltage



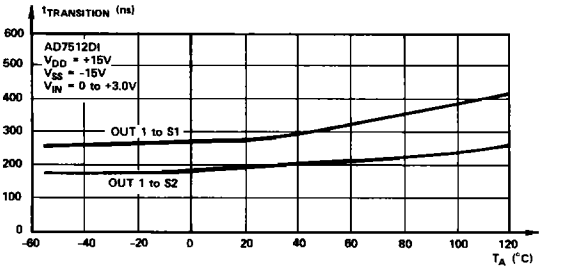
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature



I_S, $(I_D)_{OFF}$ vs V_S



$t_{TRANSITION}$ as a Function of Temperature