FEATURES

- 8.0V ~ 18.0V Power supply.
- High output power capability:
  2 x 30W/**4Ω/BTL** @16V,1KHz,THD+N=10%.
  2 x 18W/**4Ω/BTL** @12V,1KHz,THD+N=10%.
  2 x 23W/8Ω/BTL @18V,1KHz,THD+N=10%.
  2 x 18W/8Ω/BTL @16V,1KHz,THD+N=10%.
  2 x 10W/8Ω/BTL @12V,1KHz,THD+N=10%.
  4 x 11W/**4Ω/SE** @18V,1KHz,THD+N=10%.
  4 x 5W/**4Ω/SE** @12V,1KHz,THD+N=10%.
  4 x 6W/8Ω/SE @18V,1KHz,THD+N=10%.
  4 x 3W/8Ω/SE @12V,1KHz,THD+N=10%.
- 3 kinds of Output type options:
  4xSE、2xBTL、2.1Ch.(2xSE+1xBTL)
- **Include High/Low Pass Filter OP.**
- Short-Circuit Protection with automatic recovery.
- Over-Heat Protection with automatic recovery.
- Mute function selectable.
- Lead free and green package available.
  (RoHS Compliant)
- Space saving package :
  -- 48-pin LQFP 7*7 package.

GENERAL DESCRIPTION

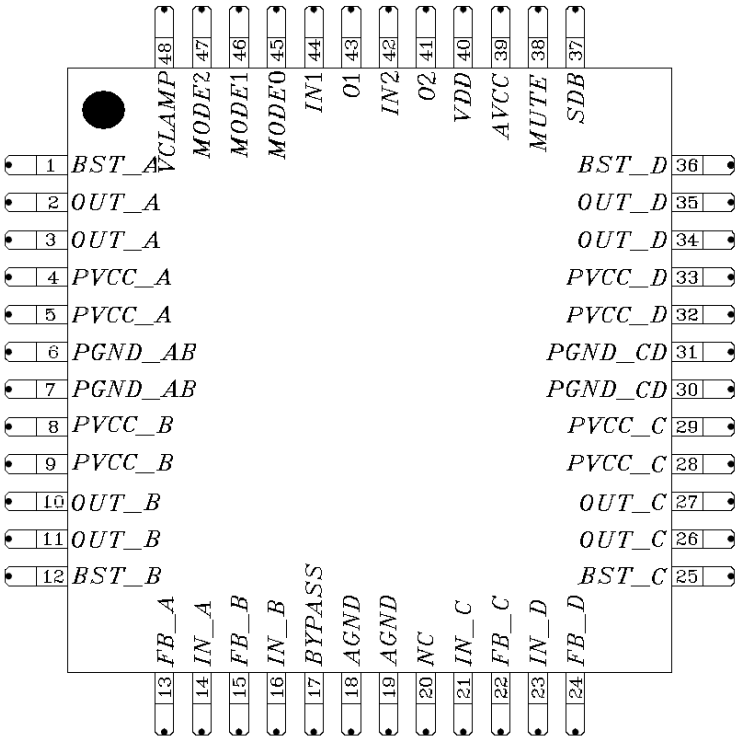
The LY8321 is a high efficiency class D audio power amplifier. It can to work either in dual bridge or quad single-ended output and 2.1 channel application configuration.
The device features a low noise and a low power consumption in shutdown mode and support thermal shutdown protection. It also utilizes circuitry to reduce low noise during device turn-on.
The outputs are also fully protected against short to output-to-output pin. The short-circuit protection and thermal protection include an auto-recovery feature.

APPLICATION

- Soundbar Home Theater.
- Powered Speakers.
- Music instrument devices.
- DVD players, Game machines.
- Multimedia TFT LCD TVs / Monitors.

PIN CONFIGURATION

LY8321 LQFP48 pin configuration
(TOP VIEW)



5F, No. 2, Industry E . Rd. IX, Science-Based Industrial Park, Hsinchu 300, Taiwan
TEL: 886-3-6668838
FAX: 886-3-6668836

PIN DESCRIPTION

SYMBOL	Pin No.	DESCRIPTION
BST_A	1	Bootstrap I/O for A channel.
OUT_A	2/3	Speaker output for A channel.(SE Mode=VOUT+) (BTL Mode=Left channel VOUT+)
PVCC	4/5/8/9/28/29/32/33	Power supply of A、B、C、D channel.
PGND	6/7/30/31	Ground of A、B、C、D channel.
OUT_B	10/11	Speaker output for B channel. (SE Mode=VOUT+) (BTL Mode=Left channel VOUT-)
BST_B	12	Bootstrap I/O for B channel.
FB_A	13	A-Channel Feedback. Connect feedback resistor between FB_A and IN_A to set amplifier gain.
IN_A	14	Input of A channel.
FB_B	15	B-Channel Feedback. Connect feedback resistor between FB_B and IN_B to set amplifier gain.
IN_B	16	Input of B channel.
BYPASS	17	Bypass pin.
AGND	18/19	Analog GND.
NC	20	No connect.
IN_C	21	Input of C channel.
FB_C	22	C-Channel Feedback. Connect feedback resistor between FB_C and IN_C to set amplifier gain.
IN_D	23	Input of D channel.
FB_D	24	D-Channel Feedback. Connect feedback resistor between FB_D and IN_D to set amplifier gain.
BST_C	25	Bootstrap I/O for C channel.
OUT_C	26/27	Speaker output for C channel. (SE Mode=VOUT+) (BTL Mode=Right channel VOUT+)
OUT_D	34/35	Speaker output for D channel. (SE Mode=VOUT+) (BTL Mode=Left channel VOUT-)
BST_D	36	Bootstrap I/O for D channel.
SDB	37	Shutdown control pin.(when **LOW** level in shutdown mode).
MUTE	38	Mute signal for quick enable/disable of output. (when **High** level in mute mode).
AVCC	39	Analog Power supply.
VDD	40	Regulator output terminal.(with external capacitor)
O2	41	Pure OP Output 2.
IN2	42	Pure OP Negative input 2.
O1	43	Pure OP Output 1.
IN1	44	Pure OP Negative input 1
Mode 0/1/2	45/46/47	Output mode selectable.
VCLAMP	48	Internally generated voltage power supply for all channel bootstrap capacitors.

▪ ORDERING INFORMATION

Ordering Code	Speaker Channels	Pin/ Package	Output Power (THD+N=10%)	Input Type	Output Type
LY8321F	Multi channel	LQFP48	2 x 30W/**4Ω/BTL** @16V *3 2 x 18W/**4Ω/BTL** @12V. 2 x 23W/8Ω/BTL @18V 2 x 18W/8Ω/BTL @16V 2 x 10W/8Ω/BTL @12V 4 x 11W/**4Ω/SE** @18V *3 4 x 5W/**4Ω/SE** @12V 4 x 6W/8Ω/SE @18V 4 x 3W/8Ω/SE @12V	SE	4xSE、 2xBTL、 2xSE+1xBTL (2.1Ch.)

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

▪ DEMO BOARD ORDERING INFORMATION

Demo Board Ordering Code	Pin/ Package	Input Type	Speaker Output Channels	Notes
LY8321F-DB1	LQFP48	SE	PBTL mode (Mono)	
LY8321F-DB2			BTLx2 mode (Stereo)	
LY8321F-DB3			2.1 mode (SEx2+BTLx1)	
LY8321F-DB4			SEx4 mode	

TYPICAL APPLICATION CIRCUIT

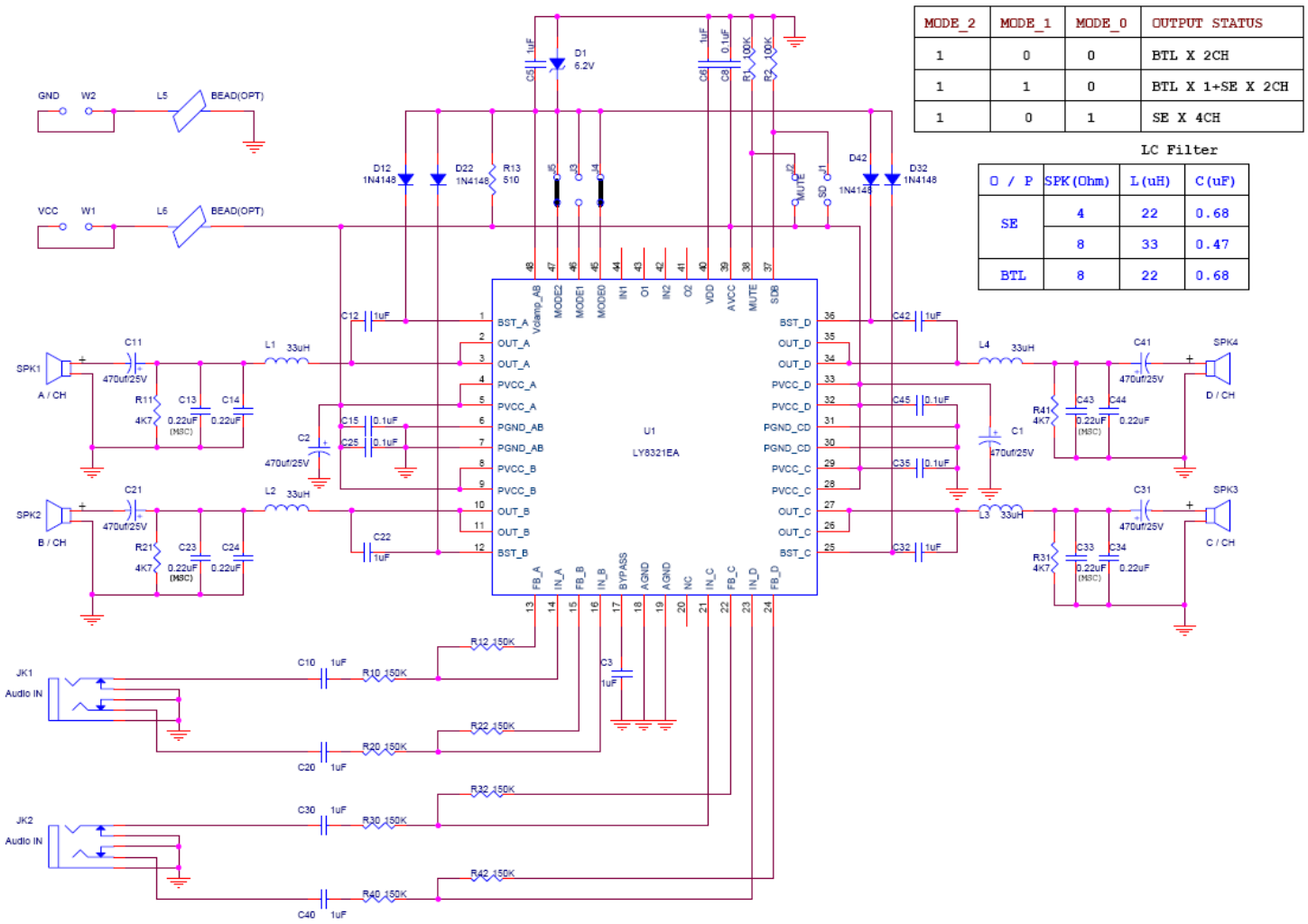


Figure 1. LY8321 Application Circuit with 4xSE Schematic

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

MODE_2	MODE_1	MODE_0	OUTPUT STATUS
1	0	0	BTL X 2CH
1	1	0	BTL X 1+SE X 2CH
1	0	1	SE X 4CH

LC Filter

O / P	SPK(Ohm)	L(uH)	C(uF)
SE	4	22	0.68
	8	33	0.47
BTL	8	22	0.68

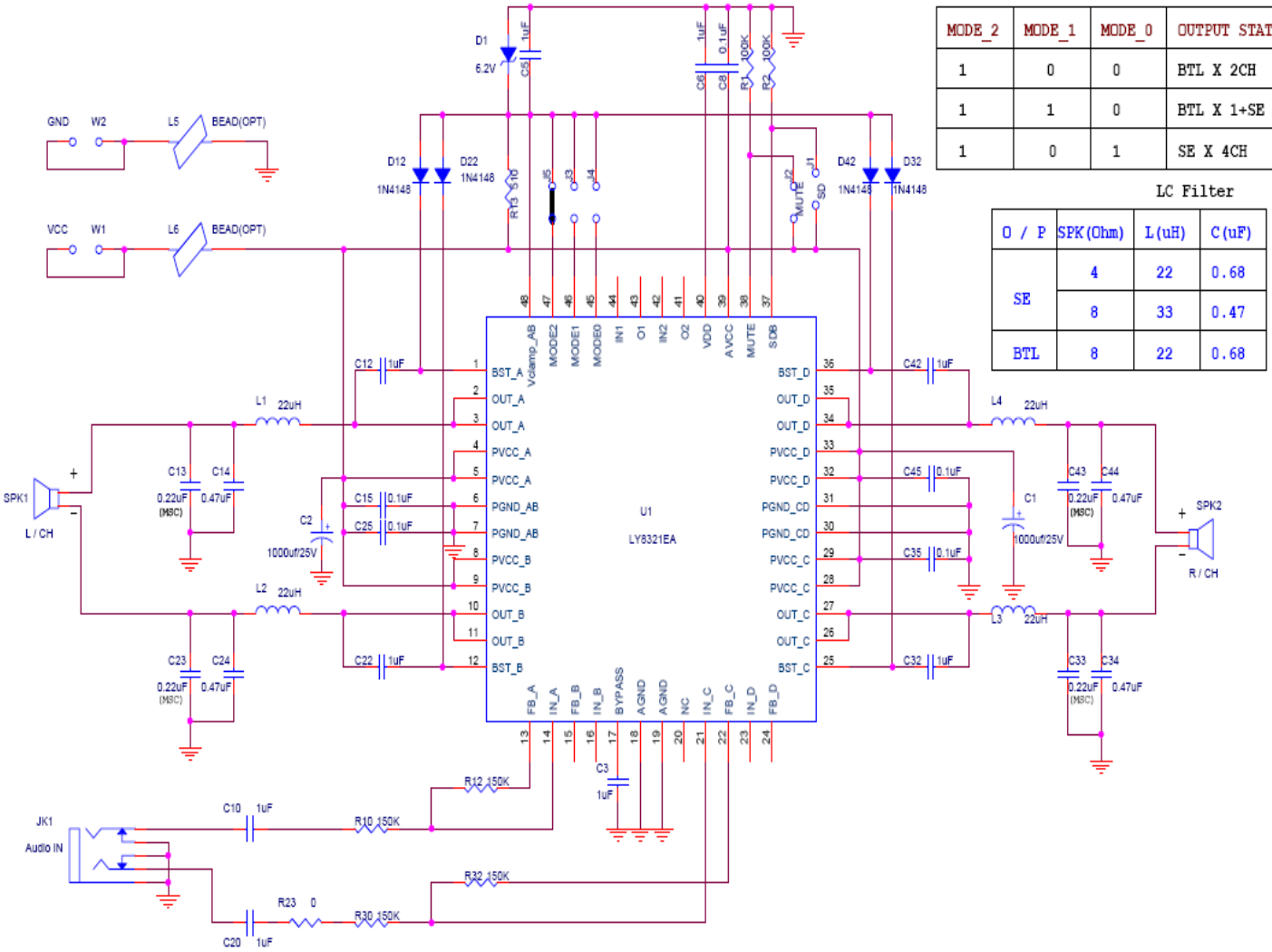


Figure 2. LY8321 Application Circuit with 2x BTL Schematic

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

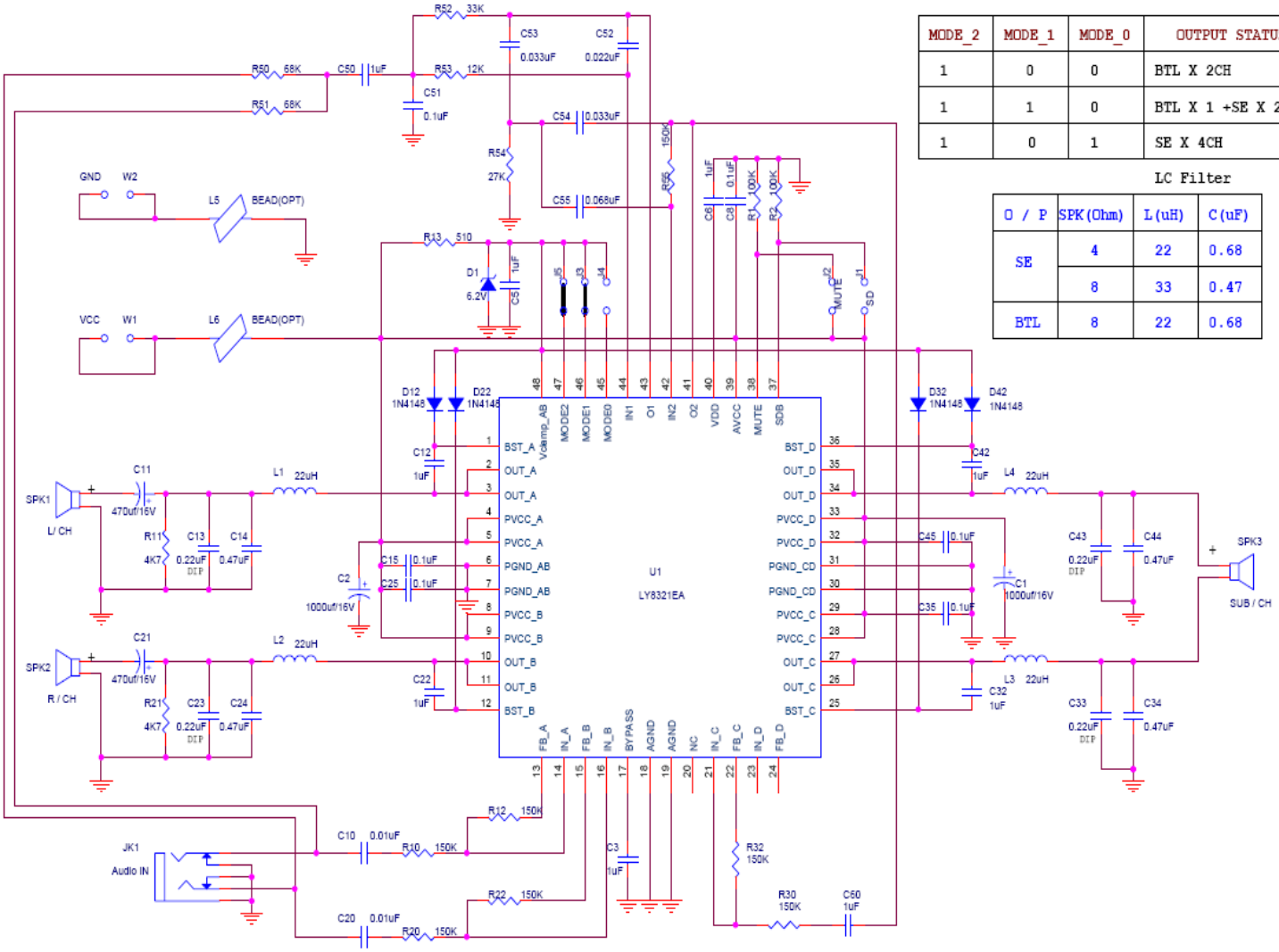


Figure 3. LY8321 Application Circuit with 2x SE+1x BTL Schematic

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	PVCC	20.0	V
Operating Temperature	T_A	-40 to 85 (I grade)	℃
Input Voltage	V_I	-0.3V to PVCC +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	℃
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	℃

ELECTRICAL CHARACTERISTICS (1) (T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *2	MAX.	UNIT
Power supply voltage	PVCC		8.0	-	18.0	V
High-level input voltage	V_{SDIH}	PVCC=8~18V	2.0	-	PVCC	
Low-level input voltage	V_{SDIL}	PVCC=8~18V	0	-	0.3	
Quiescent Current	I_Q	PVCC=12V, SD≧2.0V, MUTE=0V, No Load	-	35	-	mA
Quiescent Current (in mute mode)		PVCC=12V, MUTE≧0.8V, No Load	-	35	-	
Shutdown Current	I_{SD}	PVCC=12V,$V_{SHUTDOWN}$≦0.8V, No Load	-	0.2	-	
Drain-source on-state resistance	Rdson	PVCC=12V, Io=1A	-	360	-	mΩ
Bypass output voltage	V_{BYPASS}	No Load	-	PVCC/6	-	V
Output offset voltage	$\|V_{OS}\|$	PVCC=12V, V_I=0V, Av=10, BTL mode	-	100	-	mV

(*2) Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at PVCC = PVCC(TYP.) and T_A = 25℃

▪ OPERATING CHARACTERISTICS (2)(T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. *2	MAX.	UNIT
Supply ripple rejection	Ksvr	PVCC=12V, Av=10, Vripple = 200mVpp at 1kHz, R_L=4Ω, BTL mode	217Hz Input=GND	-	-77	-	dB
			217Hz Input=Floating	-	-78	-	
Output voltage noise	Vn	**SE Mode**, PVCC=12V, Av=10, f = 20 Hz to 20 kHz,R_L=4Ω,	A weighting	-	249	-	uV
			Without A weighting	-	336	-	
		BTL Mode, PVCC=12V, Av=10, f = 20 Hz to 20 kHz,R_L=4Ω,	A weighting	-	355	-	
			Without A weighting	-	499	-	
Signal-to-noise ratio	SNR	**SE mode**, PVCC=12V, Av=10, R_L=4Ω, Max output THD+N<1%,	A weighting	-	85	-	dB
			Without A weighting	-	82	-	
		BTL mode, PVCC=12V, Av=10, R_L=4Ω, Max output THD+N<1%,	A weighting	-	87	-	
			Without A weighting	-	84	-	
Crosstalk	Cs	**SE mode**, PVCC=12V, Av=10, R_L=4Ω, Po = 0.25W,	A ch. to B ch.	-	-76	-	dB
			B ch. to A ch.	-	-74	-	
			C ch. to D ch.	-	-68	-	
			D ch. to C ch.	-	-67	-	
		BTL mode, PVCC=12V, Av=10, R_L=4Ω, Po = 0.25W,	A ch. to C ch.	-	-78	-	dB
			C ch. to A ch.	-	-81	-	

(*2) Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at PVCC = PVCC(TYP.) and T_A = 25℃

▪ OPERATING CHARACTERISTICS (3)(T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *2	MAX.	UNIT
Oscillator frequency	fosc		-	316	-	kHz
Thermal shutdown temperature	TSD	Shutdown temp.	-	180	-	℃
		Restore temp.	-	160	-	
Mute attenuation		VDD=12V, Po=1W	-	-92	-	dB
Mute delay	Δt mute	VDD=12V, Time from mute input switches high until outputs muted.	-	780	-	us
Unmute delay	Δt mute	Time from mute input switches low until outputs muted.	-	740	-	
Start-up time from shutdown	ZI	PVCC=18V, C_{bypass}=1μF.	-	700	-	ms
		PVCC=12V, C_{bypass}=1μF.	-	640	-	
		PVCC=8V, C_{bypass}=1μF.	-	580	-	

▪ OPERATING CHARACTERISTICS (4)(T_A = 25℃)

R_L=4Ω

PARAMETER	SYMBOL	TEST CONDITION				MIN.	TYP. *2	MAX.	UNIT
Out Power / Channel	Po	RL=4Ω f=1kHz,	THD+N =10%	BTL output	PVCC=8V	-	8	-	W
					PVCC=10V	-	12.5	-	
					PVCC=12V	-	18	-	
					PVCC=14V	-	24 *3	-	
					PVCC=16V	-	30 *3	-	
					-	-	-	-	
				SE output	PVCC=8V	--	2.5	-	
					PVCC=10V	-	3.5	-	
					PVCC=12V	-	5	-	
					PVCC=14V	-	6.8	-	
					PVCC=16V	-	9	-	
					PVCC=18V	-	11	-	
			THD+N =1%	BTL output	PVCC=8V	-	5.5	-	
					PVCC=10V	-	7.6	-	
					PVCC=12V	-	14	-	
					PVCC=14V	-	17 *3	-	
					PVCC=16V	-	20 *3	-	
					-	-	-	-	
				SE output	PVCC=8V	-	1.8	-	
					PVCC=10V	-	2.2	-	
					PVCC=12V	-	3.4	-	
					PVCC=14V	-	4.5	-	
					PVCC=16V	-	5.5	-	
					PVCC=18V	-	7	-	

(*2) Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at PVCC = PVCC(TYP.) and T_A = 25℃

(*3) When driving BTL stereo 4Ω loads mode from ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink..

▪ OPERATING CHARACTERISTICS (5)(T_A = 25℃)

R_L=8Ω

PARAMETER	SYMBOL	TEST CONDITION				MIN.	TYP. *2	MAX.	UNIT
Out Power / Channel	Po	R_L=8Ω f=1kHz,	THD+N =10%	BTL output	PVCC=8V	-	4.5	-	W
					PVCC=10V	-	7	-	
					PVCC=12V	-	10	-	
					PVCC=14V	-	14	-	
					PVCC=16V	-	18 *3	-	
					PVCC=18V	-	23 *3	-	
				SE output	PVCC=8V	-	1.2	-	
					PVCC=10V	-	2	-	
					PVCC=12V	-	3	-	
					PVCC=14V	-	4	-	
					PVCC=16V	-	5	-	
					PVCC=18V	-	6	-	
			THD+N =1%	BTL output	PVCC=8V	-	3.2	-	
					PVCC=10V	-	5.5	-	
					PVCC=12V	-	8	-	
					PVCC=14V	-	9	-	
					PVCC=16V	-	13.5 *3	-	
					PVCC=18V	-	16 *3	-	
				SE output	PVCC=8V	-	0.8	-	
					PVCC=10V	-	1.2	-	
					PVCC=12V	-	1.7	-	
					PVCC=14V	-	2.5	-	
					PVCC=16V	-	3	-	
					PVCC=18V	-	4.2	-	

(*2) Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at PVCC = PVCC(TYP.) and T_A = 25℃

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4
THD+N vs. Output Power (@ Output type=BTL Mode, **RL=4Ω**, f=1kHz, AV=10)

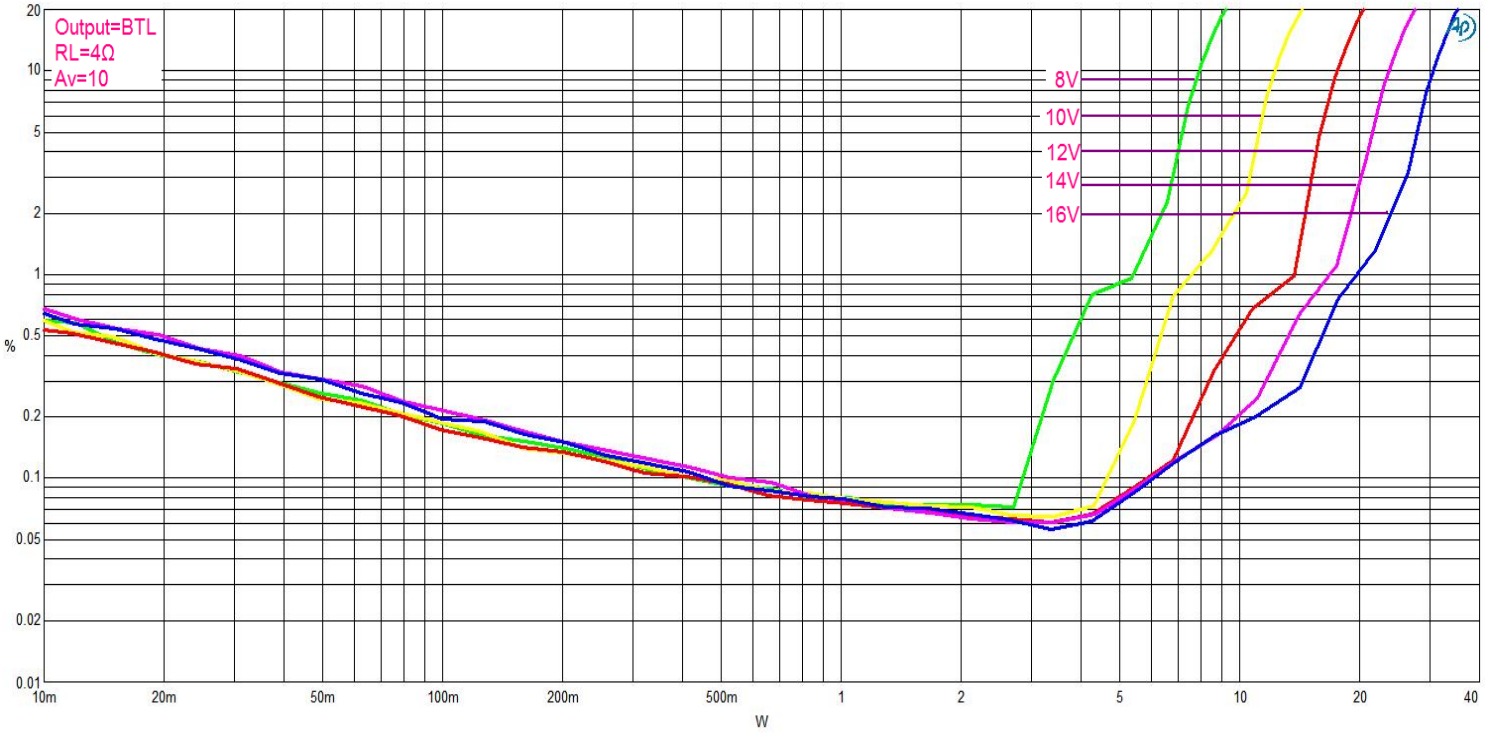


Figure 5
THD+N vs. Output Power (@ Output type=BTL Mode, **RL=8Ω**, f=1kHz, AV=10)

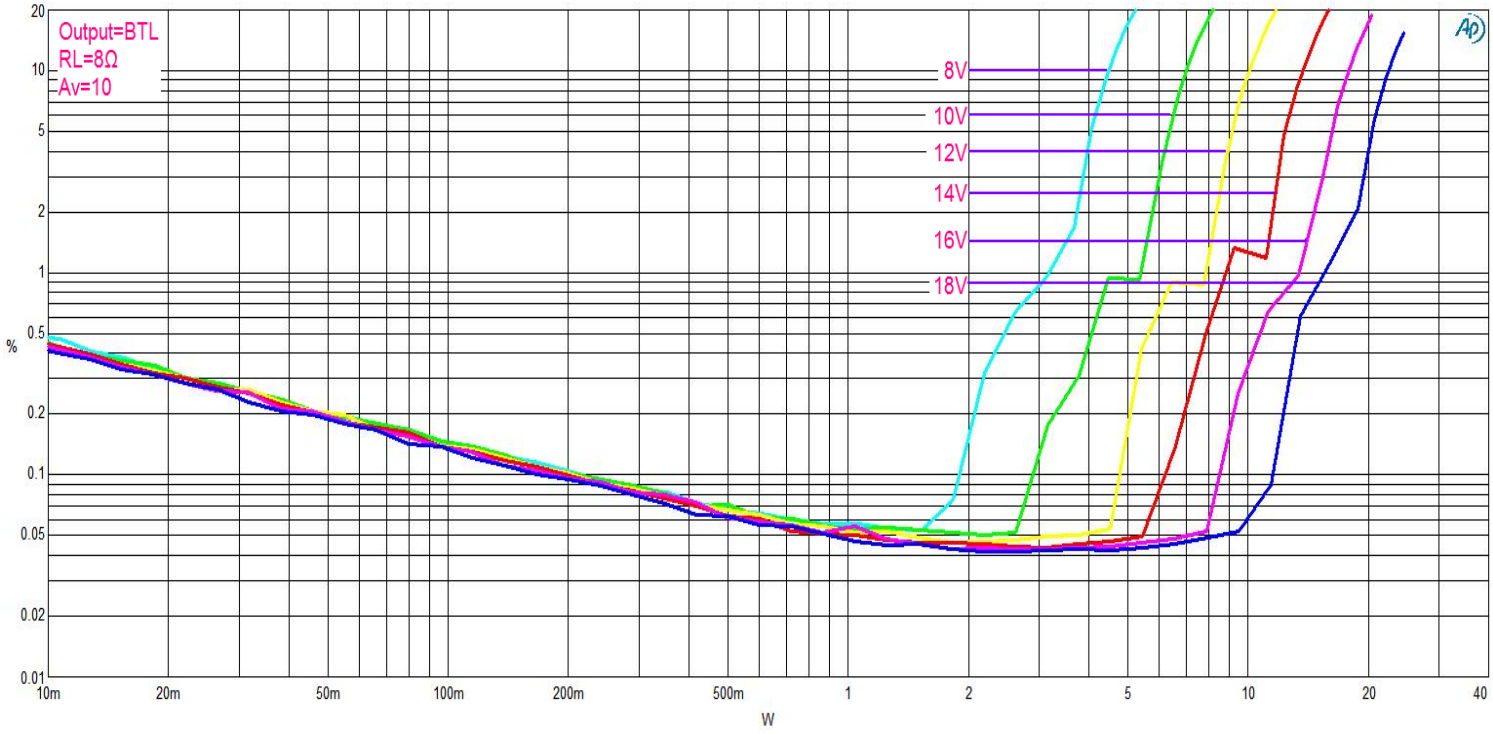


Figure 6
THD+N vs. Output Power (@ Output type=SE Mode, **RL=4Ω**, f=1kHz, AV=10)

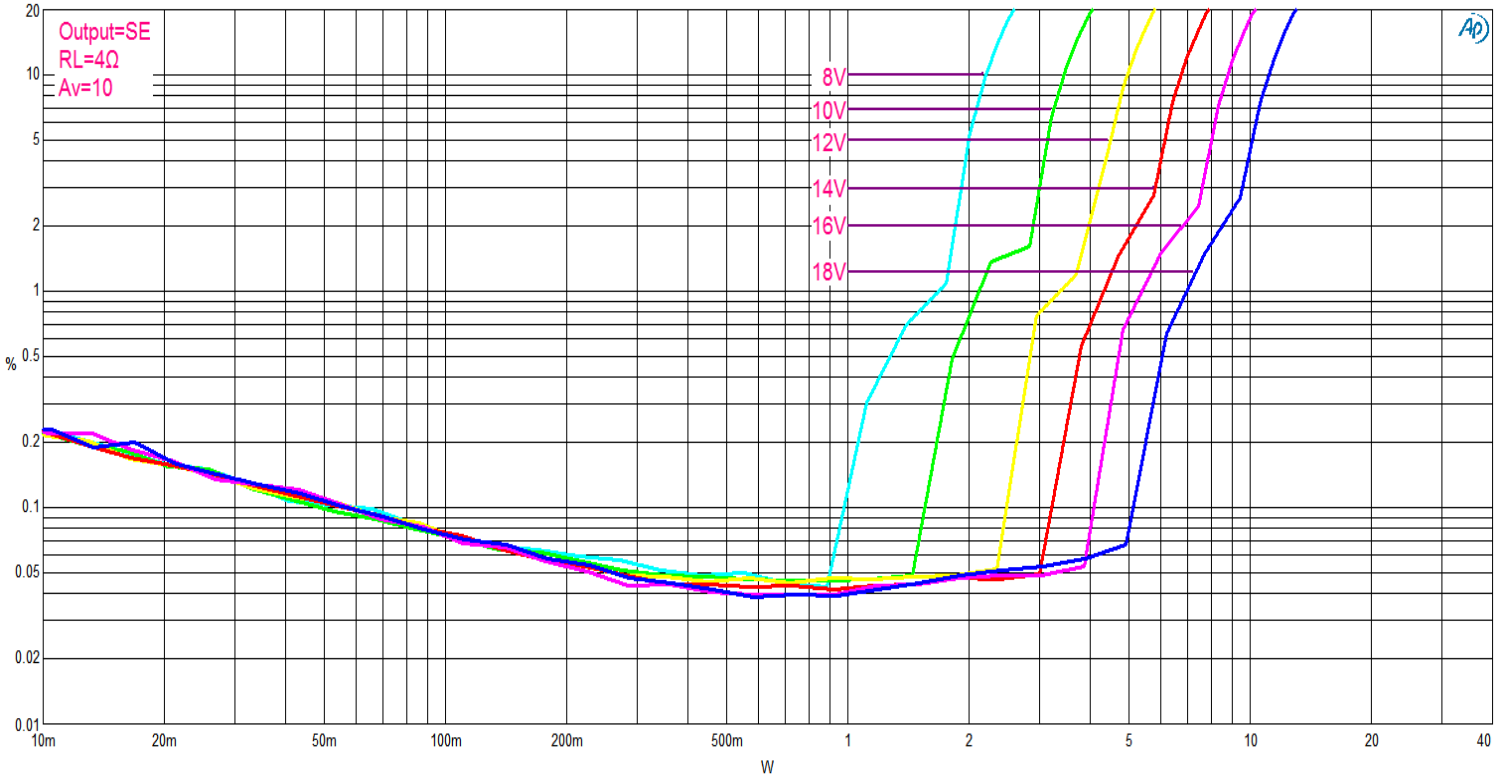


Figure 7
THD+N vs. Output Power (@ Output type=SE Mode, **RL=8Ω**, f=1kHz, AV=10)

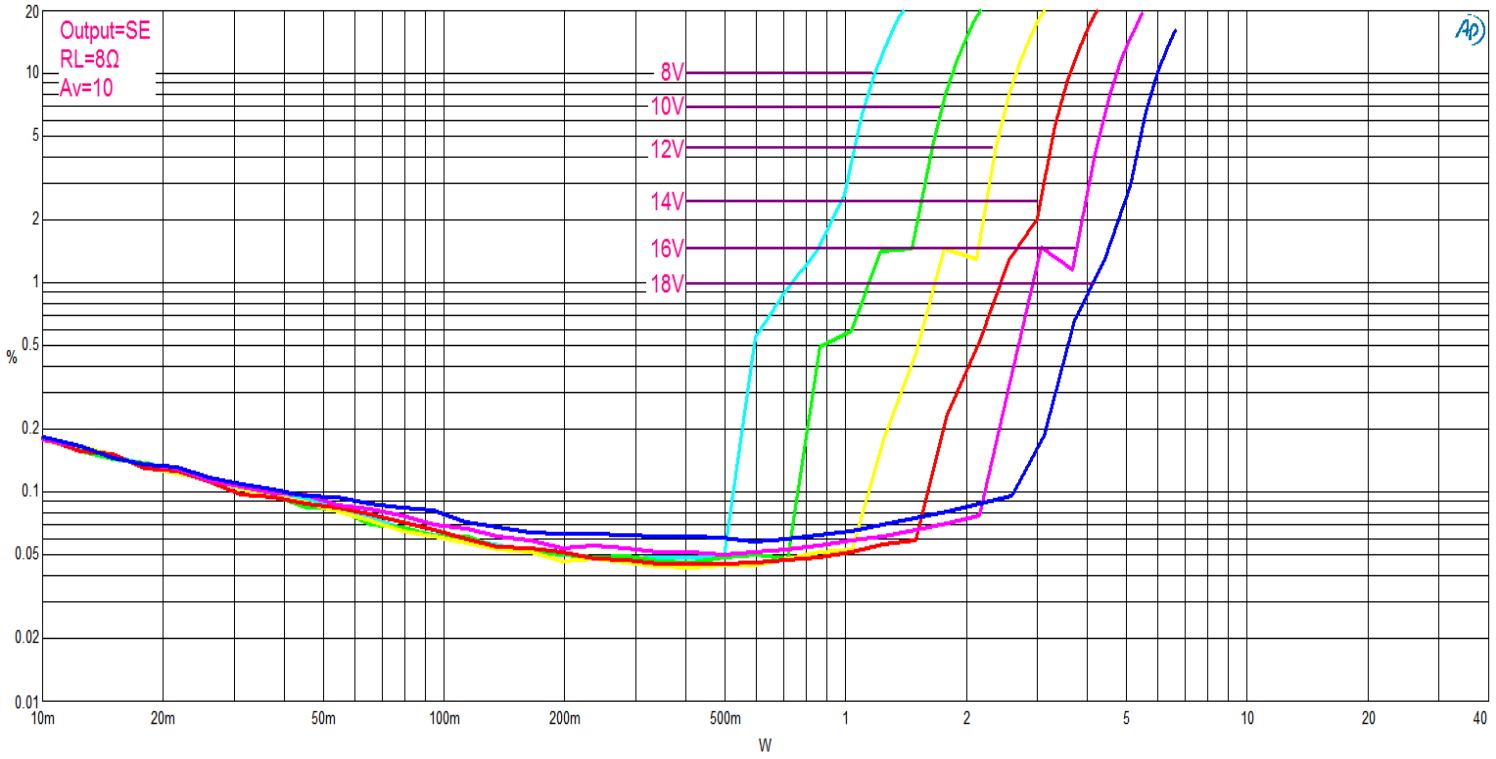


Figure 8
Supply ripple rejection (Ksvr, **RL=4Ω**, BTL mode)

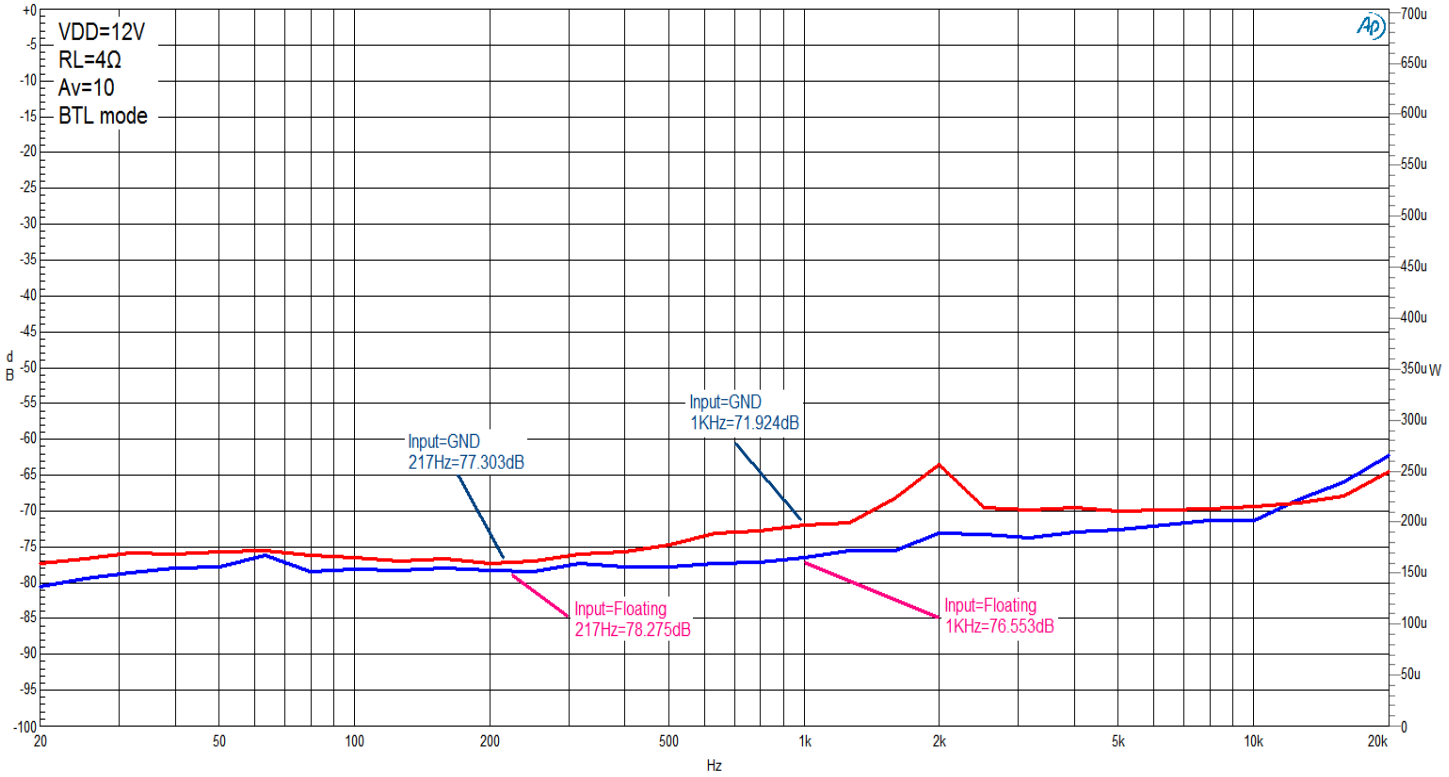


Figure 8
Supply ripple rejection (Ksvr, **RL=8Ω**, BTL mode)

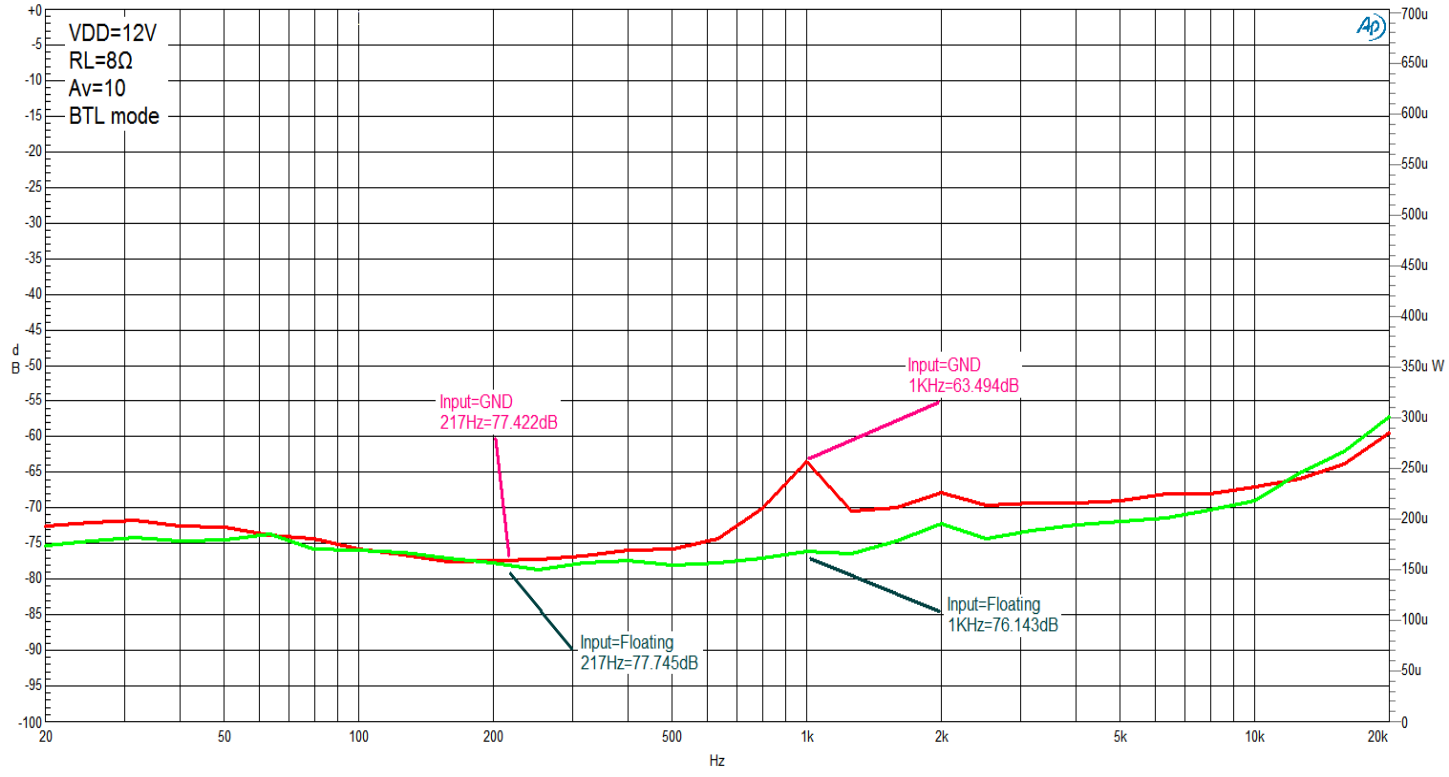


Figure 10
Supply ripple rejection (Ksvr, **RL=4Ω**, SE mode)

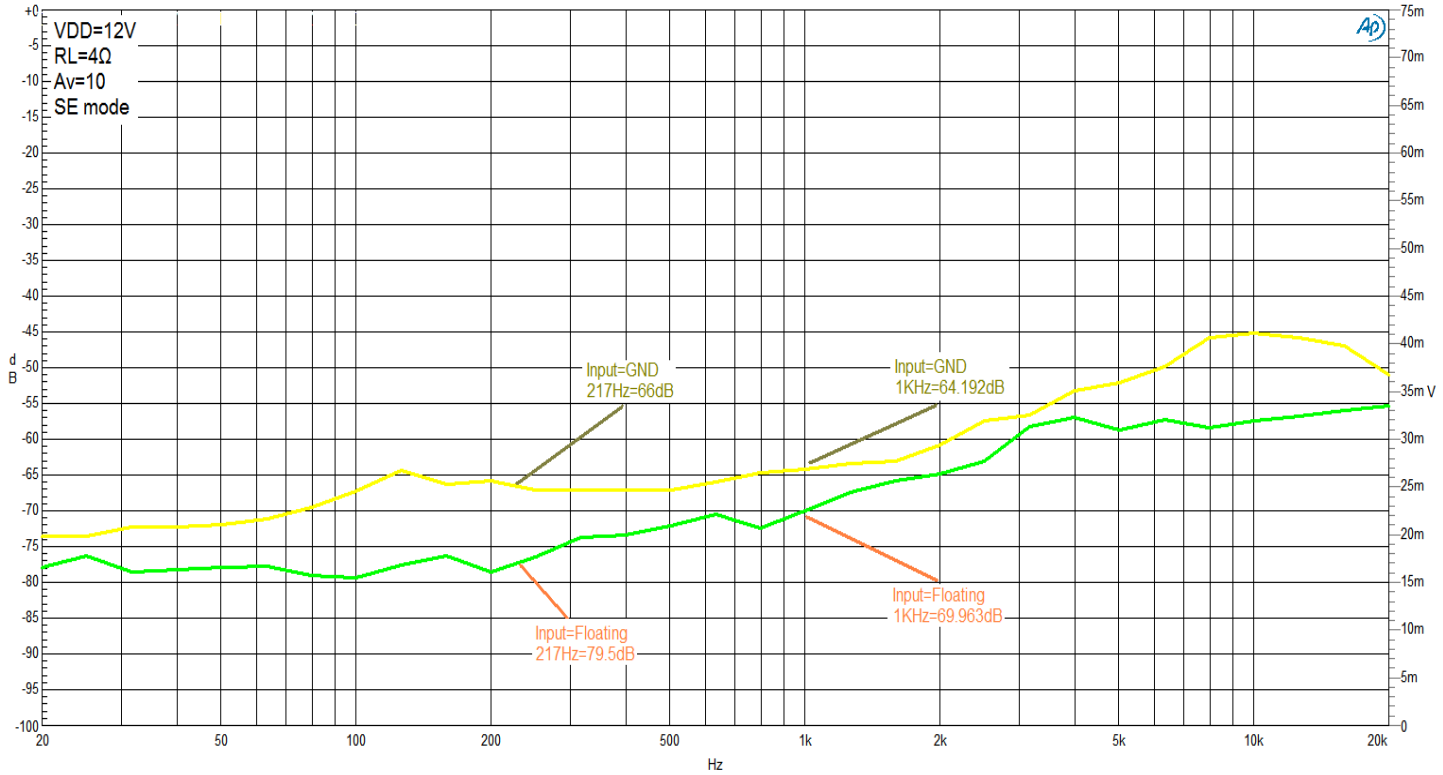


Figure 11
Supply ripple rejection (Ksvr, **RL=8Ω**, SE mode)

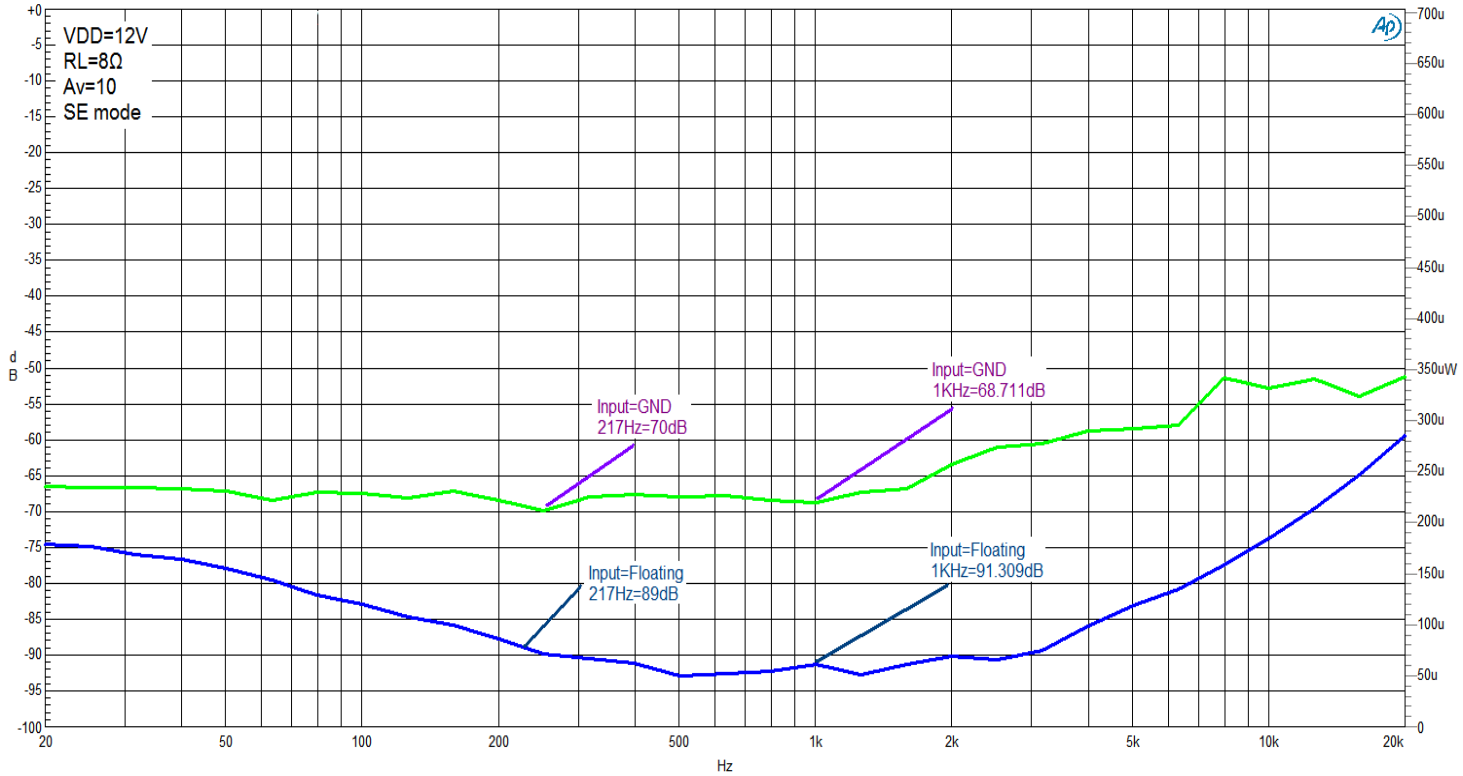


Figure 12
SNR vs. Noise Level (BTL mode)

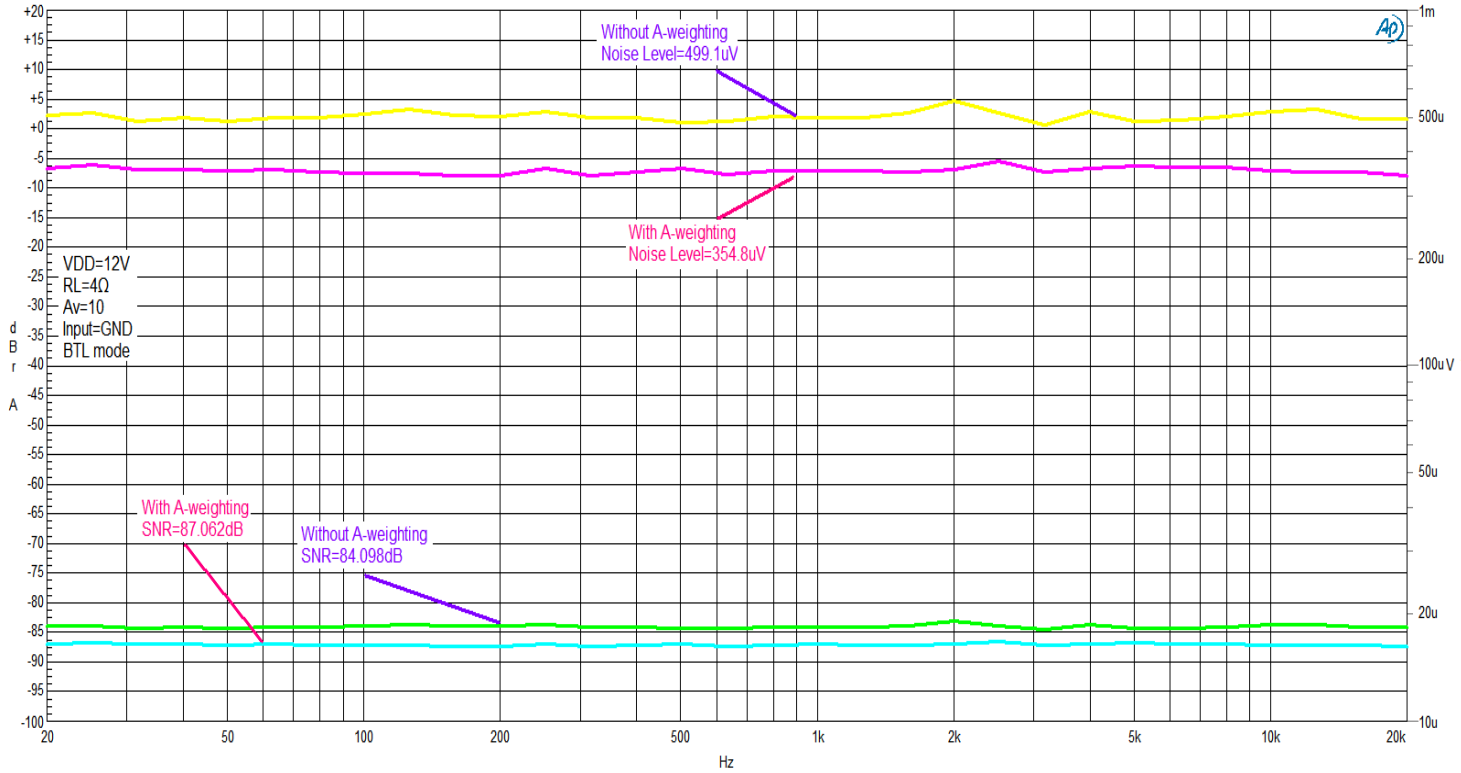


Figure 13
SNR vs. Noise Level (SE mode)

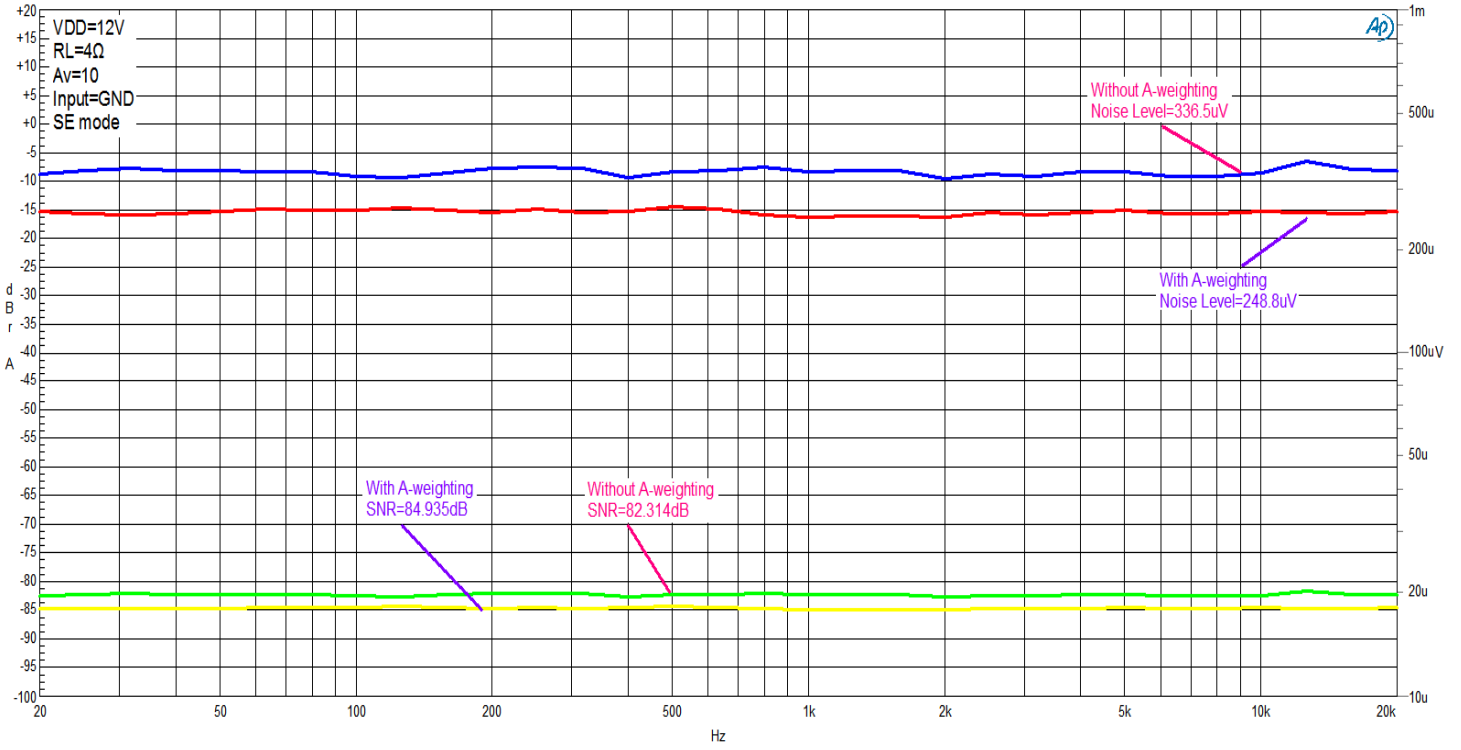


Figure 14
Crosstalk vs. Frequency (BTL mode)

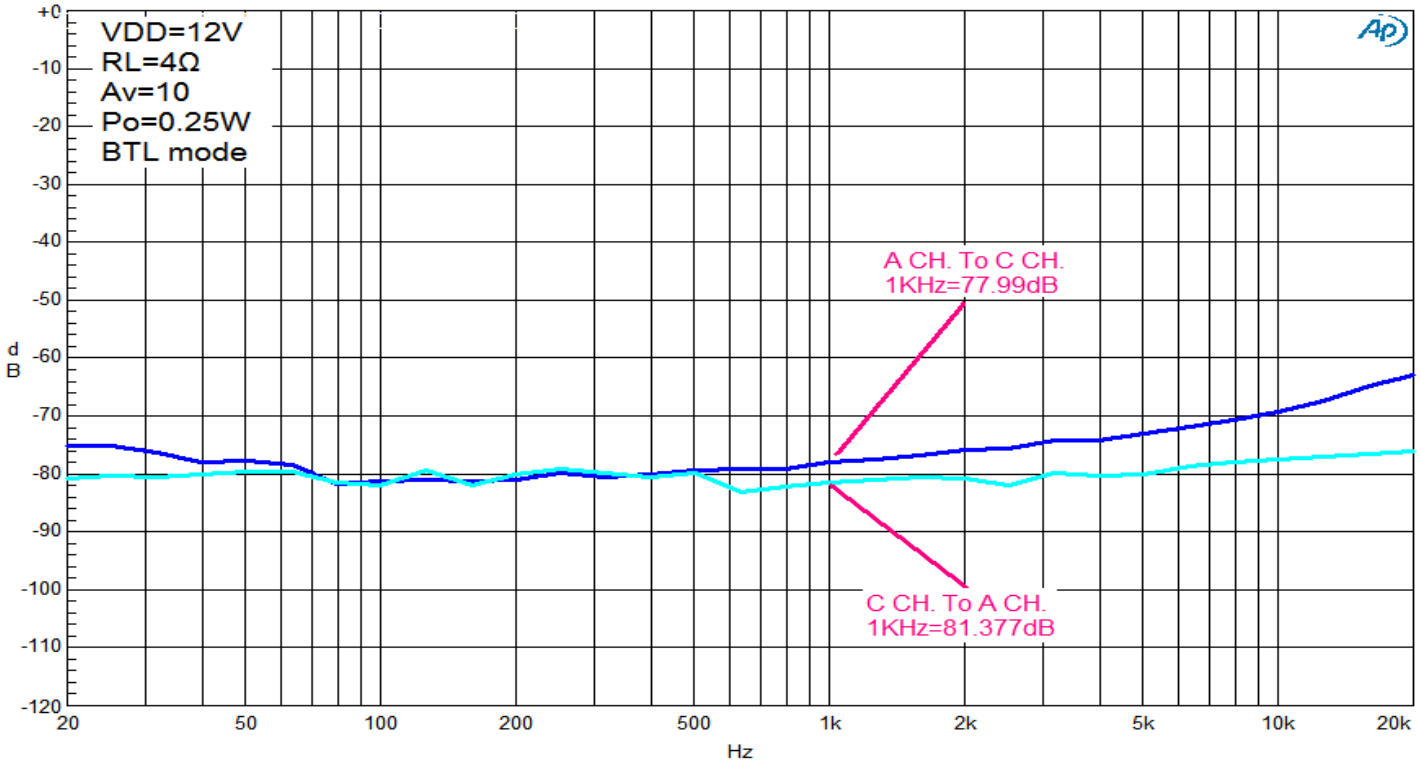
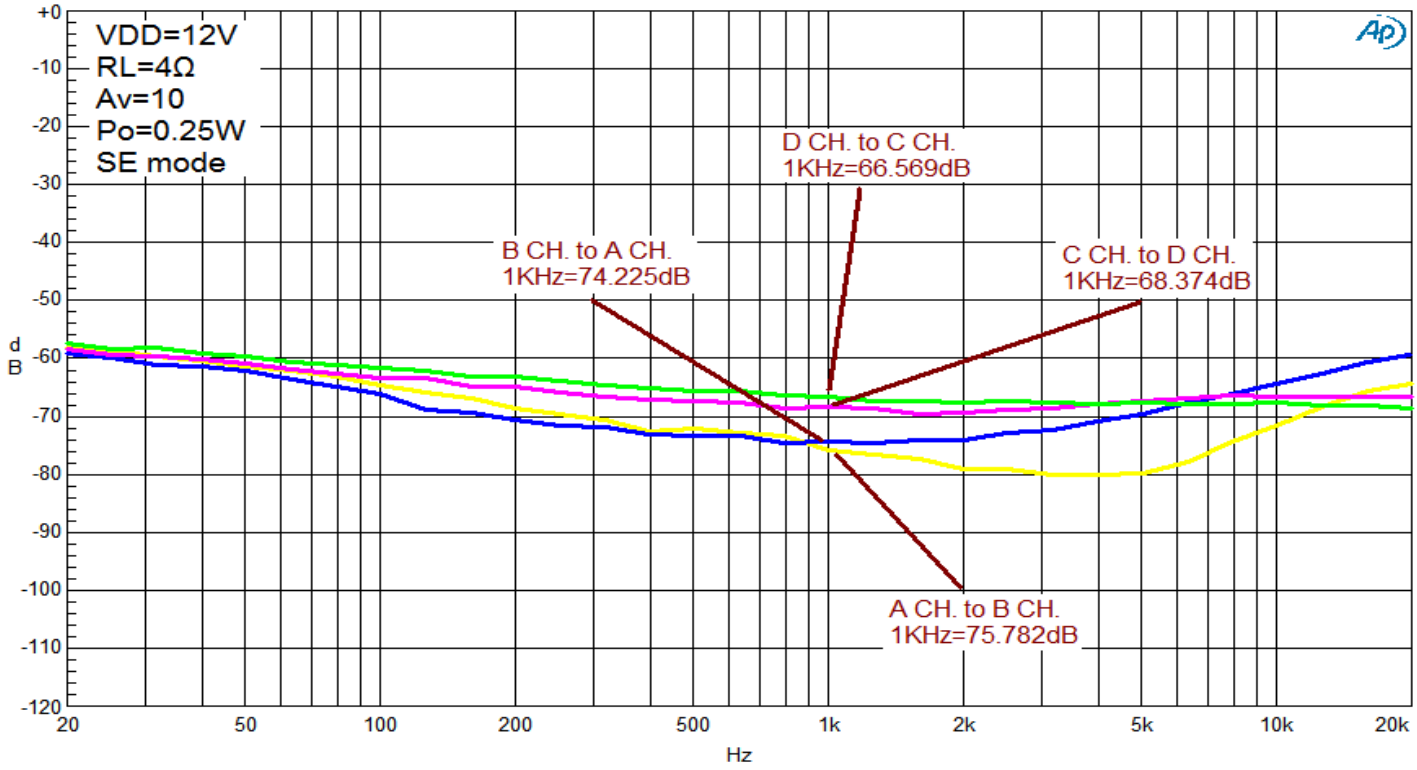
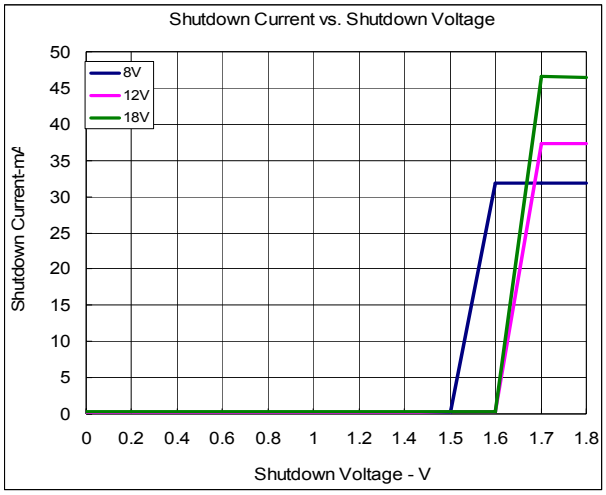


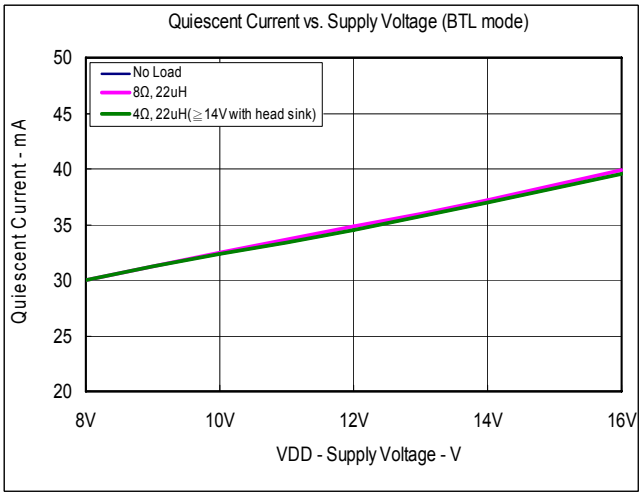
Figure 15
Crosstalk vs. Frequency (SE mode)



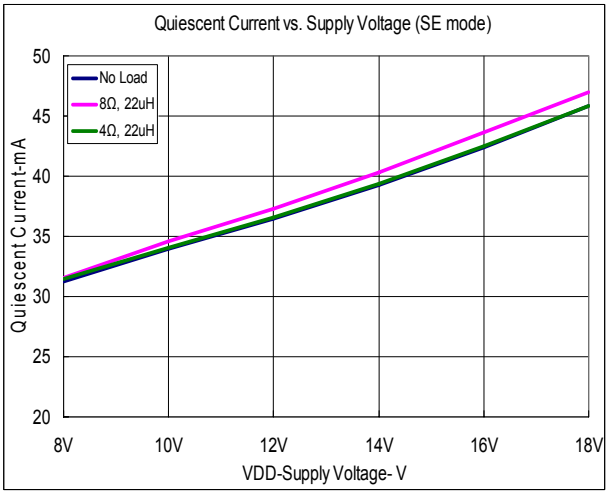
SD Current vs. SD Voltage



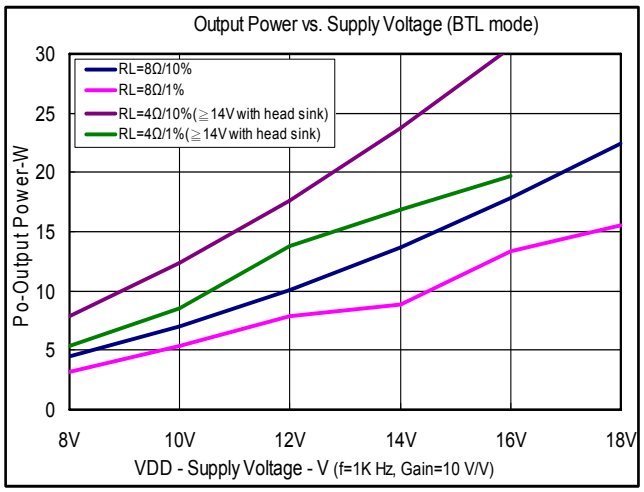
Quiescent Current vs. Supply voltage (BTL mode)



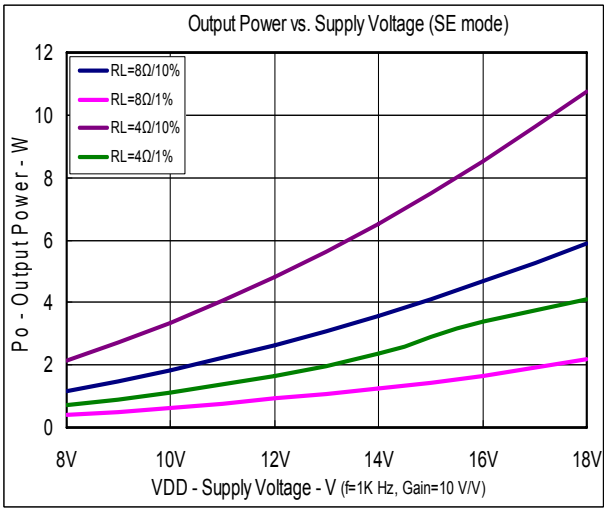
Quiescent Current vs. Supply voltage (SE mode))



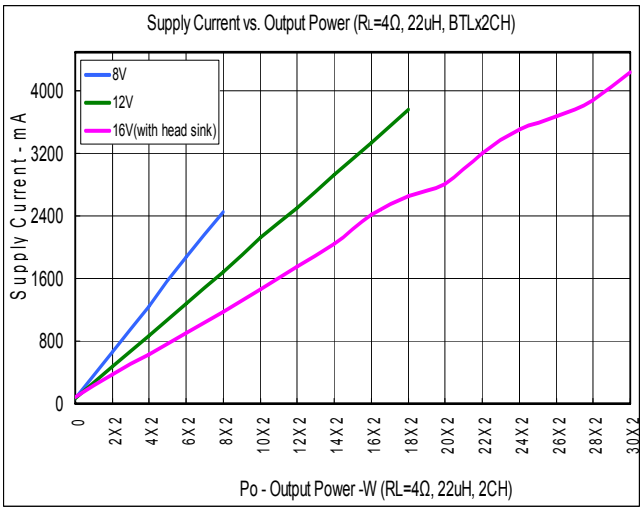
Output Power vs. Supply Voltage(BTL mode)



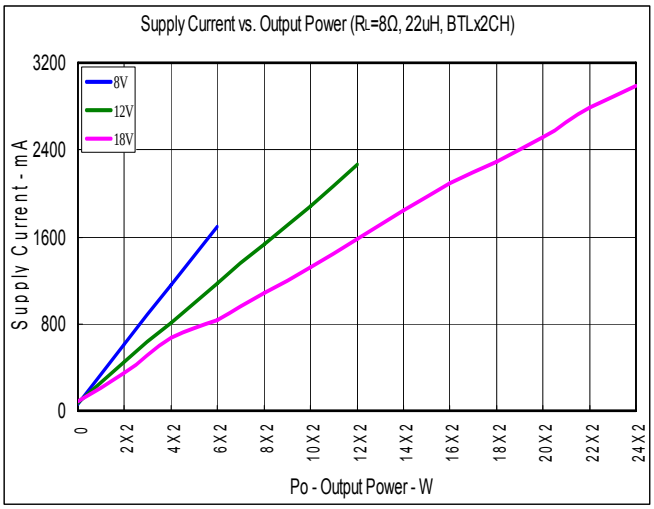
Output Power vs. Supply Voltage(SE mode)



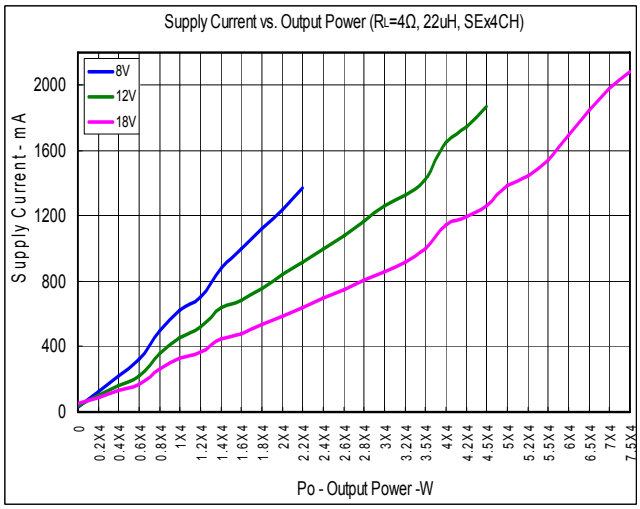
Supply Current vs. Output Power (RL=4Ω,BTL mode)



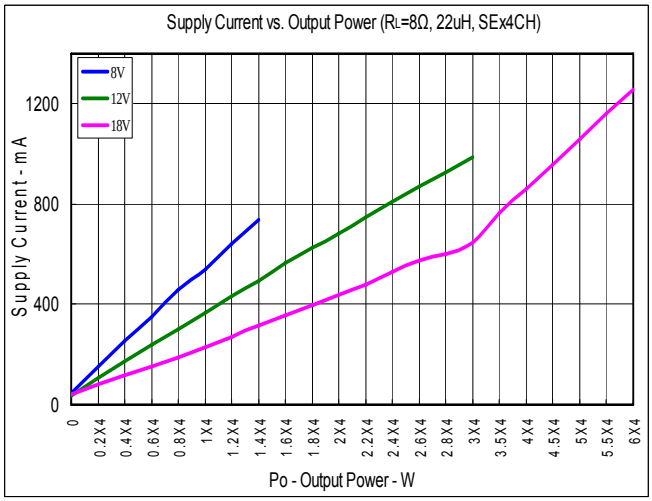
Supply Current vs. Output Power (RL=8Ω,BTL mode)



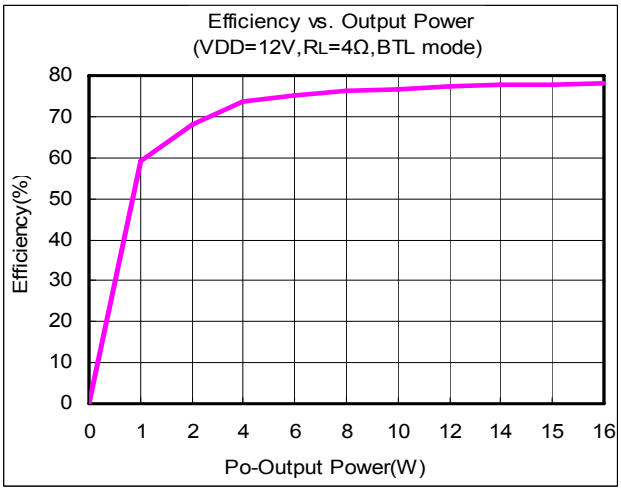
Supply Current vs. Output Power (RL=4Ω,SE mode)



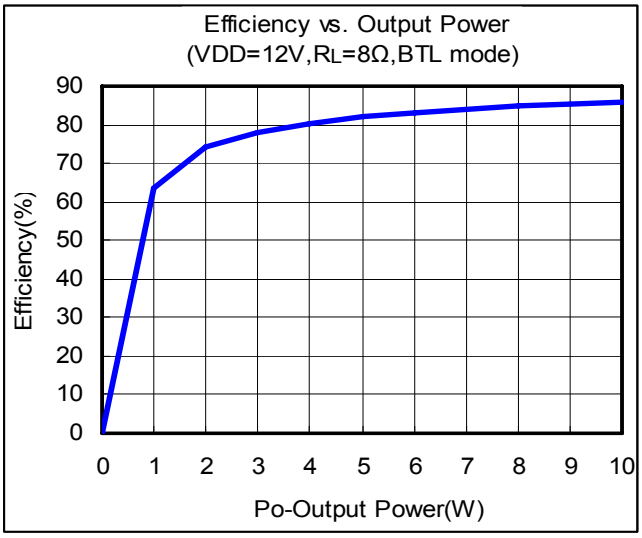
Supply Current vs. Output Power (RL=8Ω,SE mode)



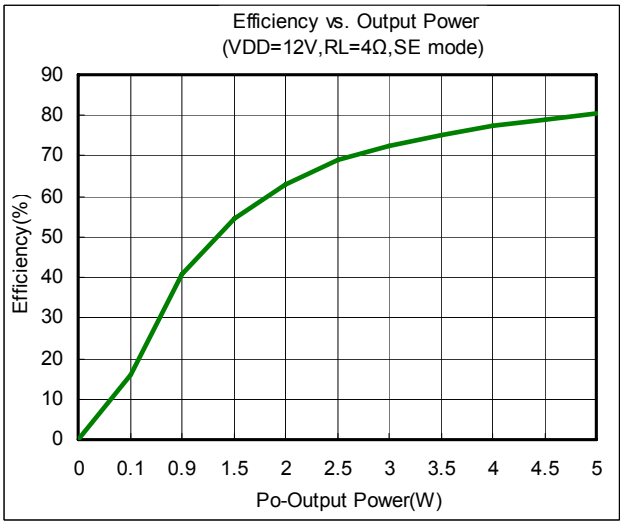
Efficiency (VDD=12V,RL=4Ω,BTL mode)



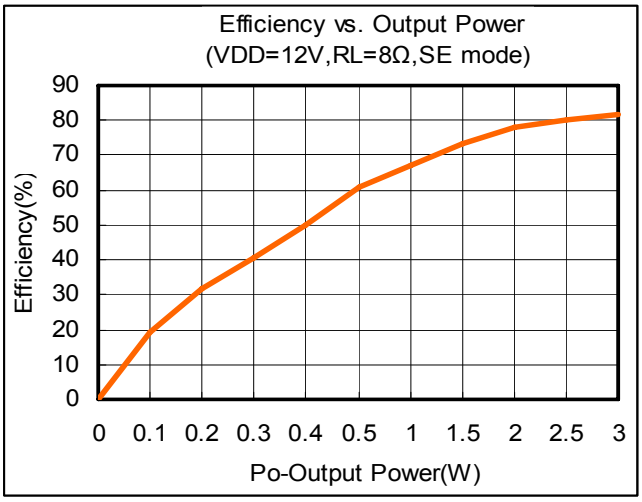
Efficiency (VDD=12V,RL=8Ω,BTL mode)



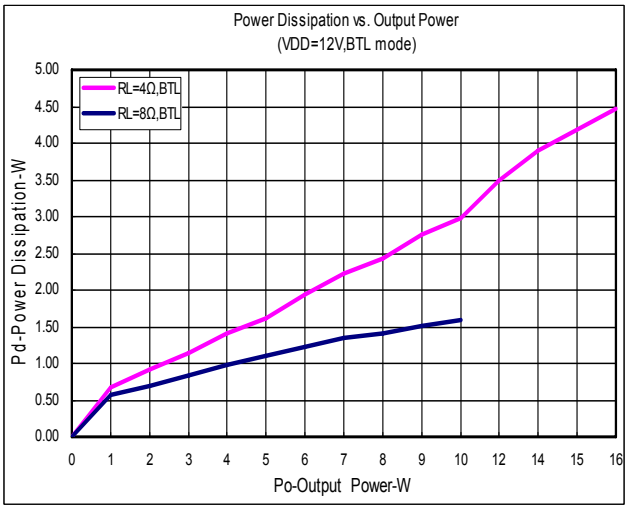
Efficiency (VDD=12V,RL=4Ω,SE mode)



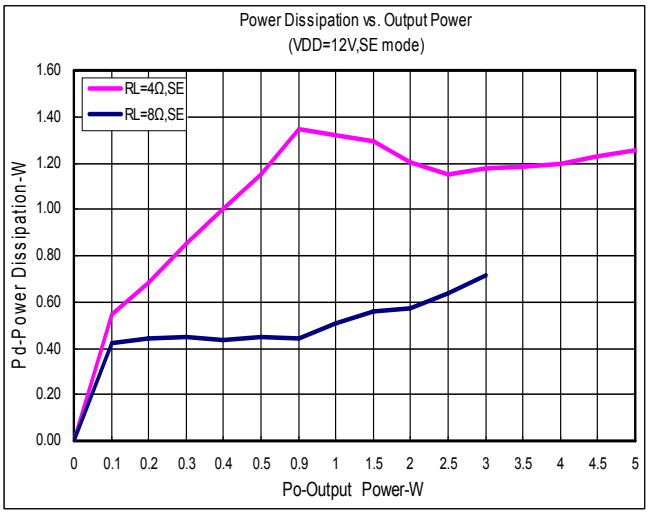
Efficiency (VDD=12V,RL=8Ω,SE mode)



Power Dissipation vs. Output Power
(VDD=12V,BTL mode)



Power Dissipation vs. Output Power
(VDD=12V,SE mode)



▪ APPLICATION INFORMATION

Input Resistors (Ri) and Gain

The LY8321 has two internal amplifier stages. The pre-amplifier gain is externally configurable, while the total gain is internally fixed. The closed-loop gain of the pre-amplifier gain is set by selecting the Rf to Ri while the total gain is fixed at 4x. So the input resistors (R_i) set the gain of the amplifier according to the equation.

Pre-Amplifier Gain = Rf / Ri

Output=SE Mode:

Total Gain = (Rf / Ri) x 4

A_{VD} = 20 x log [4 x (Rf /Ri)]

For example

Table 1. Typical Total Gain and A_{VD} Values (SE Mode)

Rf (KΩ)	50	100	150	200	250	300
Ri (KΩ)	50	50	50	50	50	50
Total Gain	4	8	12	24	20	24
A_{VD} (db)	12.04	18.06	21.58	24.08	26.02	27.6

Output=BTL Mode:

Total Gain = (Rf / Ri) x 8

A_{VD} = 20 x log [8 x (Rf /Ri)]

For example

Table 2. Typical Total Gain and A_{VD} Values (BTL Mode)

Rf (KΩ)	50	100	150	200
Ri (KΩ)	50	50	50	50
Total Gain	8	16	24	32
A_{VD} (db)	18.06	24.08	27.6	30.1

Input Capacitors (Ci)

In typical application, C_i and the input resistance of the amplifier (R_i) form a high-pass filter with the corner frequency(f_c) determined in equation.

$f_c = 1 / (2\pi R_i C_i)$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit.

For example

C_i is 0.1 µF, so one would likely choose a value in the range of 0.1 µF to 1.0 µF. R_i is 50 kΩ and the specification calls for a flat bass response down to 30 Hz.

Ci = 1 / (2πRi fc)

Ci = 1 / (2π x 50KΩ x 30Hz)=0.106uF，One would likely choose a value of 0.1uF as this value is commonly used.

Note that it is important to C_i must be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing C_i for a given cutoff frequency, size the bypass capacitor to 10 times that of the input capacitor.

Ci ≦ Cbypass

Bypass Capacitor (Cbypass)

The Bypass Capacitor (C3) is the most critical capacitor and serves important functions.
During start-up or recovery from shutdown mode, Cbypass determines the rate at which the amplifier starts up. The Cbypass will to reduce noise caused by the power supply coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded the PSRR and THD+N values.
The bypass capacitor (C3) with values of 1.0µF to 10.0µF is recommended for the best THD and noise performance. Therefore, increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop, Cbypass should be 10 times larger than C_i.

Cbypass ≧ Ci

Power Supply Decoupling Capacitor (Cs)

The LY8321 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1uF~1.0uF, placed as close as possible to the device PVCC lead works best. Placing this decoupling capacitor close to the LY8321 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 470uF or greater capacitor placed near the audio power amplifier would also help, so 470uF or larger capacitor should be placed on each PVCC terminal.

Single-Ended Output Capacitor, (Co)

In single-ended (SE) applications, the dc blocking capacitor forms a high-pass filter with the speaker impedance. The frequency response rolls off with decreasing frequency at a rate of 20 dB/decade. The cutoff frequency is determined by
fc = 1 / (2πRLCo)

Table 3. Filter Responses Reference Values

Speaker Load (Ω)	SE mode - Co Capacitor select(uF)		
	fc = 60 Hz	fc = 40 Hz	fc = 20 Hz
4	680	1000	2200
6	470	680	1500
8	330	470	1000

Output Filter and Frequency Response

The output filter components consist of the series inductor and capacitor to ground at the LOUT and ROUT pins. There are several possible configurations, depending on the speaker impedance and whether the output configuration is single-ended (SE) or bridge-tied load (BTL). Table 4 lists the recommended values for the filter components. It is important to use a high-quality capacitor in this application.

Table 4. Recommended Filter Output Components Reference Values

Output Type	Speaker Load (Ω)	Filter Inductor (uH)	Filter Capacitor (uF)
Bridge Tied Load (BTL)	8	22	0.68
Single Ended (SE)	8	33	0.47
	4	22	0.68

BST Capacitors

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 1.0 ceramic capacitor, rated for at least 25V up, must be connected from each output to its corresponding bootstrap input. Specifically, all 1.0 capacitor must be connected from OUT to BST pin.
The bootstrap capacitors connected between the BST pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitor

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, one internal regulator clamps the gate voltage. A 1.0uF capacitor must be connected from VCLAMP pin to ground and must be rated for 25V up. The voltages at the VCLAMP terminal may vary with PVCC and may not be used for powering any other circuitry.

Shutdown Function

When the LY8321 not in use. The device will be to turn off the amplifier to reduce power consumption. When logic low is applied to the shutdown pin, this shutdown feature will turns the amplifier off. By switching the shutdown pin connected to GND, the device supply current draw will be minimized in idle mode. The pin cannot be left floating due to the internal did not pull-up.

Mute Function

The Mute pin is an input pin to control the LY8321 output state. A logic high is disable the LY8321 outputs. A logic low on this pin enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a TV or transitioning between different audio sources.
The Mute pin should never be left floating. For power conservation, the SD pin should be used to reduce the quiescent current to the absolute minimum level.

Over-Heat Protection

The LY8321 has a built-in over-heat protection circuit, it will turn off all power output when the chip temperature over 180℃, the chip will return to normal operation automatically after the temperature cool down to 160℃.

Short Circuit Protection

The LY8321 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts. When a short-circuit is detected on the outputs, the part immediately goes into shutdown. This is a latched fault and must be reset by cycling the voltage on the shutdown pin to a logic low and back to the logic high, or by cycling the power off and then back on. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry activates again.

PCB Layout

Because the LY8321 is a class-D amplifier that switches at a high frequency, the layout of the PCB should be optimized according to the following guidelines for the best possible performance.

1. Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability.
2. Decoupling capacitors—The high-frequency 0.1uF decoupling capacitors should be placed as close to the PVCC pins and AVCC pin terminals as possible.
   And the Bypass pin capacitor and VCLAMP pin capacitor should also be placed as close to the device as possible.
   Large (1000uF or greater) bulk power-supply decoupling capacitors should be placed near the device on the PVCC terminals.
3. Grounding—The AVCC pin decoupling capacitor and Bypass pin capacitor should each be grounded to analog ground (AGND).
   The PVCC decoupling capacitors and VCLAMP capacitors should each be grounded to power ground (PGND). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the LY8321.
4. Output filter—The reconstruction filter should be placed as close to the output terminals as possible for the best EMI performance. The capacitors should be grounded to power ground.
5. The input resistors need to be very close to the device input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the device.
6. Making the high current traces going to PVCC, GND, V_{O+} and V_{O-} pins of the device should be as wide as possible to minimize trace resistance. If these traces are too thin, the device's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

▪ DEMO BOARD INFORMATION-1 (Satellite Type - 4xSE or 2xBTL Mode)

Demo Board Application Circuit (4xSE Mode)

MODE_2	MODE_1	MODE_0	OUTPUT STATUS
1	0	0	BTL X 2CH
1	1	0	BTL X 1+SE X 2CH
1	0	1	SE X 4CH

LC Filter

O / P	SPK(Ohm)	L(uH)	C(uF)
SE	4	22	0.68
	8	33	0.47
BTL	8	22	0.68

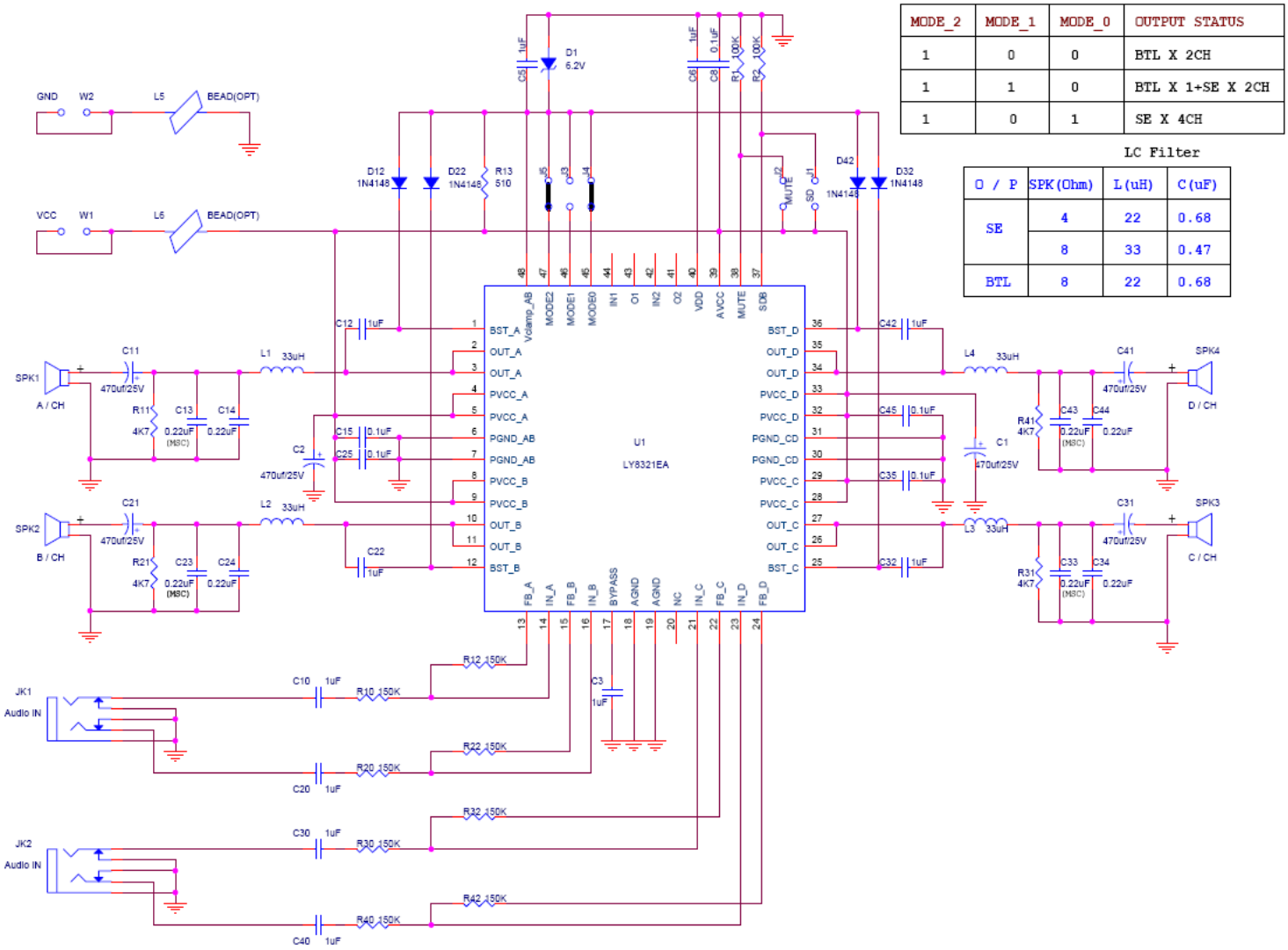


Figure 16 LY8321 Demo Board Application Circuit (4xSE Mode)

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

Demo Board Application Circuit (2xBTL Mode)

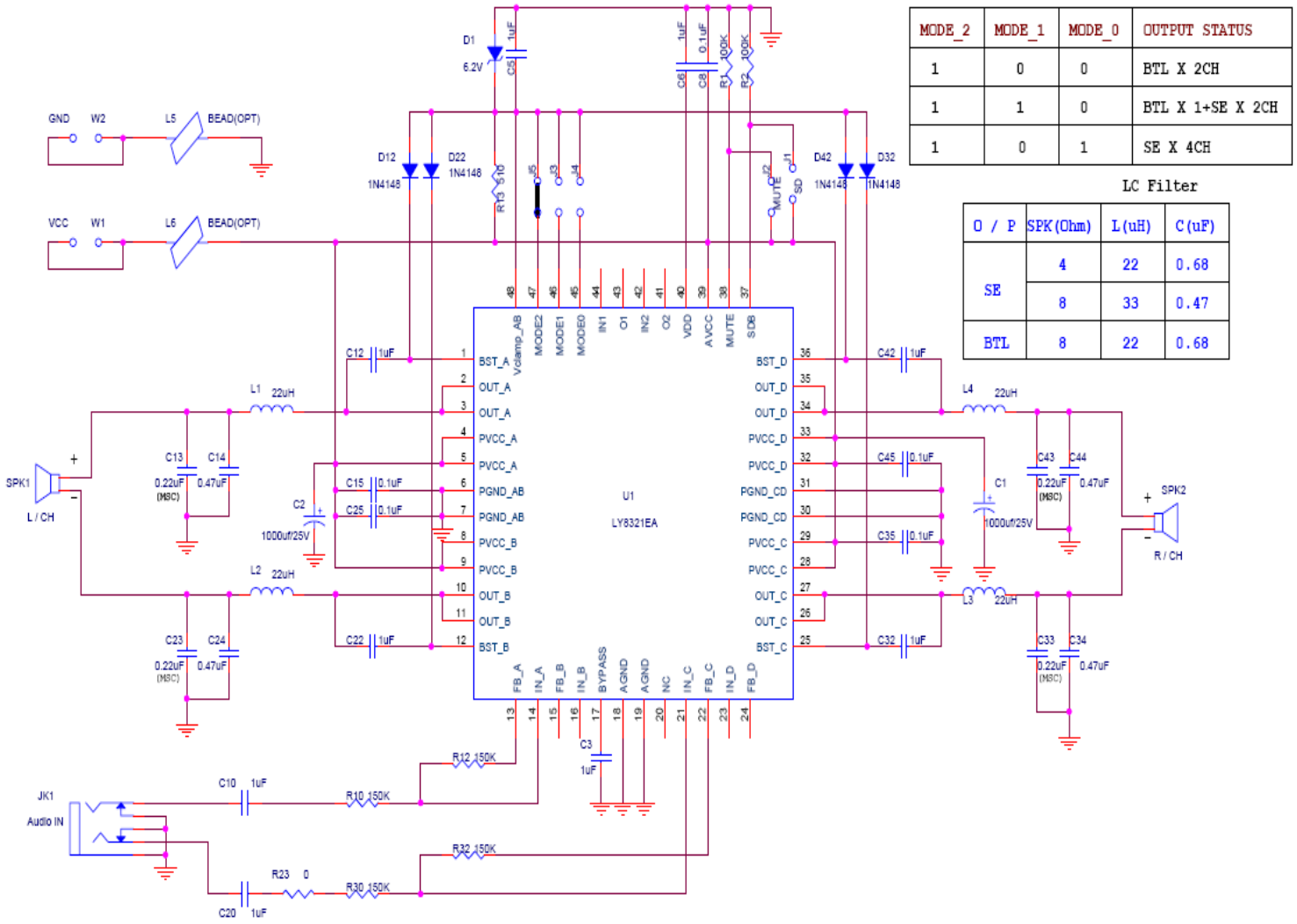


Figure 17 LY8321 Demo Board Application Circuit (2xBTL Mode)

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

Demo Board BOM List (4xSE and 2xBTL Mode)

LY8321 V1.0 BOM List (4xSE Mode)

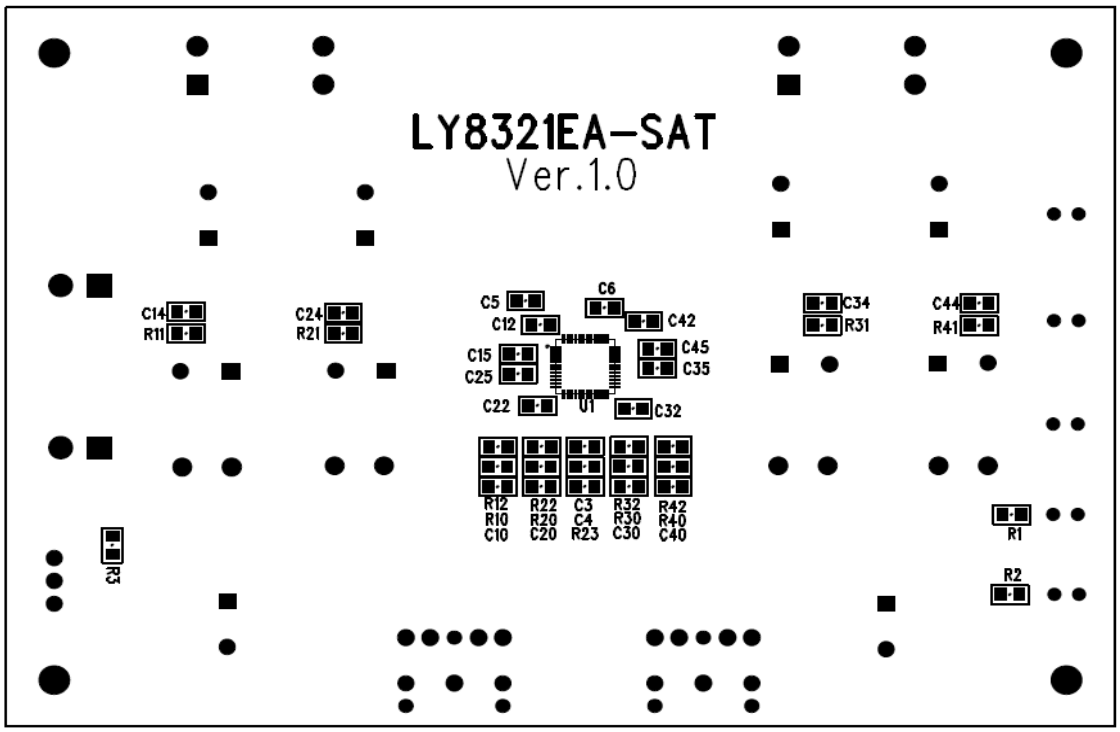
No.	Description	Reference	Amount	Note	Remark
1	Capacitor,470uF	C1,C2,C11,C21,C31,C41	6	DIP, 35V,105℃, 10*20, EC Cap.	
2	Capacitor, 0.1uF	C8, C15,C25,C35,C45	5	SMD0805,80%/-20%,NP	
3	Capacitor, 1uF	C3,C5,C6, C10, C20,C30, C40, C12, C22, C32, C42	11	SMD0805 ,80%/-20%,NP	
4	Capacitor, 0.22uF	C14,C24,C34,C44	4	SMD0805,80%/-20%,NP	
5	Capacitor, 0.22uF	C13,C23,C33,C43	4	DIP, MSC,100Vdc, ±10%	
6	Resistor, 150KΩ	R12,R22,R32,R42	4	SMD0805,1/8W, 1%	
7	Resistor, 100KΩ	R1,R2	2	SMD0805,1/8W, 1%	
8	Resistor, 51KΩ	R10,R20,R30,R40	4	SMD0805,1/8W, 1%	
9	Resistor, 4.7KΩ	R11,R21,R31,R41	4	SMD0805,1/8W, 1%	
10	Resistor, 510Ω	R13	1	SMD0805,1/8W, 1%	
11	Diode 1N4148	D12, D22, D32, D42	4	DIP, NXP 100V,200mA	
12	Zener Diode 6.2V	D1	1	DIP, HITACHI (HZ6C2TA-E)	
13	Fixed Inductors 33uH	L1,L2,L3,L4	4	DIP TOKO (A7502BY-330M)	
14	IC	U1	1	LY8321,(LQFP48)	
15	1*2 Pin Header	W1,W2	2	Pitch 3.96mm	
16	1*2 Pin Header	J1,J2,J3,J4,J5	5	Pitch 2.54mm	
17	Phone Jack	JK1, JK2	2	ψ3.5, 5P, 90°	
18	Speaker Jack	SPK A/B,SPK C/D	2	2*2p(R.B.)	

LY8321 V1.0 BOM List (2xBTL Mode)

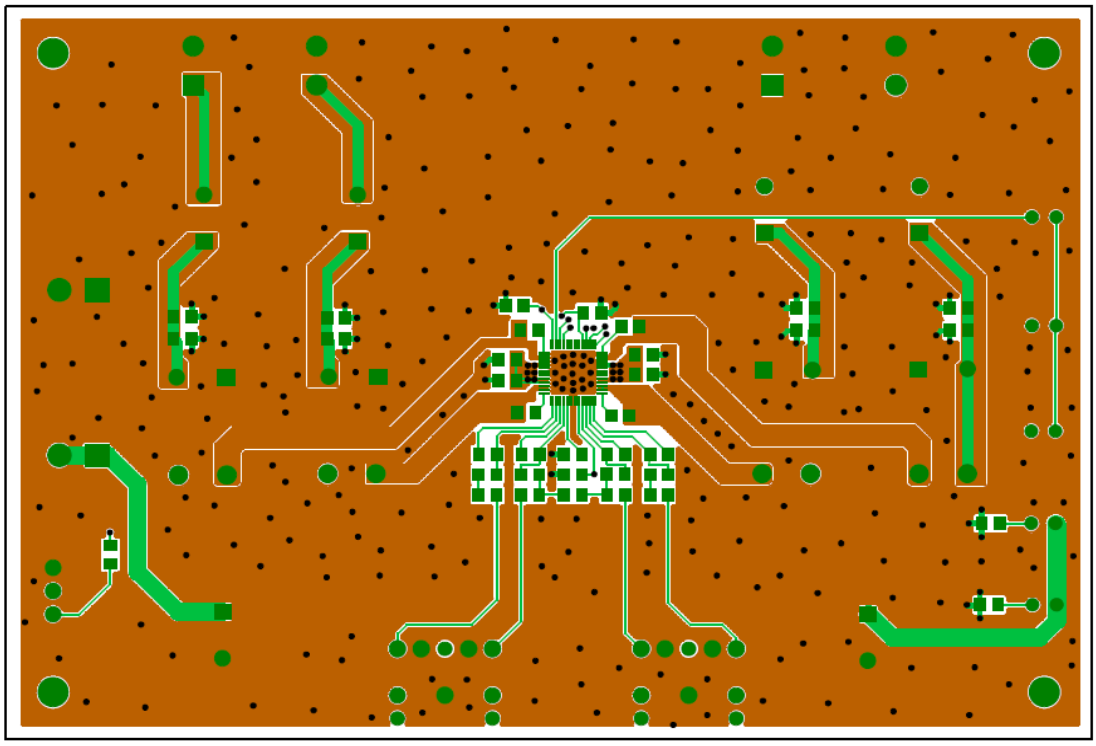
No.	Description	Reference	Amount	Note	Remark
1	Capacitor,1000uF	C1,C2	2	DIP, 35V,105℃, 10*20, EC Cap..	
2	Capacitor, 1uF	C3, C5, C6, C10, C20, C12,C22,C32,C42	9	SMD0805 ,80%/-20%,NP	
3	Capacitor,0.47uF	C14, C24, C34, C44	4	SMD0805 ,80%/-20%,NP	
4	Capacitor, 0.1uF	C8,C15,C25,C35,C45	5	SMD0805,80%/-20%,NP	
5	Capacitor, 0.22uF	C13,C23,C33,C43	4	DIP, MSC,100Vdc, ±10%	
6	Resistor, 150KΩ	R12,R32	2	SMD0805,1/8W, 1%	
7	Resistor, 100KΩ	R1,R2	2	SMD0805,1/8W, 1%	
8	Resistor, 51KΩ	R10,R30	2	SMD0805,1/8W, 1%	
9	Resistor, 510Ω	R13	1	SMD0805,1/8W, 1%	
10	Resistor, 0Ω	R23	1	SMD0805,1/8W, 1%	
11	Diode 1N4148	D12, D22, D32, D42	4	DIP, NXP 100V,200mA	
12	Zener Diode 6.2V	D1	1	DIP, HITACHI (HZ6C2TA-E)	
13	Fixed Inductors 22uH	L1,L2,L3,L4	4	DIP, TOKO (A7502BY-330M)	
14	IC	U1	1	LY8321,(LQFP48)	
15	1*2 Pin Header	W1,W2	2	Pitch 3.96mm	
16	1*2 Pin Header	J1,J2,J3,J4,J5	5	Pitch 2.54mm	
17	Phone Jack	JK1, JK2	2	ψ3.5, 5P, 90°	
18	Speaker Jack	SPK A/B, SPK C/D	2	2*2p(R.B.)	

Demo Board Artwork (4xSE or 2xBTL Mode)

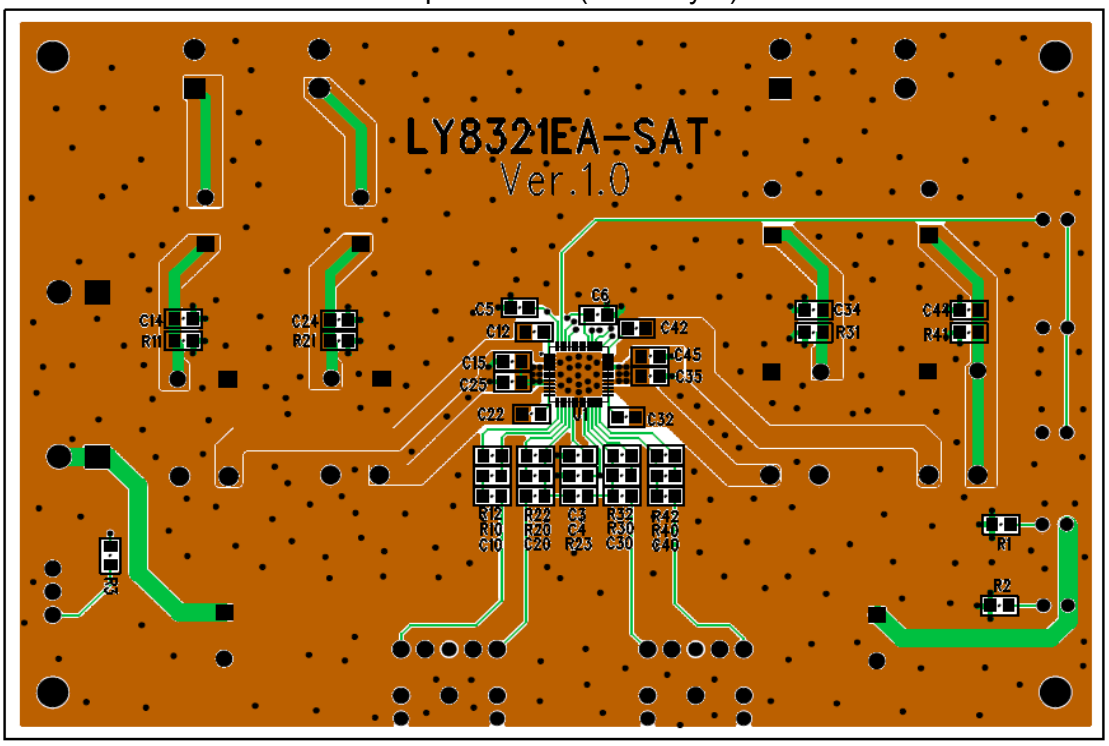
Top Silkscreen



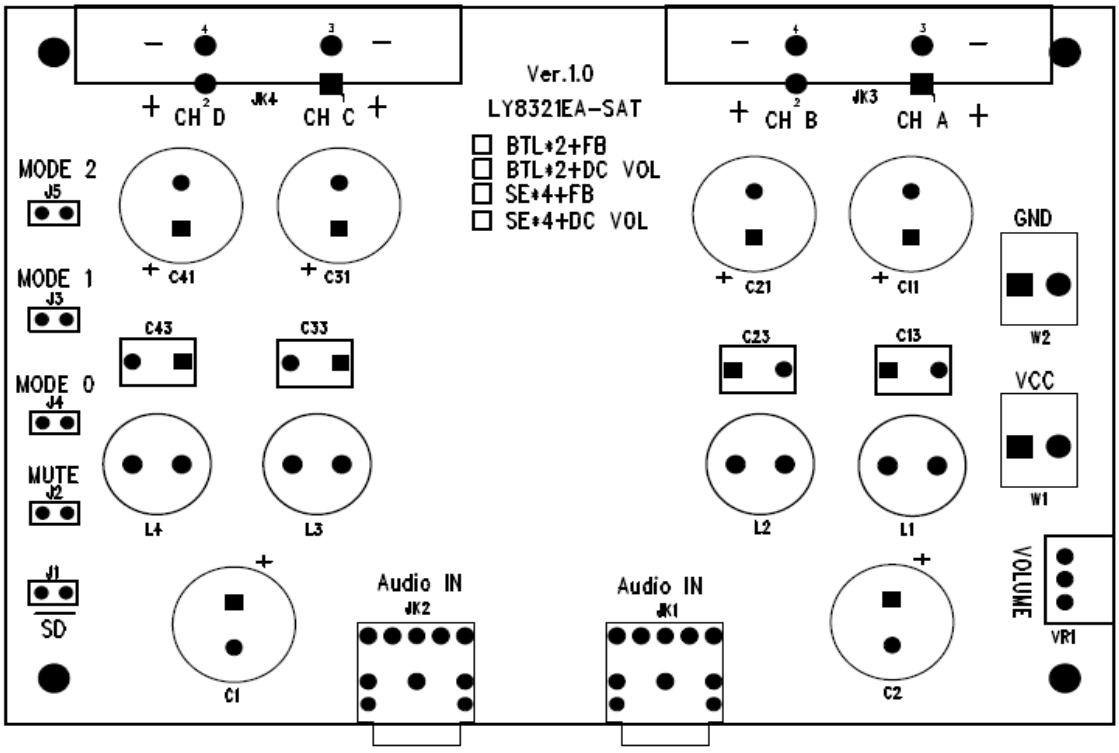
Top Layer



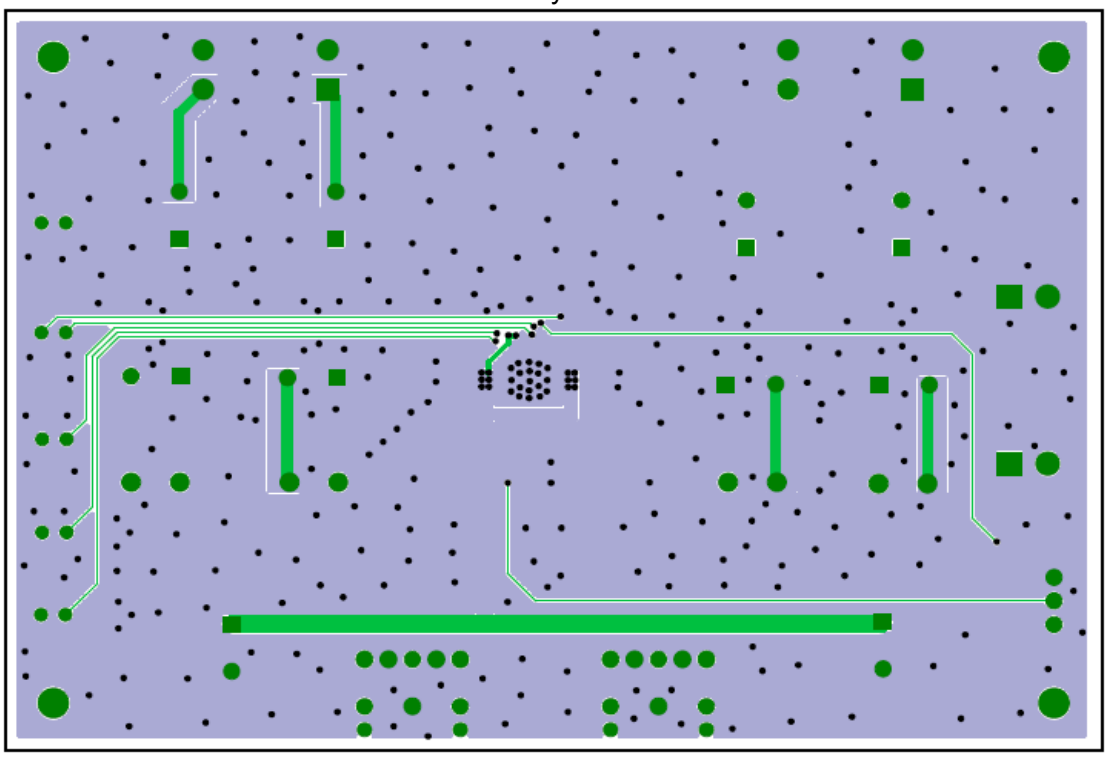
Composite view (TOP Layer)



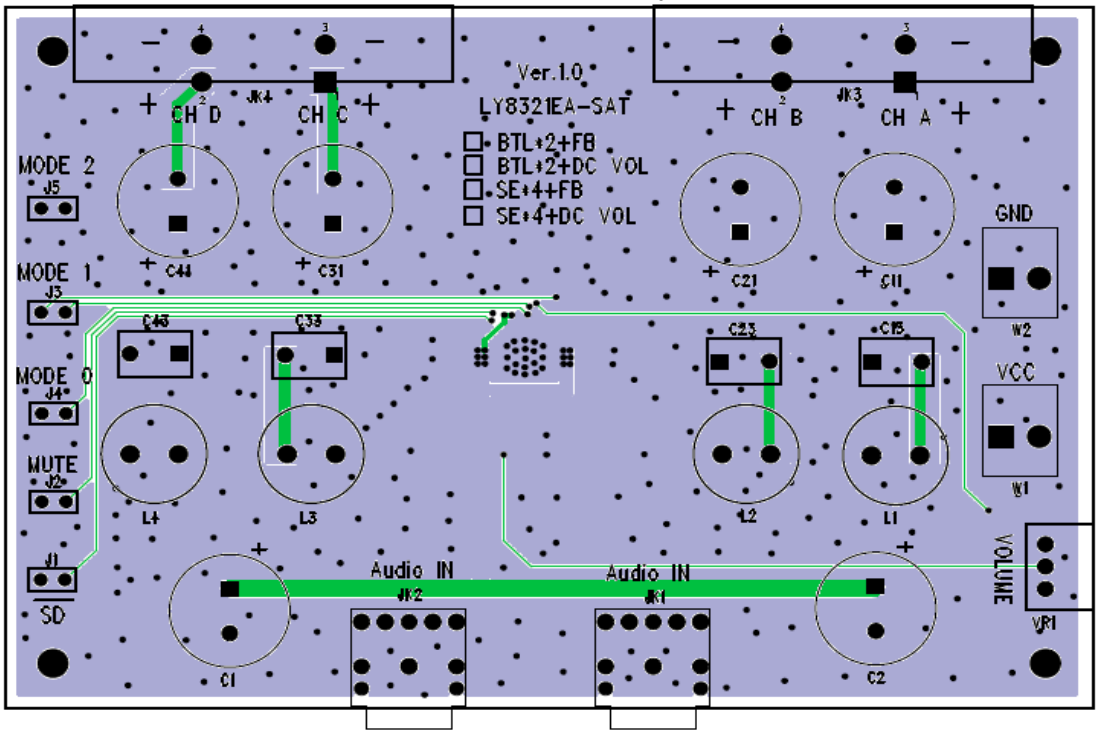
Bottom Silkscreen



Bottom Layer



Composite view (Bottom Layer)



▪ DEMO BOARD INFORMATION-2 (2xSE+1xBTL(Subwoofer) Mode)

Demo Board Application Circuit (2xSE+1xBTL Mode)

MODE_2	MODE_1	MODE_0	OUTPUT STATUS
1	0	0	BTL X 2CH
1	1	0	BTL X 1 +SE X 2 CH
1	0	1	SE X 4CH

LC Filter

O / P	SPK(Ohm)	L(uH)	C(uF)
SE	4	22	0.68
	8	33	0.47
BTL	8	22	0.68

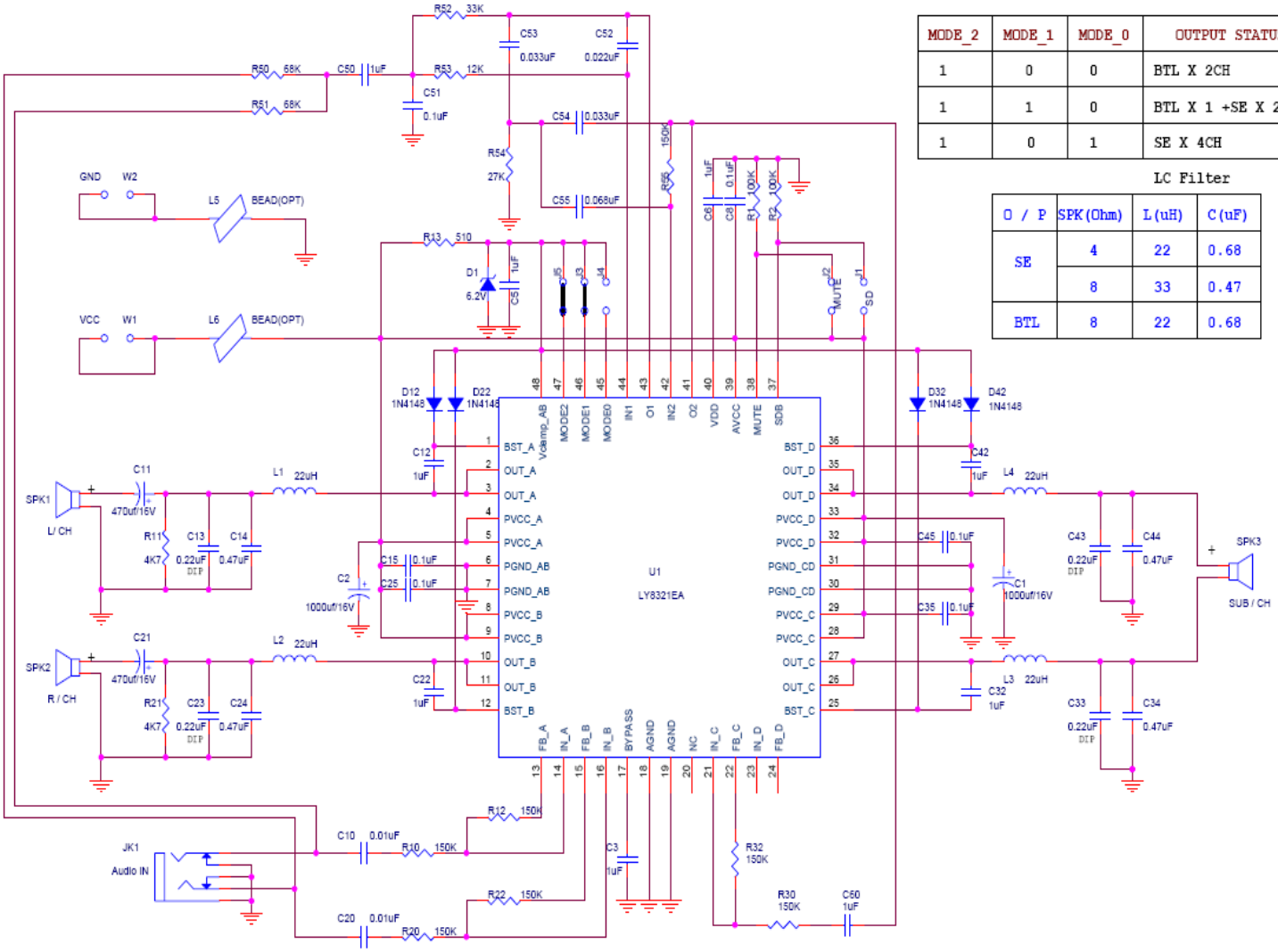


Figure 18 LY8321 Demo Board Application Circuit (2xSE+1xBTL Mode)

(*3) When driving ≧14V power supply, the device must be mounted to the PCB board and increase a large area of copper or recommended to use external heat sink.

Demo Board BOM List (2xSE+1xBTL Mode)

LY8321 V1.0 BOM List (2xSE+1xBTL Mode)

No.	Description	Reference	Amount	Note	Remark
1	Capacitor,1000uF	C1,C2	2	DIP 35V,105℃, 10*20, EC Cap.	
2	Capacitor,470uF	C11,C21	2	DIP 35V,105℃, 10*20, EC Cap.	
3	Capacitor, 1uF	C3, C5, C6, C50, C60 C12,C22,C32,C42	9	SMD0805,80%/-20%,NP	
4	Capacitor,0.47uF	C14,C24, C34, C44	4	SMD0805,80%/-20%,NP	
5	Capacitor, 0.1uF	C8, C51, C15, C25, C35,C45	6	SMD0805 ,80%/-20%,NP	
6	Capacitor, 0.01uF	C10, C20	1	SMD0805,80%/-20%,NP	
7	Capacitor, 0.068uF	C55	2	SMD0805,80%/-20%,NP	
8	Capacitor, 0.033uF	C53, C54	2	SMD0805,80%/-20%,NP	
9	Capacitor, 0.022uF	C52	1	SMD0805,80%/-20%,NP	
10	Capacitor, 0.22uF	C13,C23,C33,C43	4	DIP, MSC,100Vdc, ±10%	
11	Resistor, 150KΩ	R12,R22, R32, R55	4	SMD0805,1/8W, 1%	
12	Resistor, 100KΩ	R1,R2	2	SMD0805,1/8W, 1%	
13	Resistor, 68KΩ	R50,R51	2	SMD0805,1/8W, 1%	
14	Resistor, 51KΩ	R10,R20, R30	3	SMD0805,1/8W, 1%	
15	Resistor, 33KΩ	R52	1	SMD0805,1/8W, 1%	
16	Resistor, 27KΩ	R54	1	SMD0805,1/8W, 1%	
17	Resistor, 12KΩ	R53	1	SMD0805,1/8W, 1%	
18	Resistor, 4.7KΩ	R11,R21	2	SMD0805,1/8W, 1%	
19	Resistor, 510Ω	R13	1	SMD0805,1/8W, 1%	
20	Diode 1N4148	D12, D22, D32, D42	4	DIP, NXP 100V,200mA	
21	Zener Diode 6.2V	D1	1	DIP HITACHI (HZ6C2TA-E)	
22	Fixed Inductors 22uH	L1,L2,L3,L4	2	DIP, TOKO (A7502BY-220M)	
23	IC	U1	1	LY8321,(LQFP48)	
24	1*2 Pin Header	W1,W2	2	Pitch 3.96mm	
25	1*2 Pin Header	J1,J2,J3,J4,J5	5	Pitch 2.54mm	
26	Phone Jack	JK1, JK2	2	ψ3.5, 5P, 90°	
27	Speaker Jack	SPK A/B / SPK C/D	2	2*2p(R.B.)	

2.1 Channel (2xSE+1xBTL Mode) Hi-Low Pass filter cutoff frequency chart

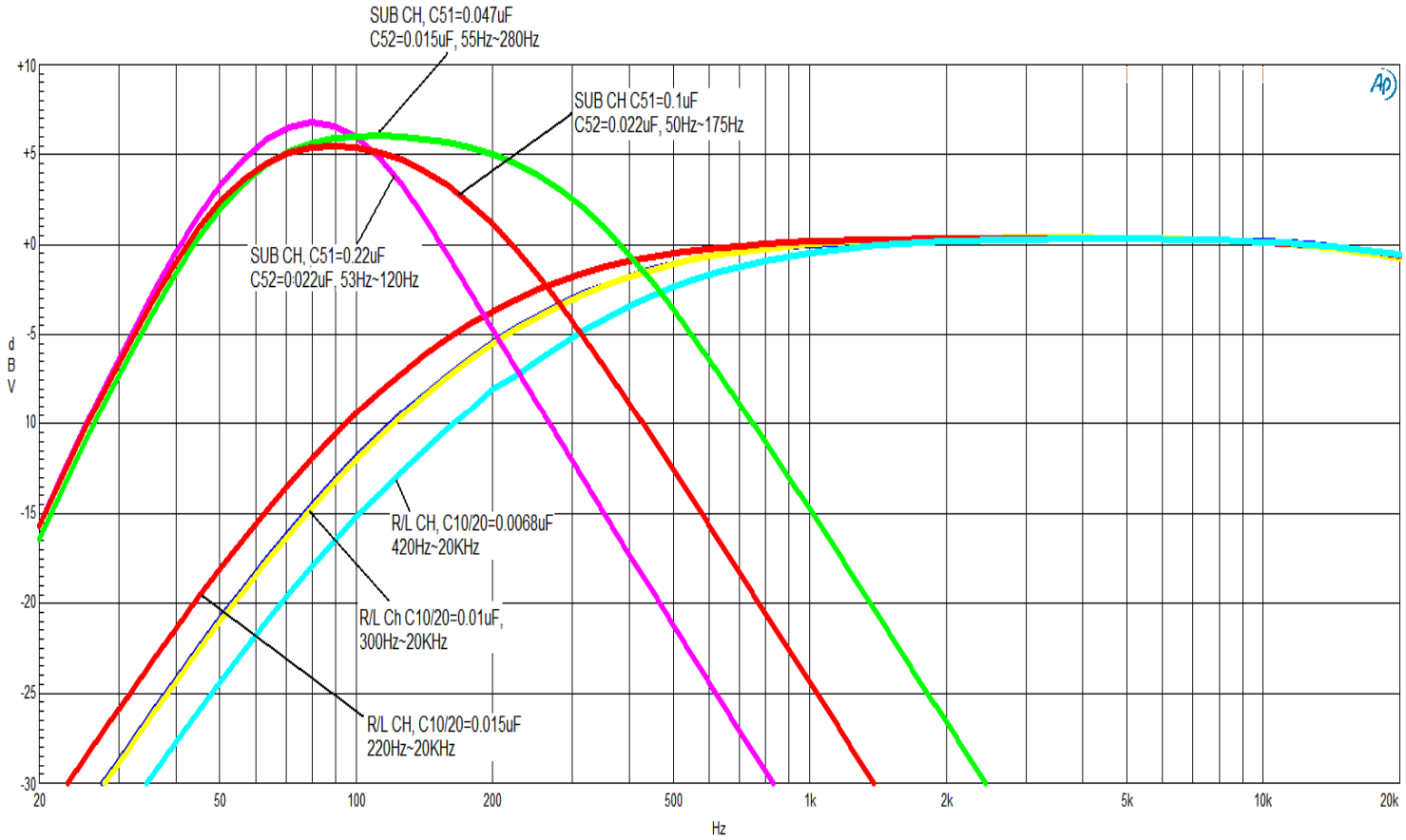
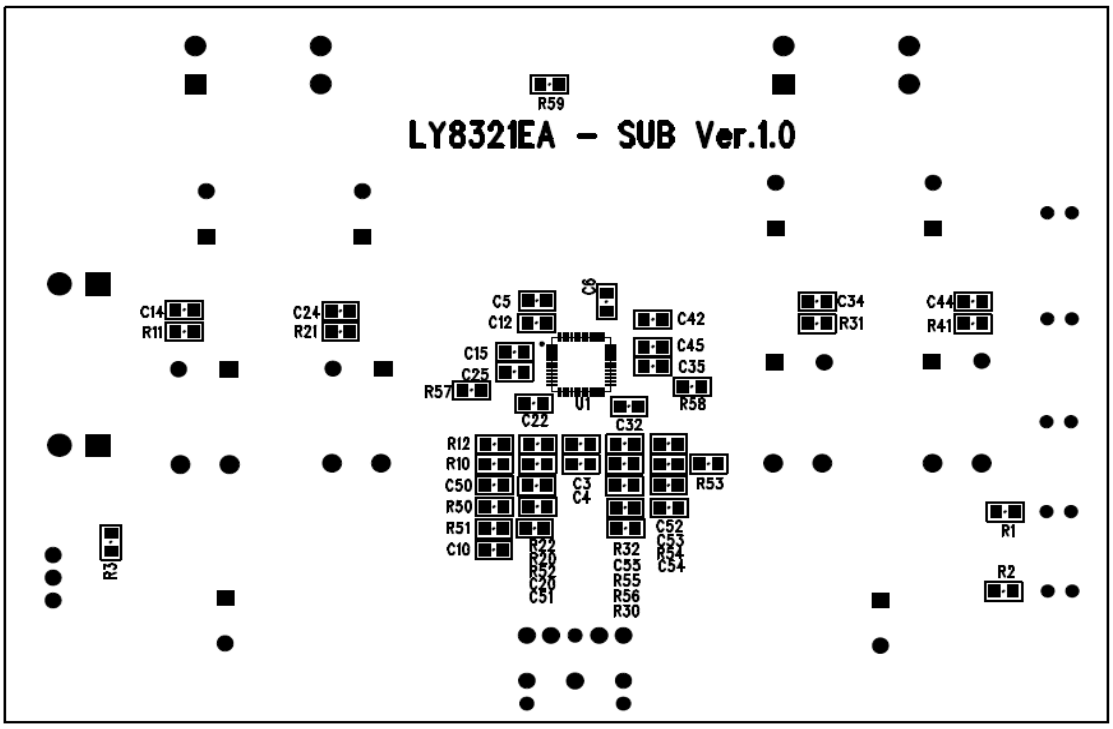


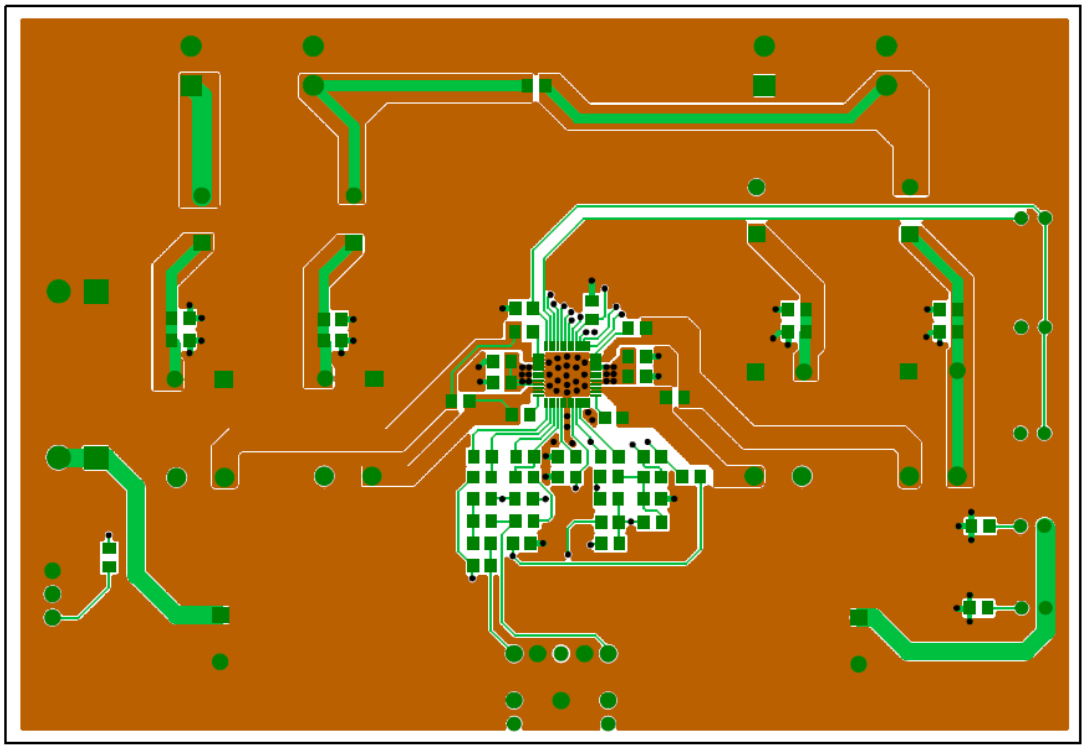
Figure 19 LY8321 2.1CH. (2xSE+1xBTL Mode) Hi-Low Pass filter cutoff frequency chart

Demo Board Artwork (2xSE + 1xBTL Mode)

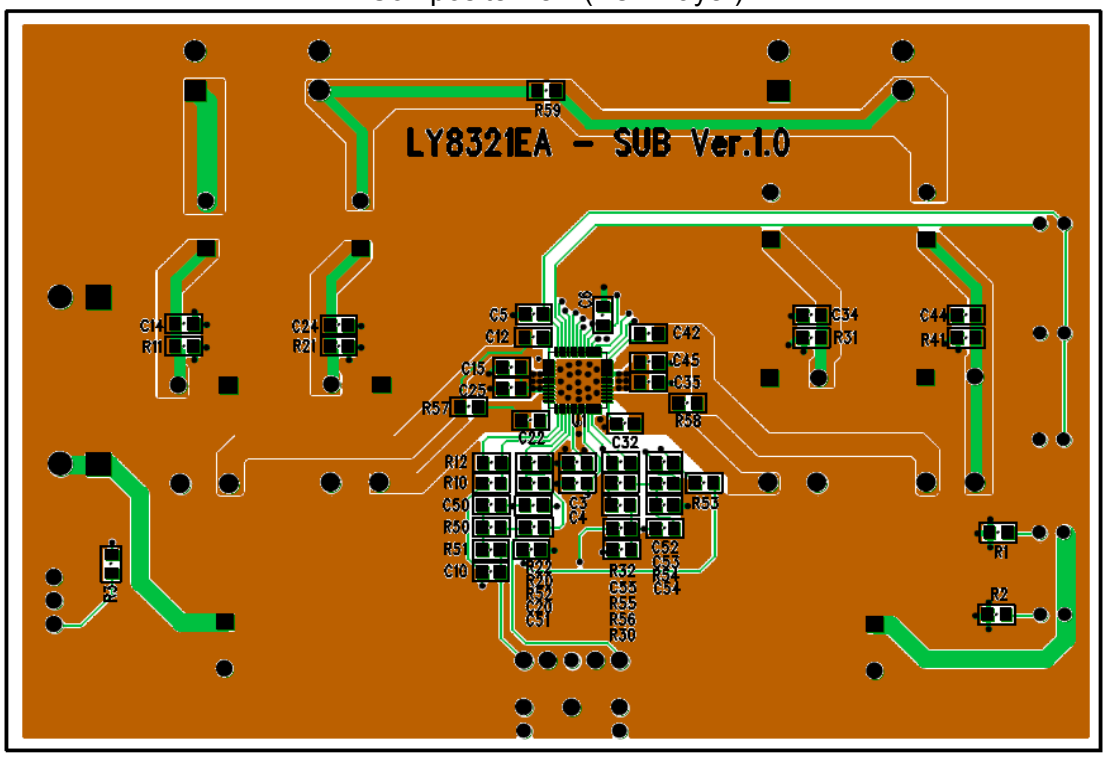
Top Silkscreen



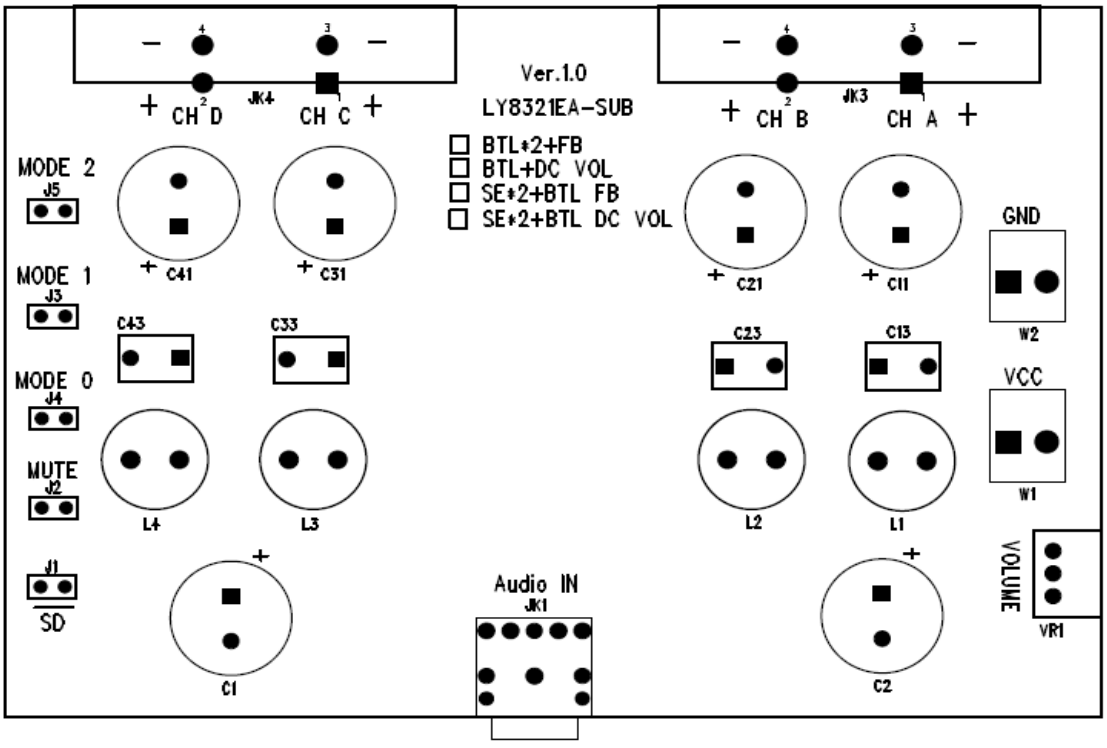
Top Layer



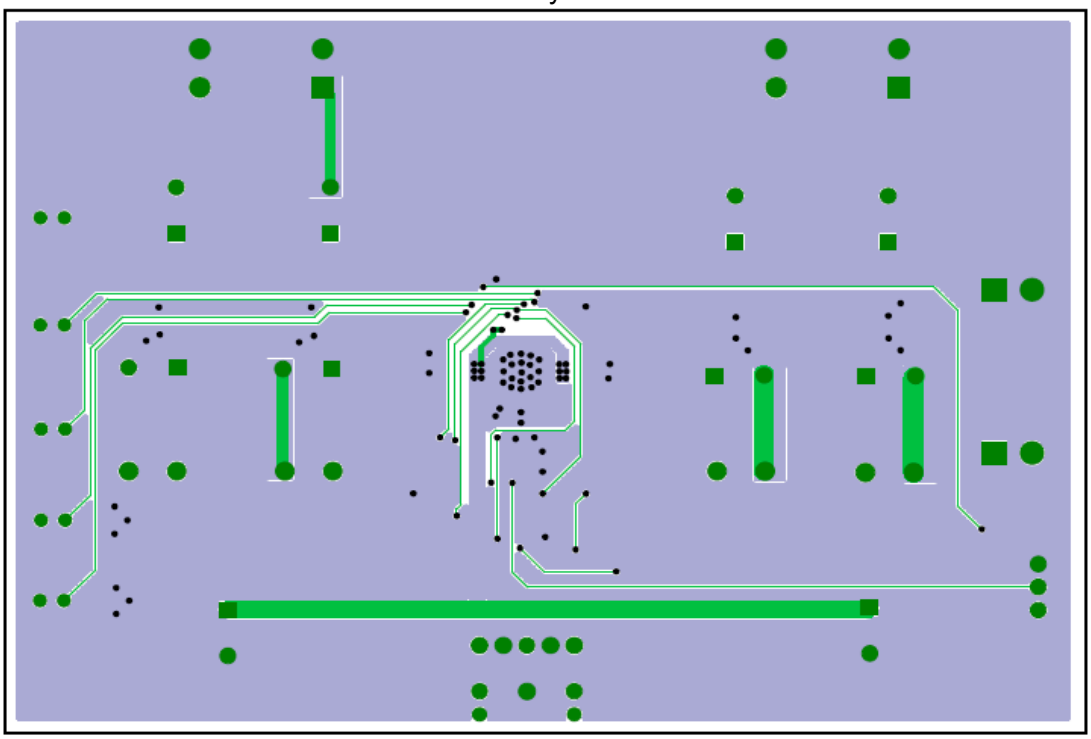
Composite view (TOP Layer)



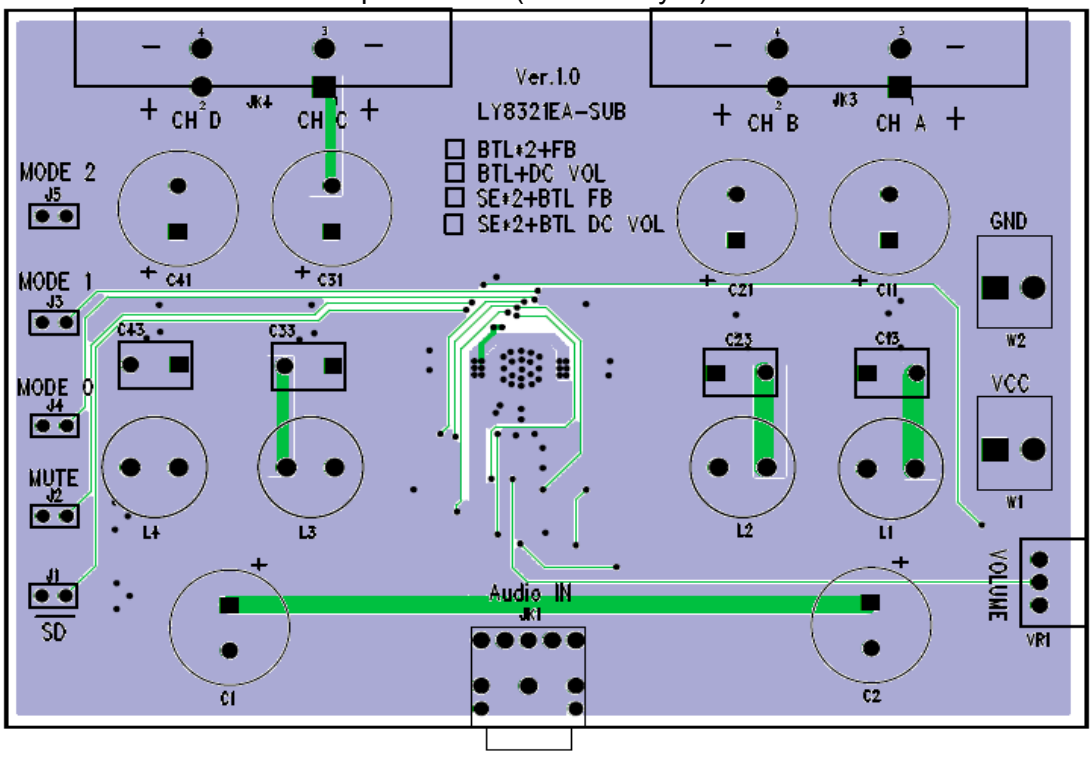
Bottom Silkscreen



Bottom Layer

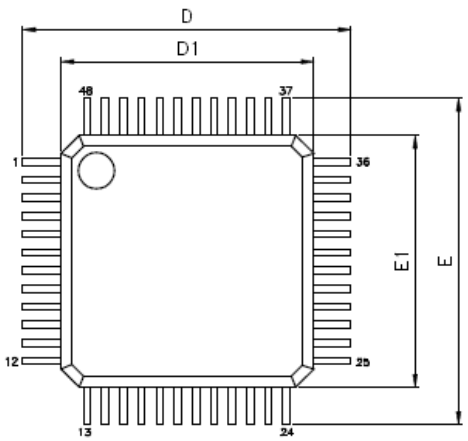


Composite view (Bottom Layer)



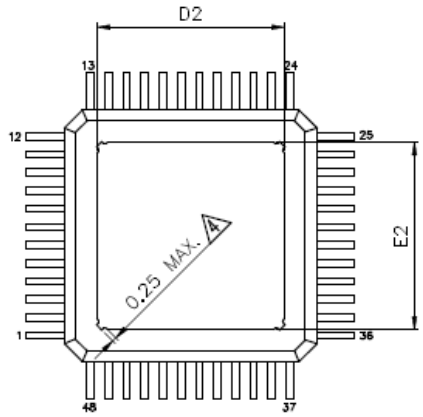
PACKAGE OUTLINE DIMENSION

LQFP 48 Pin Package Outline Dimension



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



THERMALLY ENHANCED VARIATIONS ONLY

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
205X20E	4.31	5.21	4.31	5.21