

November 2013

FDD7N60NZ / FDU7N60NZTU N-Channel UniFETTM II MOSFET 600 V, 5.5 A, 1.25 Ω

Features

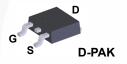
- $R_{DS(on)}$ = 1.05 Ω (Typ.) @ V_{GS} = 10 V, I_D = 2.75 A
- · Low Gate Charge (Typ. 13 nC)
- Low C_{rss} (Typ. 7 pF)
- 100% Avalanche Tested
- · Improved dv/dt Capability
- · ESD Improved Capability
- · RoHS Compliant

Applications

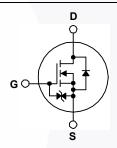
- Lighting
- · Uninterruptible Power Supply

Description

UniFETTM II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest onstate resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFETTM II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FDD7N60NZTM/ FDU7N60NZTU	Unit
V _{DSS}	Drain to Source Voltage			600	V
V _{GSS}	Gate to Source Voltage			±25	V
	Drain Current	- Continuous (T _C = 25°C)		5.5	^
ID	Drain Current	- Continuous (T _C = 100°C)		3.3	Α
I _{DM}	Drain Current	- Pulsed	(Note 1)	22	Α
E _{AS}	Single Pulsed Avalanche Ener	rgy	(Note 2)	347	mJ
I _{AR}	Avalanche Current		(Note 1)	5.5	Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	12.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	10	V/ns
D	Davier Dissination	$(T_C = 25^{\circ}C)$		90	W
P_{D}	Power Dissipation	- Derate Above 25°C		0.7	W/°C
T _J , T _{STG}	Operating and Storage Tempe	erature Range		-55 to +150	°C
T _L	Maximum Lead Temperature f	for Soldering, 1/8" from Case for s	Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FDD7N60NZTM/ FDU7N60NZTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	90	C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD7N60NZTM	FDD7N60NZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units
FDU7N60NZTU	FDU7N60NZ	IPAK	Tube	N/A	N/A	75 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	eteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	600	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.6	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	50	
IDSS	Zeio Gale vollage Didili Cultelli	$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	100	μА
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±10	μΑ

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 2.75 A	-	1.05	1.25	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 2.75 A	-	7.3	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05 V V 0 V		-	550	730	pF
Coss	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-\	70	90	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12		- \	7	10	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 5.5 A,		- \	13	17	nC
Q _{gs}	Gate to Source Gate Charge	V _{GS} = 10 V		-	3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	5.6	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			-	17.5	45	ns
t _r	Turn-On Rise Time	$V_{DD} = 250 \text{ V}, I_D = 5.5 \text{ A},$		- /	30	70	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 25 \Omega$		-	40	90	ns
t _f	Turn-Off Fall Time		(Note 4)	-	25	60	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Dioc	Maximum Continuous Drain to Source Diode Forward Current		-	5.5	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	22	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 5.5 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 5.5 A,	-	250	_	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.4	-	μС

Notes:

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 23 mH, I_{AS} = 5.5 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C.
- 3. I $_{SD}$ \leq 5.5 A, di/dt \leq 200 A/ μ s, V $_{DD}$ \leq BV $_{DSS}$, starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

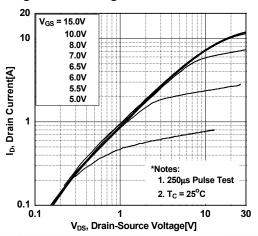


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

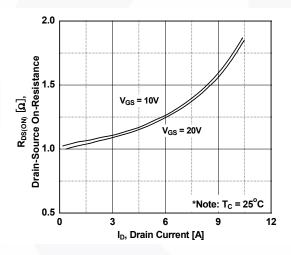


Figure 5. Capacitance Characteristics

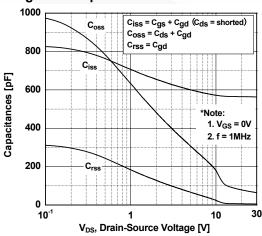


Figure 2. Transfer Characteristics

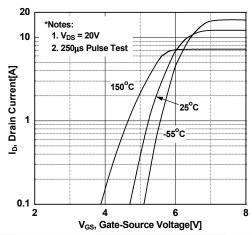


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

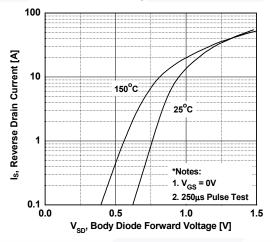
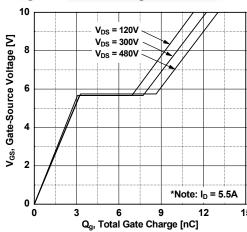


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

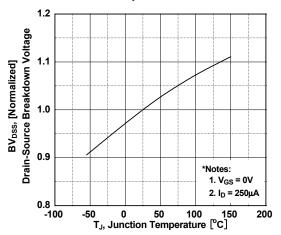


Figure 9. Maximum Safe Operating Area

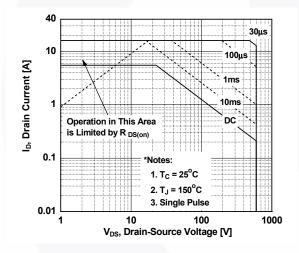


Figure 8. On-Resistance Variation vs. Temperature

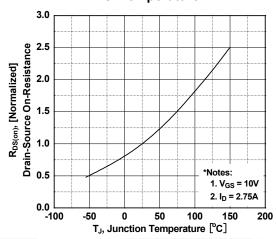


Figure 10. Maximum Drain Current vs. Case Temperature

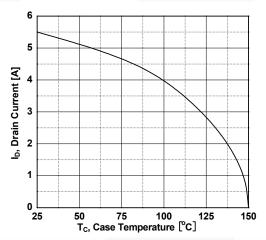
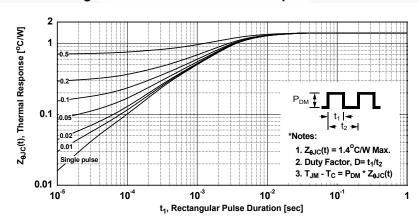


Figure 11. Transient Thermal Response Curve



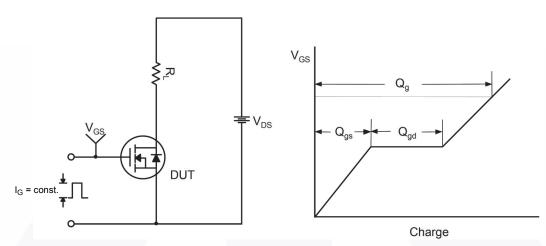


Figure 12. Gate Charge Test Circuit & Waveform

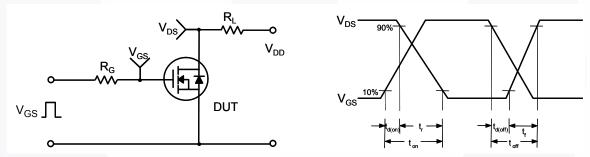


Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

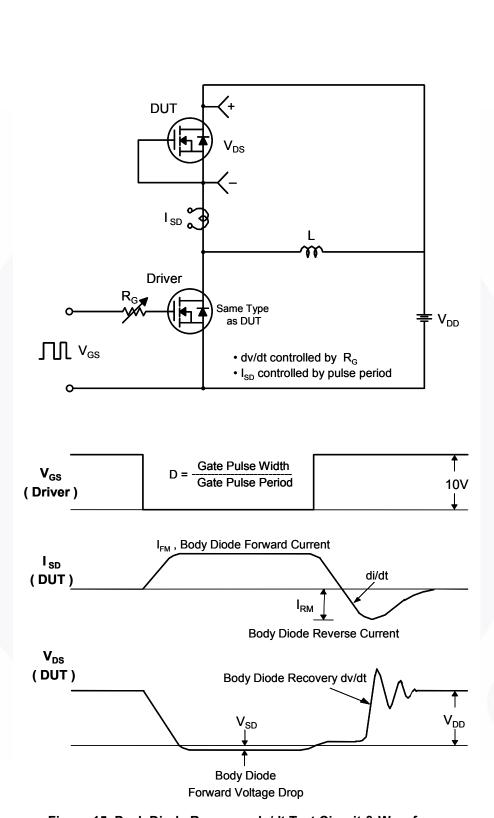


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

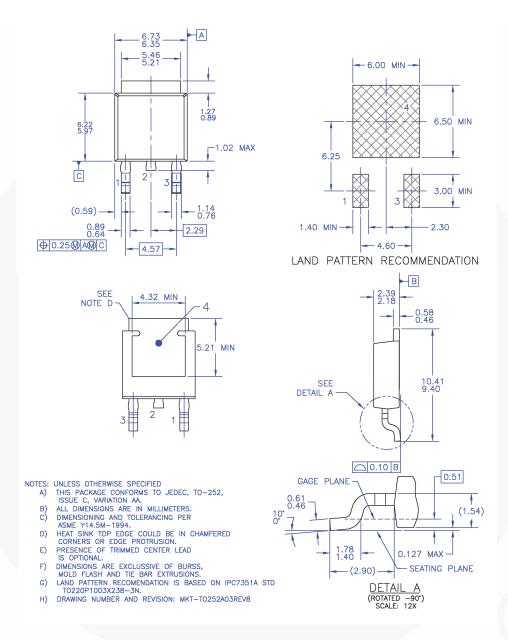


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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Mechanical Dimensions

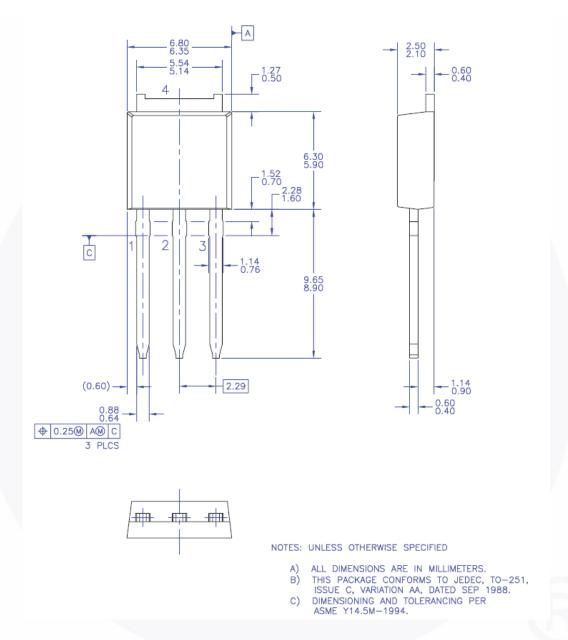


Figure 17. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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