



SPP4435W P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP4435W is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

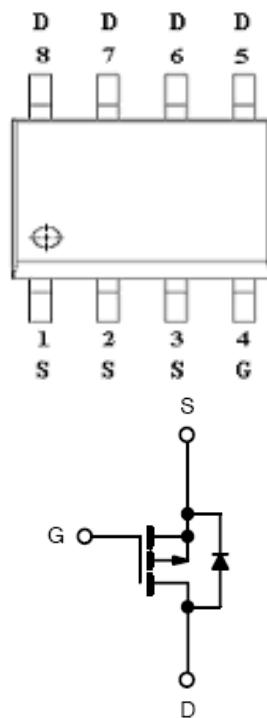
FEATURES

- ◆ -30V/-9.2A,R_{DS(ON)}= 24mΩ@V_{GS}=- 10V
- ◆ -30V/-7.0A,R_{DS(ON)}= 30mΩ@V_{GS}=-4.5V
- ◆ Super high density cell design for extremely low RDS (ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)



PART MARKING



A : Lot Code
B : Date Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP4435WS8RGB	SOP- 8P	SPP4435W

※ SPP4435WS8RGB : 13" Tape Reel ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	ID	A
	T _A =70°C		
Pulsed Drain Current	I _{DM}	-50	A
Continuous Source Current(Diode Conduction)	I _S	-2.3	A
Power Dissipation	T _A =25°C	P _D	W
	T _A =70°C		
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	70	°C/W



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ELECTRICAL CHARACTERISTICS

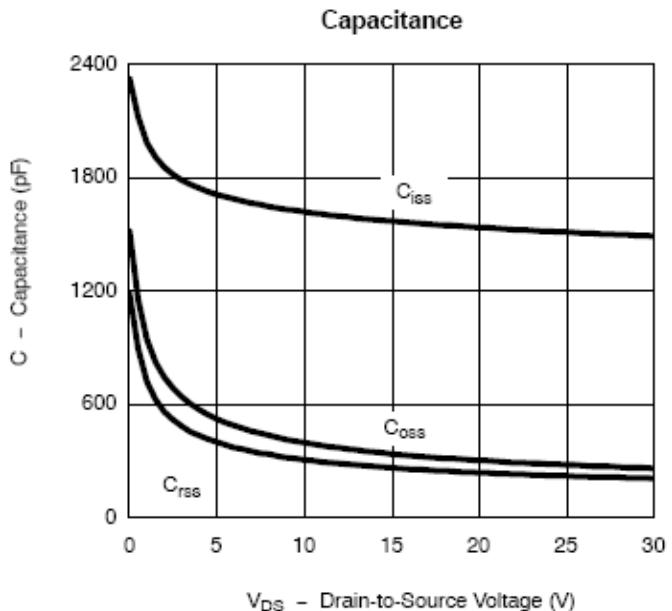
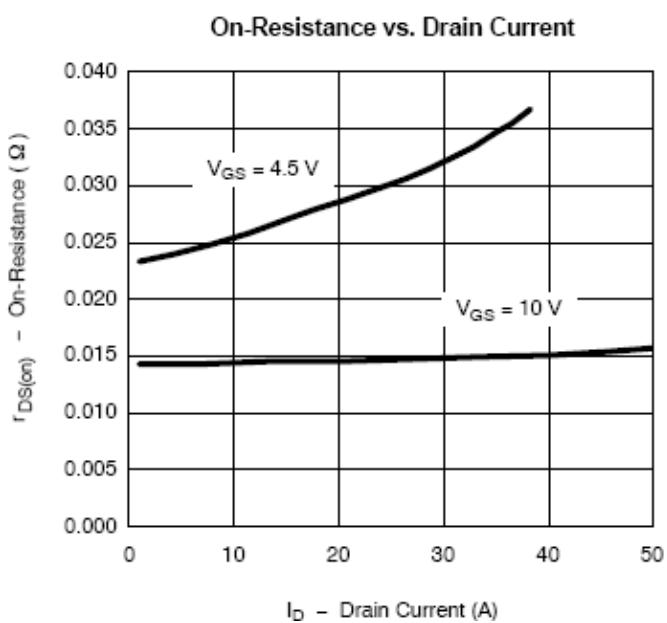
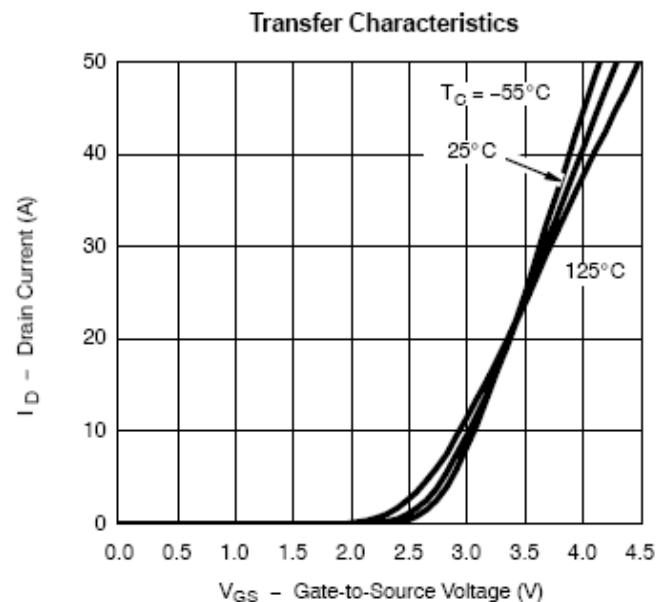
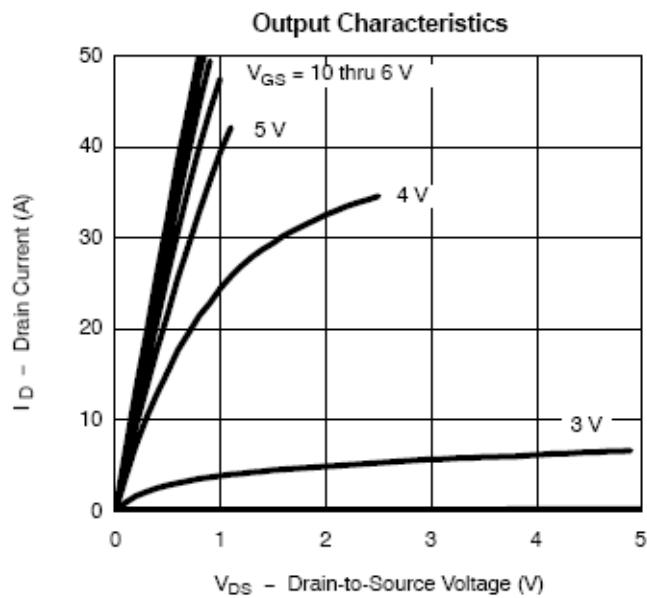
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V(BR)DSS	VGS=0V, ID=-250uA	-30			V
Gate Threshold Voltage	VGS(th)	VDS=VGS, ID=-250uA	-0.7		-1.6	
Gate Leakage Current	IGSS	VDS=0V, VGS=±20V			±100	nA
Zero Gate Voltage Drain Current	IDSS	VDS=-24V, VGS=0V			-1	uA
		VDS=-24V, VGS=0V TJ=55°C			-5	
On-State Drain Current	ID(on)	VDS= -5V, VGS =-4.5V	-40			A
Drain-Source On-Resistance	RDS(on)	VGS=-10V, ID=-9.2A		0.020	0.024	Ω
		VGS=-4.5V, ID=-7.0A		0.025	0.030	
Forward Transconductance	gfs	VDS=-10V, ID=-9.0A		24		S
Diode Forward Voltage	VSD	IS=-2.3A, VGS =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Qg	VDS=-15V, VGS=-10V ID= -9.0A		20	30	nC
Gate-Source Charge	Qgs			3.5		
Gate-Drain Charge	Qgd			4.8		
Input Capacitance	Ciss	VDS=-15V, VGS=0V f=1MHz		1850		pF
Output Capacitance	Coss			450		
Reverse Transfer Capacitance	Crss			335		
Turn-On Time	td(on)	VDD=-15V, RL=15Ω ID=-1.0A, VGEN=-10V RG=6Ω		20	30	nS
	tr			20	30	
Turn-Off Time	td(off)			75	110	
	tf			40	80	



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TYPICAL CHARACTERISTICS

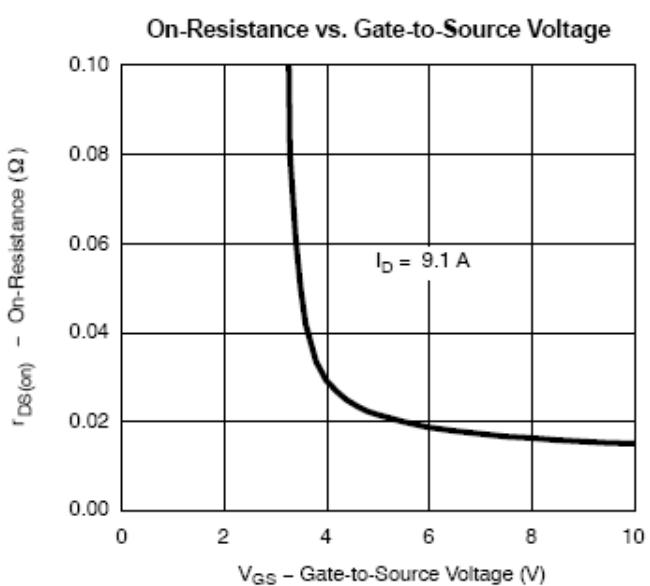
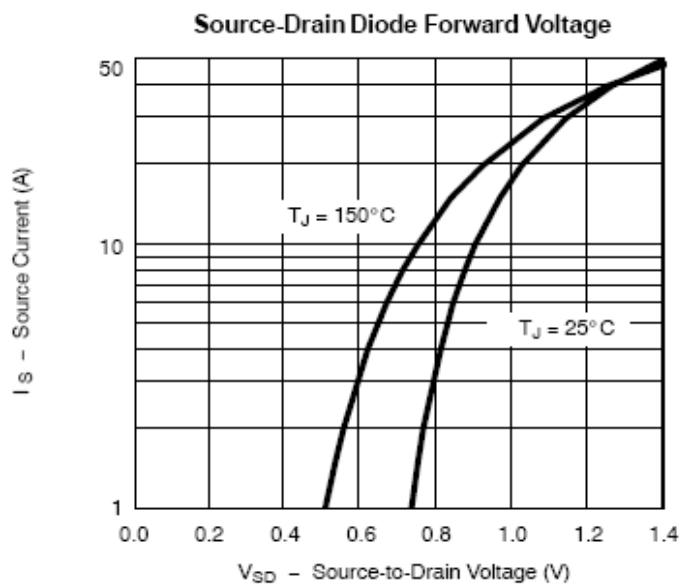
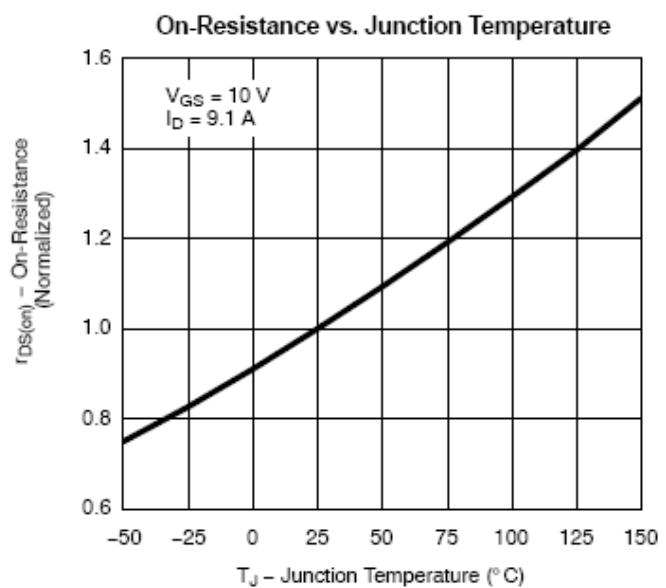
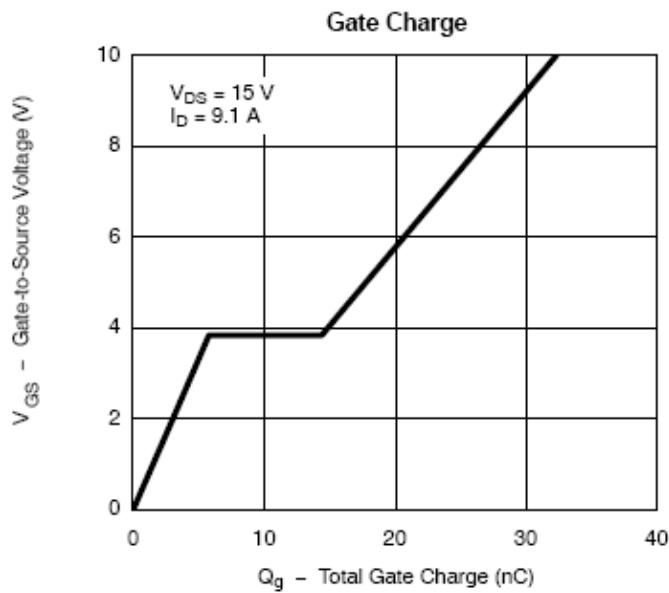




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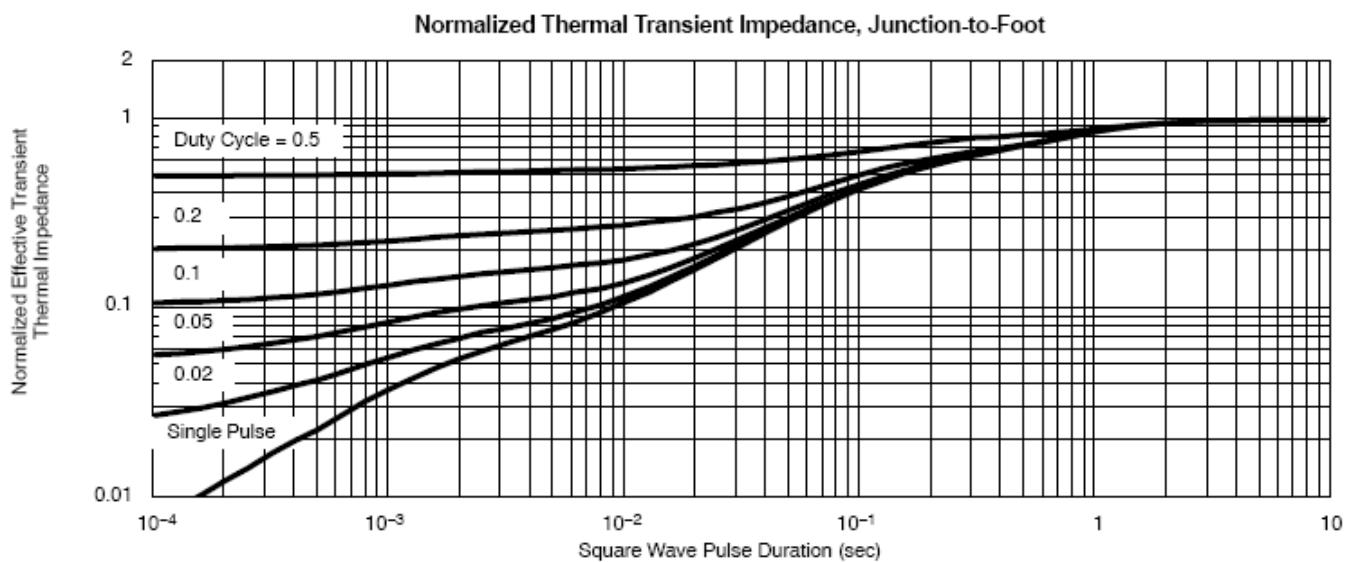
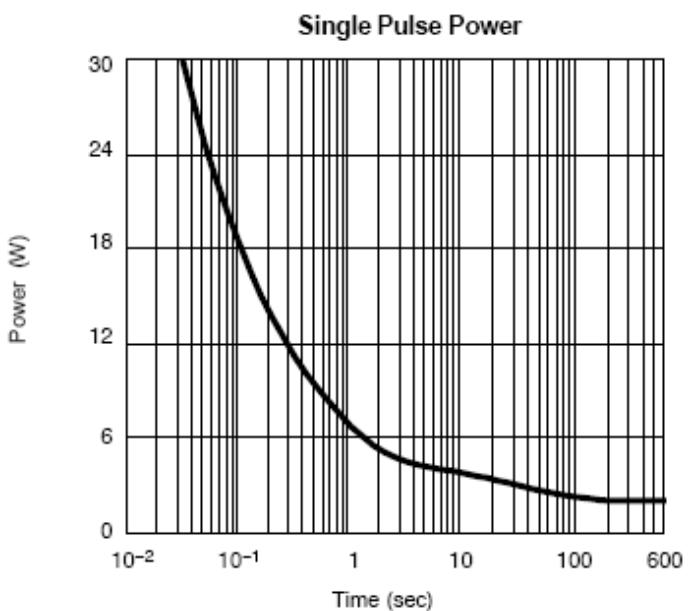
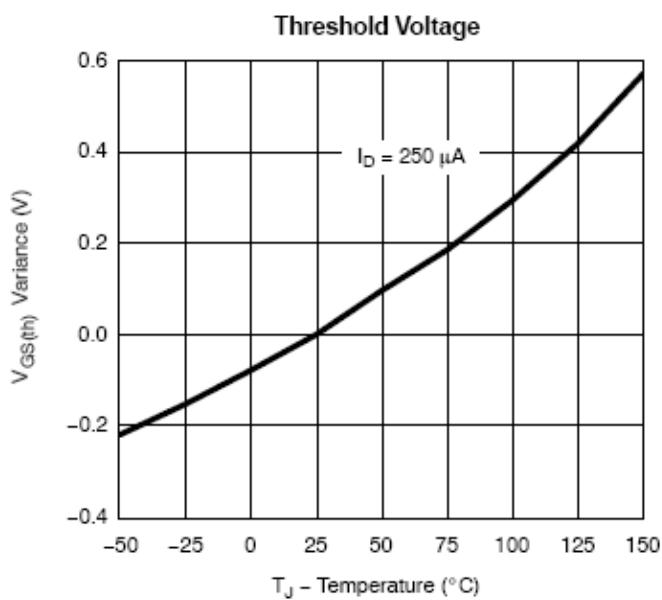




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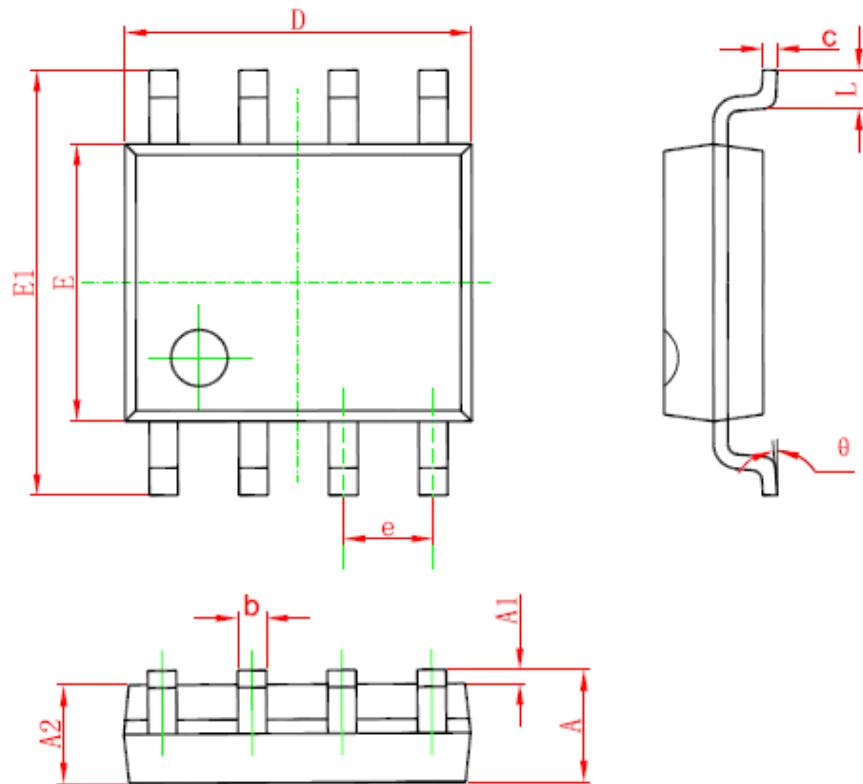




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SOP- 8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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