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Circuit Note
CN-0046

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| Devices Connected/Referenced | |
|---|---|
| AD8352 | Ultralow Distortion Differential RF/IF Amplifier |
| AD9445 | 14-Bit, 105 MSPS/125 MSPS Analog-to-Digital Converter |

# Using the AD8352 as an Ultralow Distortion Differential RF/IF Front End for High Speed ADCs

## CIRCUIT FUNCTION AND BENEFITS

These circuits provide both a single-ended and a differential configuration for driving high speed ADCs using the AD8352 ultralow distortion differential RF/IF amplifier. The AD8352 provides the gain, isolation, and distortion performance necessary for efficiently driving high linearity converters, such as the AD9445. This device also provides balanced outputs whether driven differentially or single-ended, thereby maintaining excellent second-order distortion levels.

## CIRCUIT DESCRIPTION

Figure 1 and Figure 2 illustrate two front-end circuits for driving the AD9445 14-bit ADC at 105 MSPS. Figure 1 provides a differential input configuration, while Figure 2 provides a single-ended input configuration.

In the differential configuration shown in Figure 1, the input 49.9 Ω resistor provides a differential input impedance to the 50 Ω RF/IF source. When the driver is located less than approximately one eighth of the wavelength of the maximum input RF/IF frequency from the AD8352, impedance matching is not required, thereby eliminating the need for this termination resistor. The output 24 Ω series resistors provide isolation from the input capacitance of the ADC, and the optimum value is determined empirically. The 100 MHz FFT plots shown in Figure 3 and Figure 4 display the performance results for the differential configuration.

In the single-ended input configuration shown in Figure 2, the net input impedance at $V_{IP}$ is $R_N$ (200 Ω) plus the external 24.9 Ω balancing resistor, or ~225 Ω. This requires a 64.9 Ω parallel resistor to provide the input impedance match for a 50 Ω source. If input reflections are minimal, this impedance match is not required. The 200 Ω resistor ($R_N$) is required to balance the output voltages to minimize second-order distortion.

The single-ended configuration provides −3 dB bandwidths similar to input differential drive and shows little or no degradation in overall third-order harmonic performance. The single-ended, third-order distortion levels are similar to the

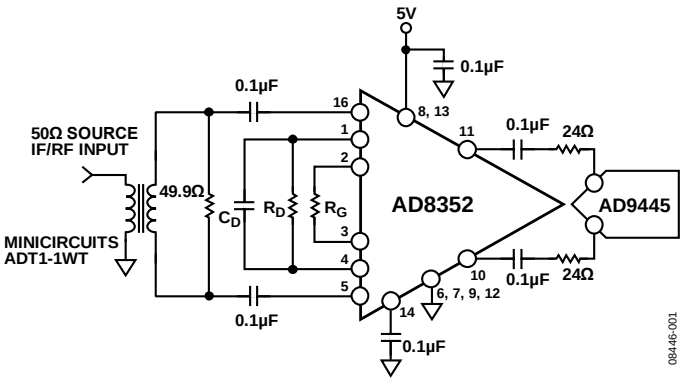


*Figure 1. Differential Input to the AD8352 Driving the AD9445 14-Bit, 105 MSPS/125 MSPS ADC (Simplified Schematic, All Connections Not Shown)*



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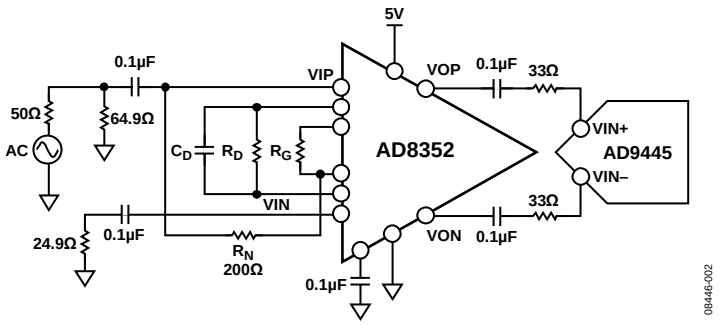


*Figure 2. Single-Ended Input to the AD8352 Driving the AD9445 ADC (Simplified Schematic, All Connections Not Shown)*

differential FFT plots in Figure 3 and Figure 4. The single-ended circuit avoids the use of a transformer or balun in front of the amplifier while still maintaining excellent distortion up to approximately 100 MHz. However, at frequencies above approximately 100 MHz, second-order distortion increases when the AD8352 is driven single-ended due to phase-related errors.

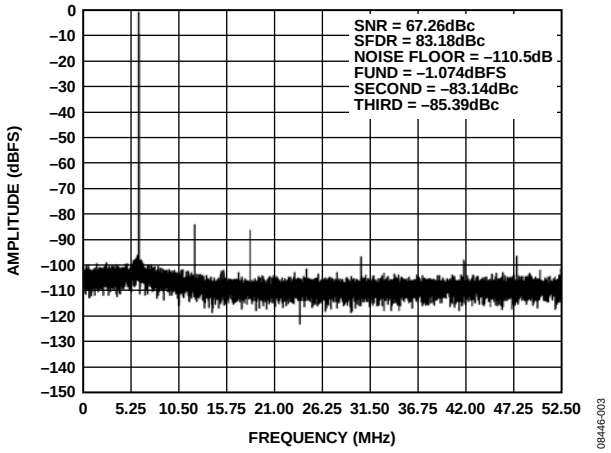


*Figure 3. Single Tone Distortion, AD8352 Driving AD9445, Sampling Clock = 105 MSPS, Analog Input Frequency = 100 MHz, $A_V$ = 10 dB. See Figure 1.*

In both configurations, $R_G$ is the gain setting resistor for the AD8352, with the $R_D$ and $C_D$ components providing distortion cancellation. The AD9445 differential input impedance is approximately 2 kΩ in parallel with 5 pF and requires a 2.0 V p-p differential signal ($V_{REF}$ = 1 V) between $V_{IN+}$ and $V_{IN-}$ for a full-scale input signal.

The output of the amplifier is ac-coupled to allow for an optimum common-mode voltage at the ADC input. The common-mode voltage at the input of the AD9445 is set to 3.5 V by an internal network. Input ac-coupling can be required if the source also requires a common-mode voltage that is outside the optimum range of the AD8352. A $V_{CM}$ common-mode pin is provided on the AD8352 that equally shifts both input and output common-mode levels. Increasing the gain of the AD8352 increases the system noise and, thus, decreases the SNR (3.5 dB at 100 MHz input for $A_V$ = 10 dB) of the AD9445 when no filtering is used. However, it should be noted that amplifier gains from 3 dB to 18 dB, with proper selection of $C_D$ and $R_D$, do not appreciably affect distortion levels. These circuits, when configured properly, can result in SFDR performance of better than 87 dBc at 70 MHz and 82 dBc at 180 MHz input. Single-ended drive, with appropriate $C_D$ and $R_D$, gives similar results for SFDR and third-order intermodulation levels as shown in these figures.

Excellent layout, grounding, and decoupling techniques must be utilized in order to achieve the desired performance from the circuits discussed in this note. As a minimum, a 4-layer PCB should be used with one ground plane layer, one power plane layer, and two signal layers.

All IC power pins must be decoupled to the ground plane with low inductance multilayer ceramic capacitors (MLCC) of 0.01 µF to 0.1 µF (this is not shown in the diagrams for simplicity). Follow the recommendations on the individual data sheets for the ICs.

The product evaluation boards should be consulted for recommended layout and critical component placement. They can be accessed through the main product pages for the devices or their data sheets.

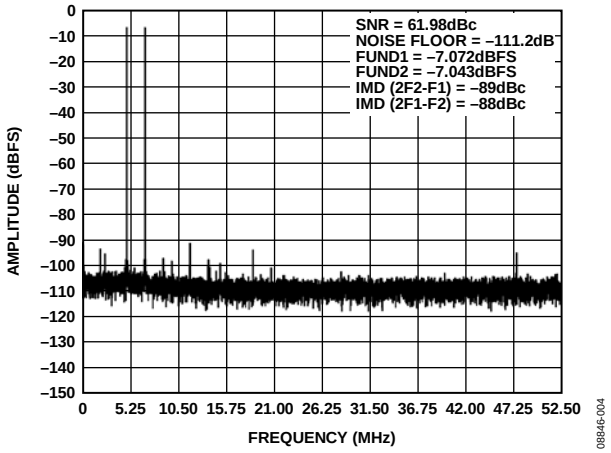


*Figure 4. Two Tone Intermodulation Distortion, AD8352 Driving AD9445, Sampling Clock = 105 MSPS, Analog Input Frequency = 98 MHz and 101 MHz, $A_V$ = 10 dB. See Figure 1.*

## COMMON VARIATIONS

Placing antialiasing filters between the ADC and the amplifier is a common approach for improving overall noise and broadband distortion performance for both band-pass and low-pass applications. For high frequency filtering, matching to the filter is required. The AD8352 maintains a 100 Ω output impedance well beyond most applications and is well-suited to drive most filter configurations with little or no degradation in distortion.

The AD8352 low distortion differential amplifier can be replaced by the high IP3, low noise figure AD8375 variable gain amplifier (VGA). The AD8375 is a digitally controlled, variable gain, wide bandwidth amplifier that provides precise gain control across a broad 24 dB gain range, with 1 dB resolution. The AD8376 is a dual version of the AD8375. (See Circuit Note CN-0002, *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*.)

## LEARN MORE

CN-0002 Circuit Note, *Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications*. Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*. Analog Devices.

MT-075 Tutorial, *Differential Drivers for High Speed ADCs Overview*. Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices.

### *Data Sheets*

AD8352 Data Sheet.

AD8375 Data Sheet.

AD8376 Data Sheet.

AD9445 Data Sheet.

AD9445 Evaluation Board.

High Speed ADC Evaluation Kits and Evaluation Boards.

## REVISION HISTORY

**8/09—Rev. 0 to Rev. A**

Updated Format ..... Universal

**10/08—Revision 0: Initial Version**