

Low Vcesat NPN Epitaxial Planar Transistor

BTD1805F3

Description

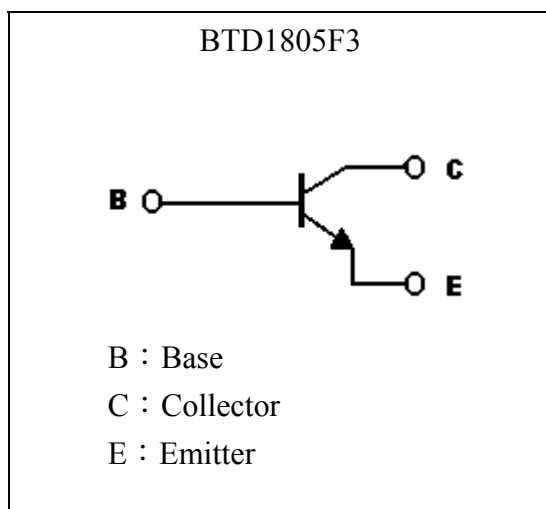
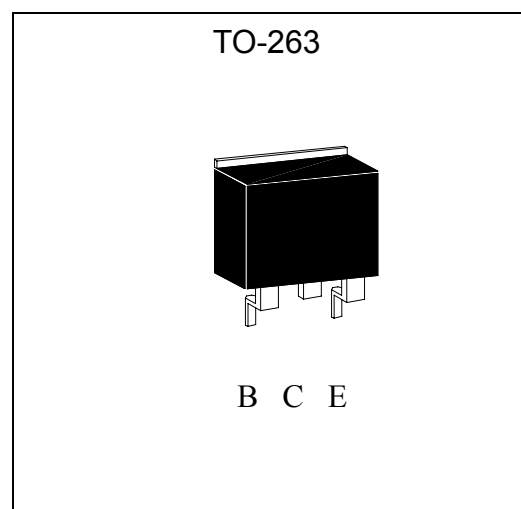
The device is manufactured in NPN planar technology by using a “Base Island” layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage.

Features

- Very low collector-to-emitter saturation voltage
- Fast switching speed
- High current gain characteristic
- Large current capability
- RoHS compliant package

Applications

- CCFL drivers
- Voltage regulators
- Relay drivers
- High efficiency low voltage switching applications

Symbol**Outline**



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage (IE=0)	V _{CBO}	150	V
Collector-Emitter Voltage (IB=0)	V _{CEO}	60	V
Emitter-Base Voltage (IC=0)	V _{EBO}	7	V
Collector Current (DC)	I _C	7	A
Collector Current (Pulse)	I _{CP}	12 (Note 1)	
Base Current	I _B	2	A
Power Dissipation @ TA=25°C	P _D	1.65	W
Power Dissipation @ TC=25°C	P _D	40	
Thermal Resistance, Junction to Ambient	R _{θJA}	75.8	°C/W
Thermal Resistance, Junction to Case	R _{θJC}	3.125	°C/W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : 1. Single Pulse , Pw ≤ 380μs, Duty ≤ 2%.

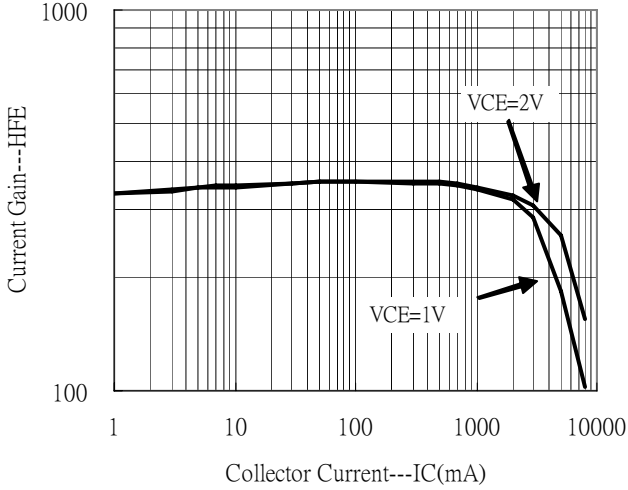
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	150	-	-	V	I _C =100μA, I _E =0
*BV _{CEO}	60	-	-	V	I _C =1mA, I _B =0
BV _{EBO}	7	-	-	V	I _C =100μA, I _C =0
I _{CBO}	-	-	100	nA	V _{CB} =150V, I _E =0
I _{EBO}	-	-	100	nA	V _{EB} =7V, I _C =0
*V _{CE(sat)} 1	-	-	50	mV	I _C =100mA, I _B =5mA
*V _{CE(sat)} 2	-	200	300	mV	I _C =2A, I _B =50mA
*V _{CE(sat)} 3	-	240	320	mV	I _C =3A, I _B =150mA
*V _{CE(sat)} 4	-	-	400	mV	I _C =5A, I _B =200mA
*V _{BE(sat)}	-	0.9	1.2	V	I _C =2A, I _B =100mA
*h _{FE} 1	200	-	400	-	V _{CE} =2V, I _C =100mA
*h _{FE} 2	100	-	-	-	V _{CE} =2V, I _C =5A
*h _{FE} 3	40	-	-	-	V _{CE} =2V, I _C =10A
f _T	-	150	-	MHz	V _{CE} =10V, I _C =50mA
C _{ob}	-	50	-	pF	V _{CB} =10V, f=1MHz
t _{on}	-	50	-	ns	V _{CC} =30V, I _C =10I _B 1=-10I _B 2=1A, R _L =30Ω
t _{stg}	-	1.35	-	μs	
t _f	-	120	-	ns	

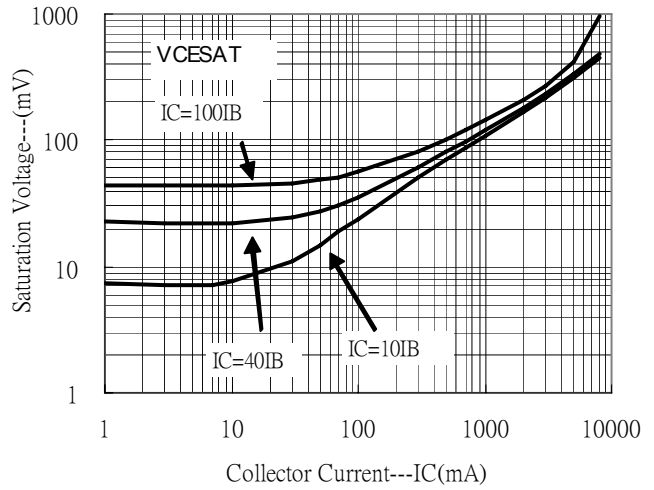
*Pulse Test : Pulse Width ≤ 380μs, Duty Cycles ≤ 2%

Typical Characteristics

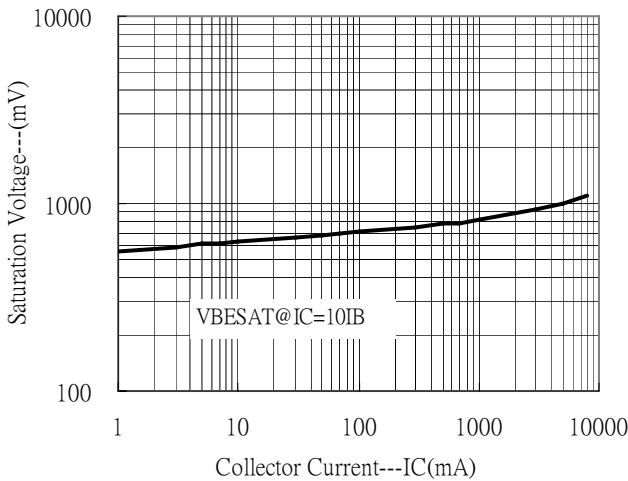
Current Gain vs Collector Current



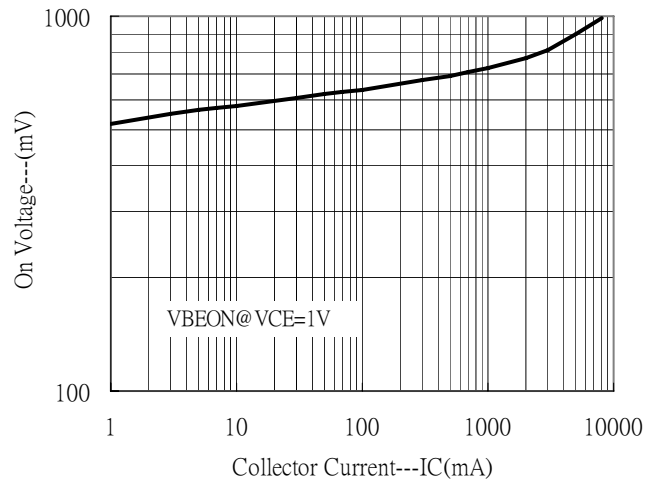
Saturation Voltage vs Collector Current



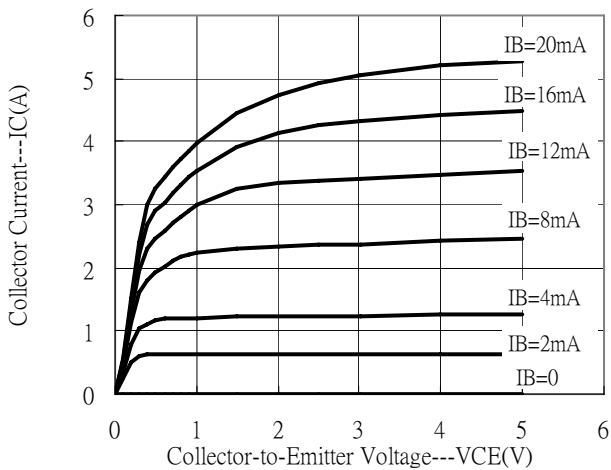
Saturation Voltage vs Collector Current



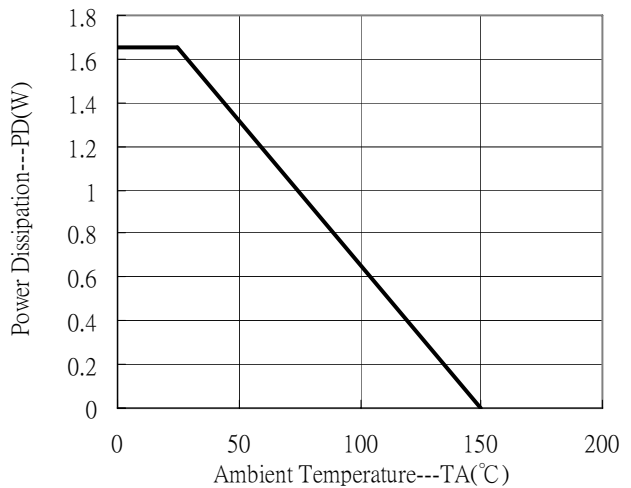
On Voltage vs Collector Current



Output Characteristics

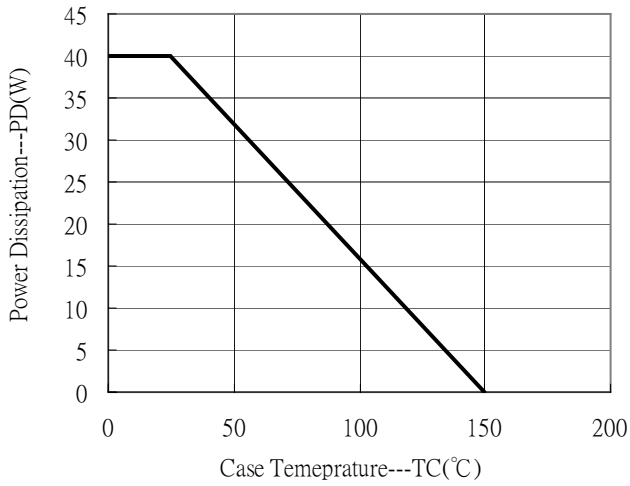


Power Derating Curve



Typical Characteristics(Cont.)

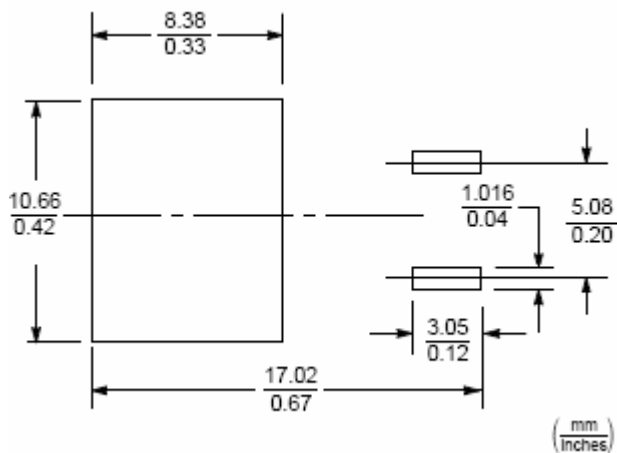
Power Derating Curve



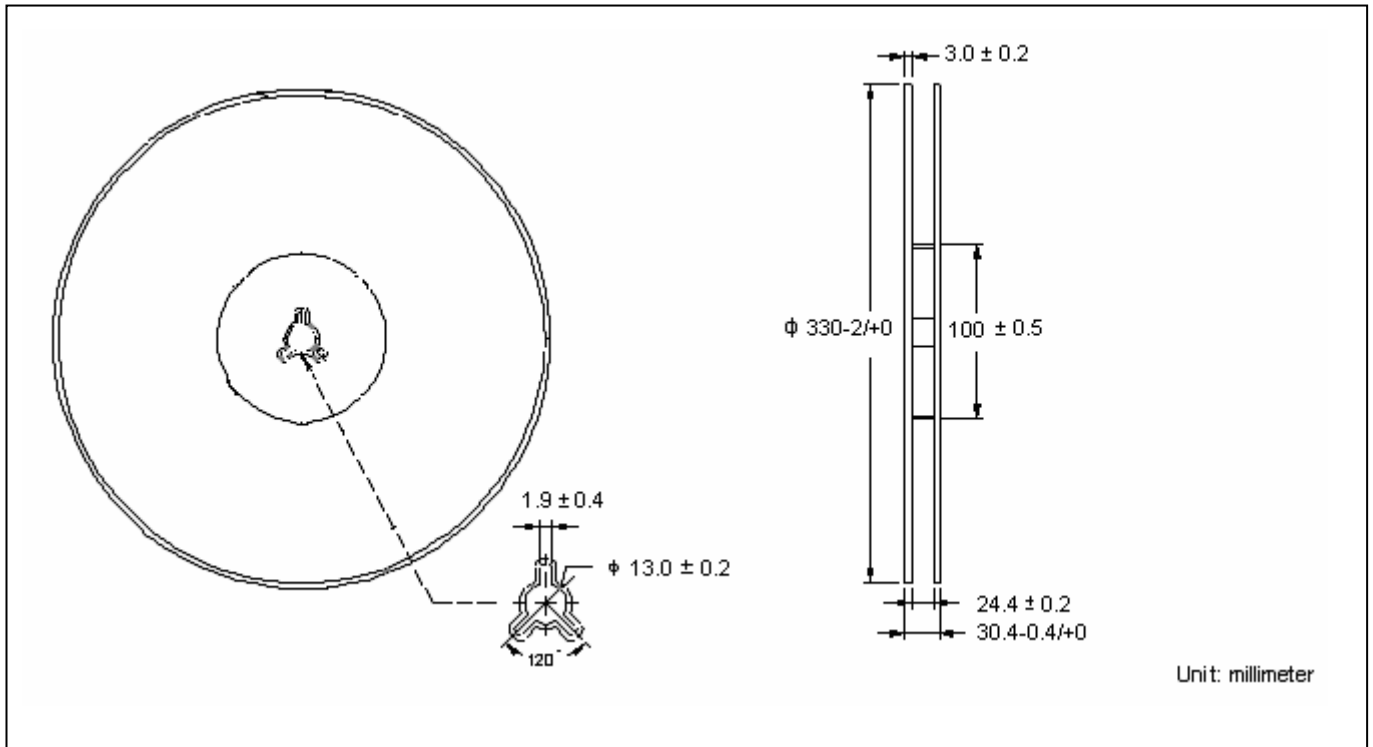
Ordering Information

Device	Package	Shipping
BTD1805F3	TO-263 (Pb-free lead plating)	800pcs / tape & reel

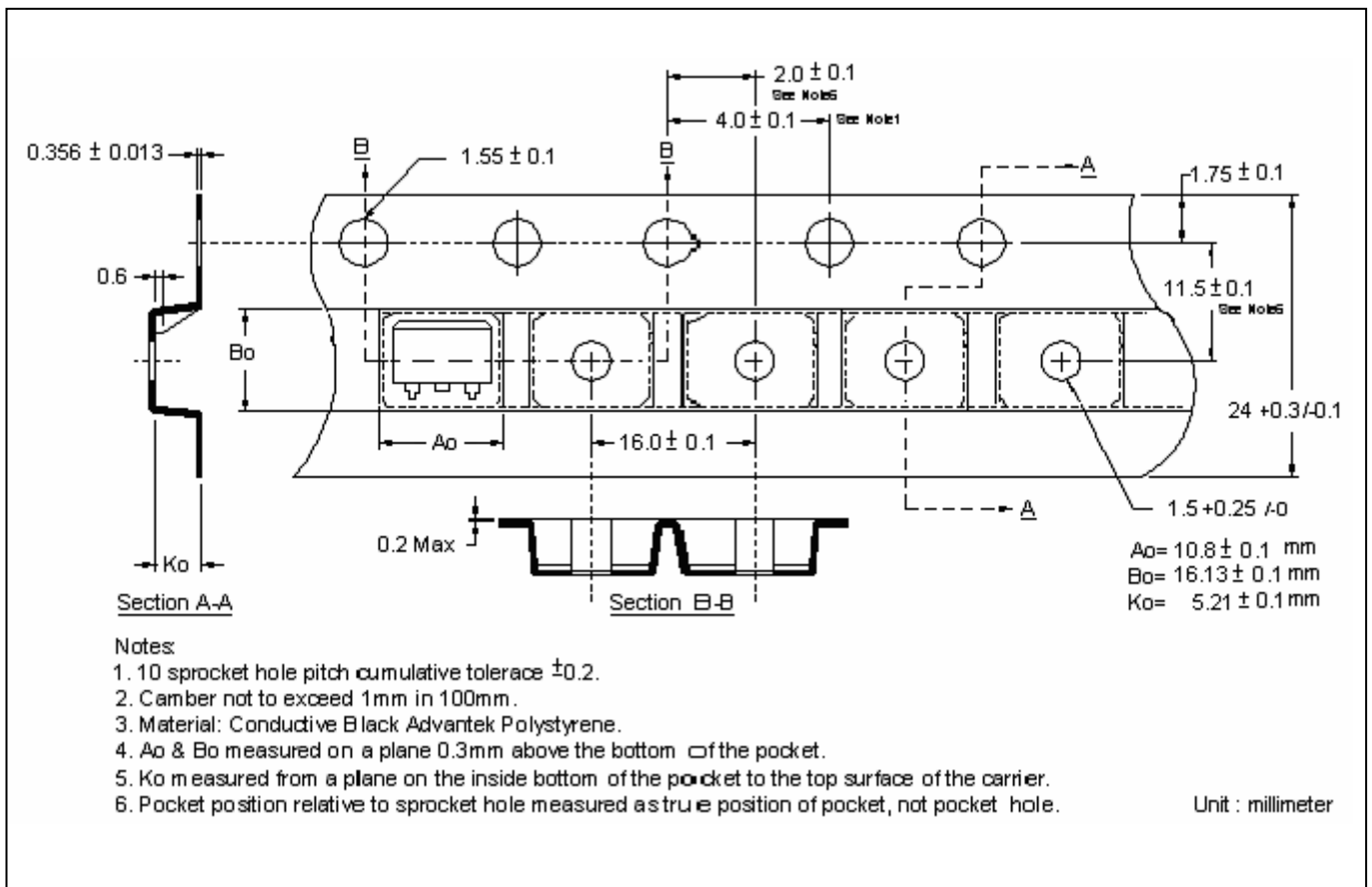
Recommended Soldering Footprint



Reel Dimension



Carrier Tape Dimension



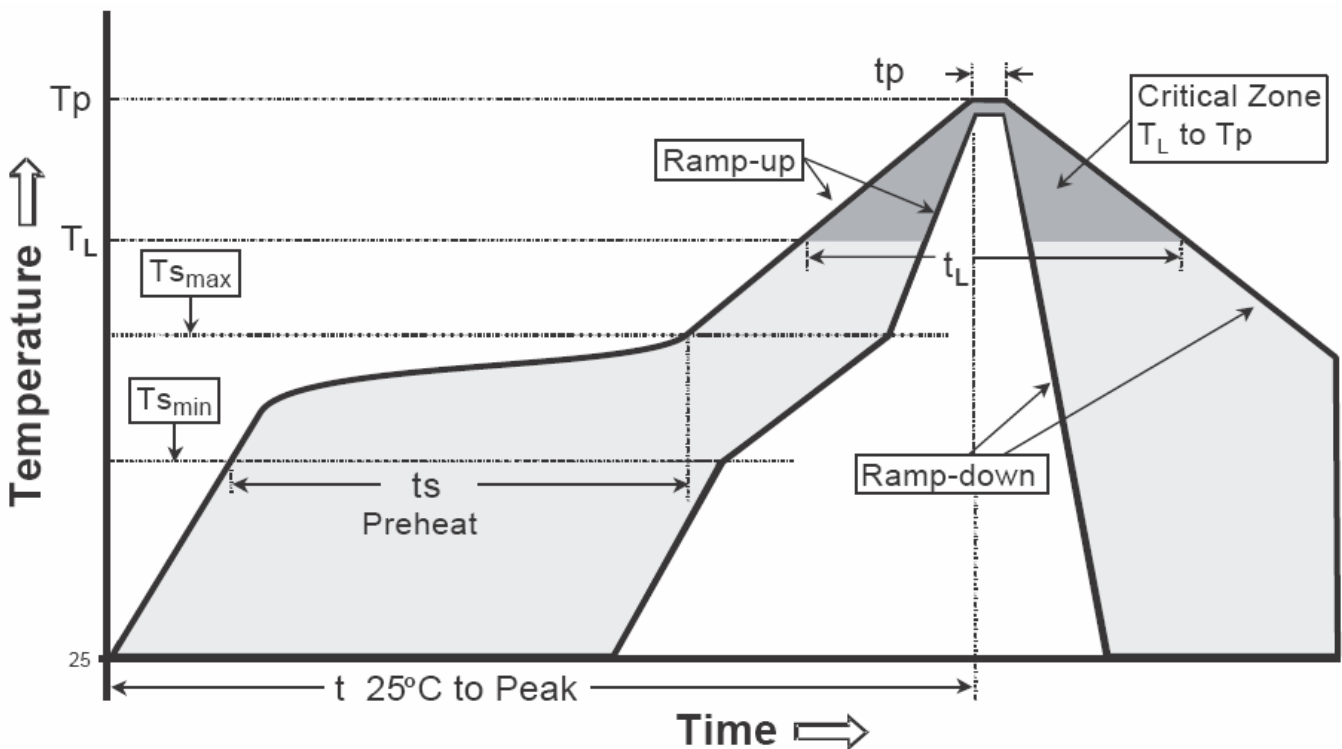
Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Advantek Polystyrene.
4. A_o & B_o measured on a plane 0.3mm above the bottom of the pocket.
5. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

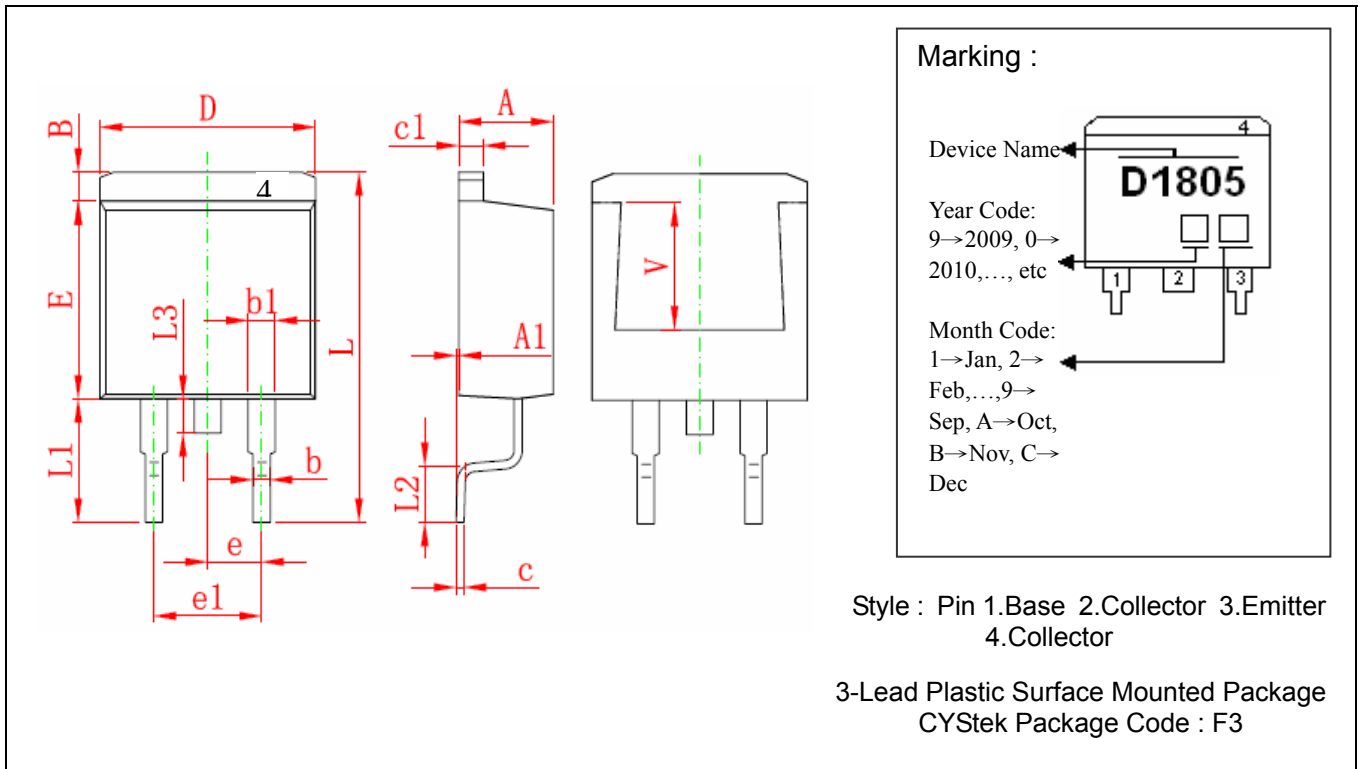
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-263 Dimension



Marking :

Device Name: **D1805**

Year Code:
 9→2009, 0→2010, ..., etc

Month Code:
 1→Jan, 2→Feb, ..., 9→Sep, A→Oct, B→Nov, C→Dec

Style : Pin 1.Base 2.Collector 3.Emitter 4.Collector

3-Lead Plastic Surface Mounted Package
 CYStek Package Code : F3

*:Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.060	4.830	0.160	0.190	E	8.380	9.400	0.330	0.370
A1	0.000	0.150	0.000	0.006	e	*2.540		*0.100	
B	1.170	1.400	0.046	0.055	e1	4.980	5.180	0.196	0.204
b	0.510	0.990	0.020	0.039	L	14.610	15.880	0.575	0.625
b1	1.140	1.400	0.045	0.055	L1	5.080	5.480	0.200	0.216
c	0.310	0.740	0.012	0.029	L2	2.290	2.790	0.090	0.110
c1	1.140	1.400	0.045	0.055	L3	1.270	1.780	0.050	0.070
D	9.650	10.310	0.380	0.406	V	5.600	REF	0.220	REF

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.