PRELIMINARY | COM'L: -7/10/12/15 IND: -10/12/14/18

MACH4-128/MACH4LV-128

High-Density EE CMOS Programmable Logic

VANTIS
The Programmable Logic Company From AMD

DISTINCTIVE CHARACTERISTICS

- **100 pins in PQFP, TQFP**
- **5-V and 3.3-V options**
  - — JEDEC compatible for both 5-V and 3.3-V versions
- **Fully pinout, function, and JEDEC programming data file compatible with MACH445**
- **Enhanced features**
  - — Bus-Friendly™ inputs and I/Os
  - — PAL® Block programmable power-down mode for further power savings
  - — Individual output slew rate control
  - — Both 5-V and 3.3-V supply operation versions are safe for mixed supply voltage system designs
- **5-V or 3.3-V in-system programmable through JTAG (IEEE Std. 1149.1) interface**
- **JTAG boundary scan testing capability**
- **128 macrocells**
- **7.5 ns t_{PD}**
- **133 MHz f_{CNT}**
- **70 Inputs**
- **64 Outputs**
- **192 flip-flops**
  - — 128 Macrocell flip-flops
  - — 64 Input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability and pinout retention**
- **Fixed, predictable, deterministic delays**
- **Zero-hold-time input register option**
- **Peripheral Component Interconnect (PCI) compliant (-7,-10, -12 speed grades)**

PLEASE NOTE: The MACH4-128 (M4-128) reflects a new nomenclature for the MACH® 4 Family. This device is currently dual-marked with the MACH446 ordering part number. The dual-mark scheme will facilitate design and manufacturing flows until we have completely phased in the new M4-128 nomenclature. Please use the MACH446/MACHLV446 data sheet (PID#21237) as a reference.

GENERAL DESCRIPTION

The MACH4-128 (M4-128) and MACH4LV-128 (M4LV-128) are members of Vantis' high-performance EE CMOS MACH 4 family. This device has approximately 12 times the macrocell capability of the popular PALCE22V10, with significant density and functional features that the PALCE22V10 does not provide.

The M4-128 (M4LV-128) consists of 8 PAL® blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix.

The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The M4-128 (M4LV-128) has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

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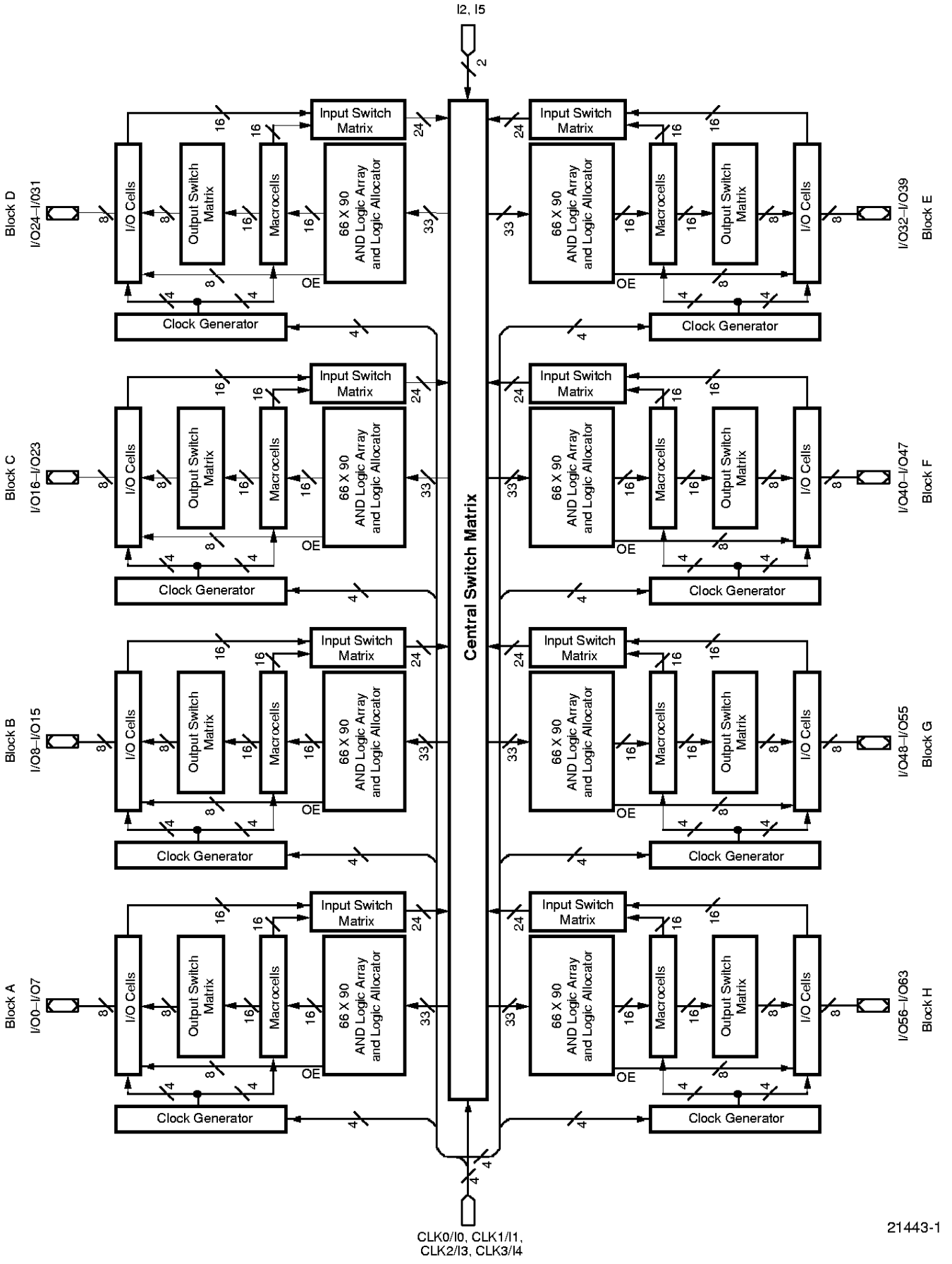
The M4-128 (M4LV-128) macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

The M4-128 (M4LV-128), an enhanced version of the MACH445, is fully pinout, function and JEDEC programming data file compatible with the MACH445. The enhanced features include: low power consumption; each PAL block has a programmable power-down mode for further power saving of up to 50%; each I/O has an individually programmable output slew-rate control bit; all inputs and I/Os feature the Bus-Friendly circuitry which weakly holds the voltage at the input to a logic low or high level depending on the last driven logic level. Both 5-V and 3.3-V supply operation versions are safe for mixed supply voltage system designs. The 3.3-V supply operation device power consumption is significantly reduced due to the lower required supply voltage, both versions 5-V and 3.3-V supply operation devices provide the same high performance.

MACH designs can be implemented using Vantis' MACHXL®, and industry-standard universal design software tools. Vantis and MINC have developed a strategic partnership that ensures timely universal software support for the MACH devices. MINC develops back-end PLD software for nearly every major industry-standard PLD and board-level design tools. This back-end software fits a design into a device and creates a JEDEC programming data file. Schematic capture, boolean, state machine, VHDL, and Verilog HDL design entry and simulation are features of the front-end tool. MINC produces the back-end for PC tools such as MicroSim's Design Center, Synario Design Automation's Synario, and others. MINC also supplies the back-end for workstation tools from Cadence, Mentor Graphics, Synopsys, and Viewlogic. The Vantis-MINC partnership provides timely, accurate, and quality support for MACH devices in almost every design environment. Please see Vantis' Universal Tools brochure for more information.

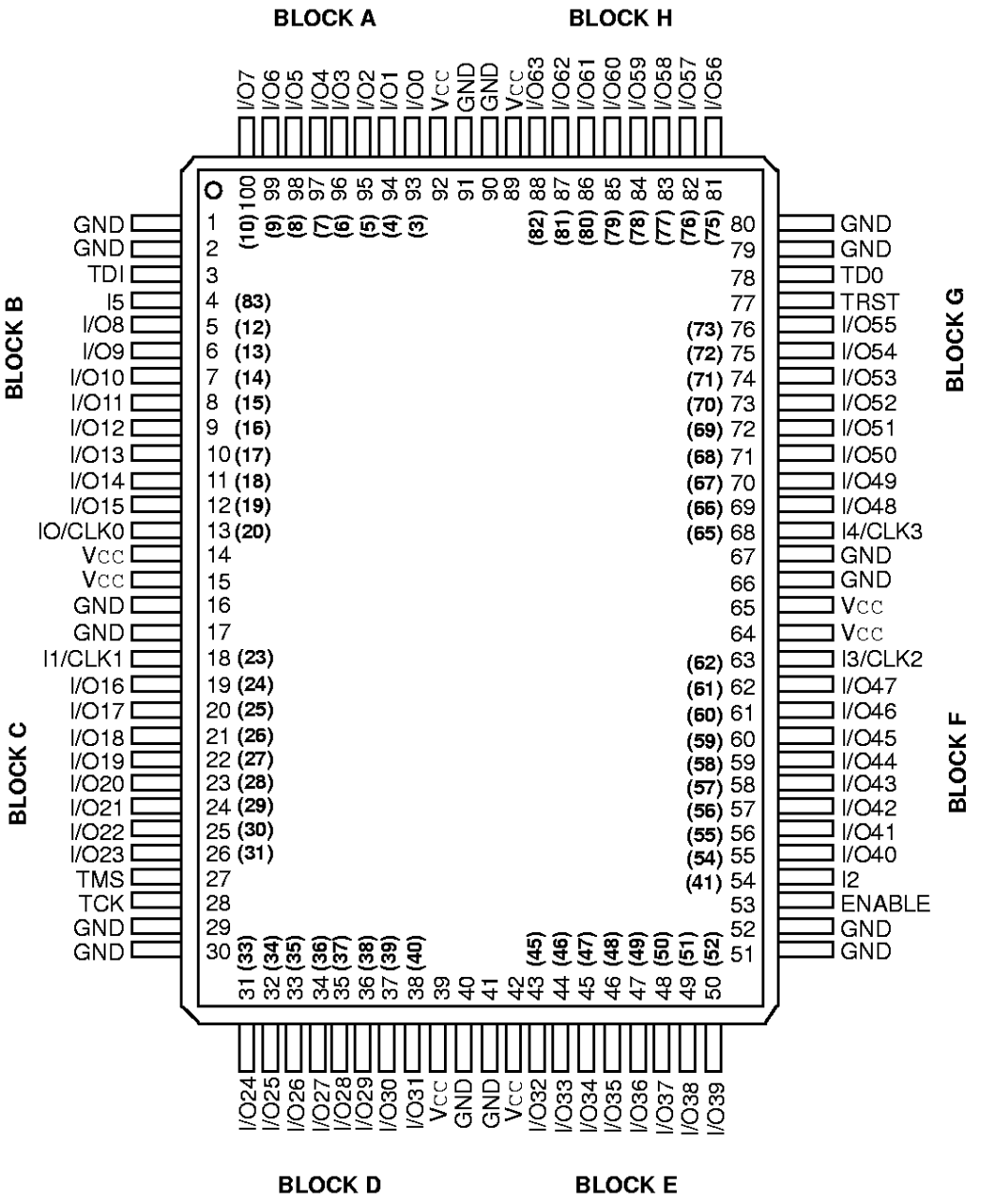
BLOCK DIAGRAM



CONNECTION DIAGRAM

Top View

PQFP



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

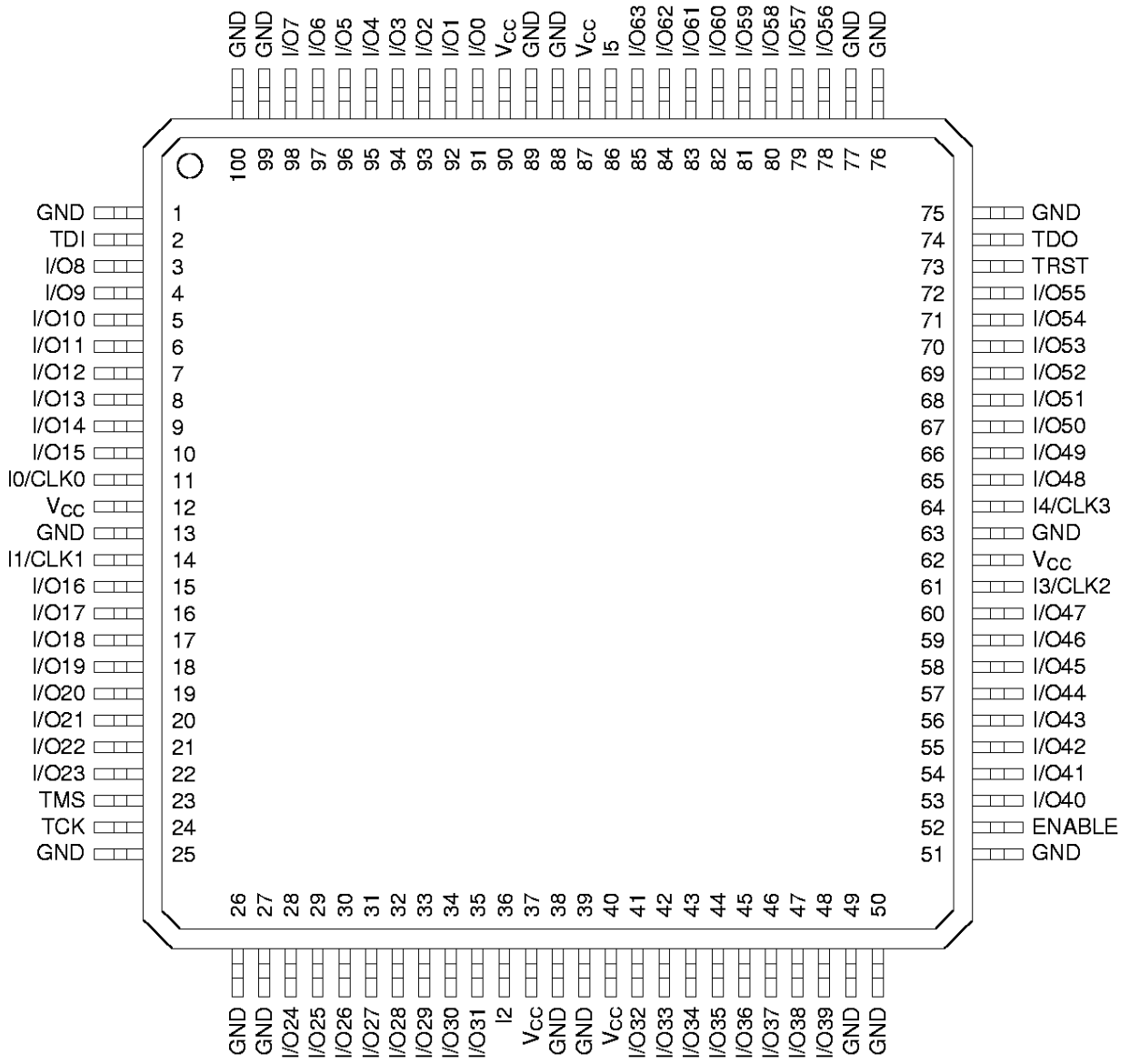
I/O = Input/Output

V_{CC}=Supply Voltage

CONNECTION DIAGRAM

Top View

100-Pin TQFP



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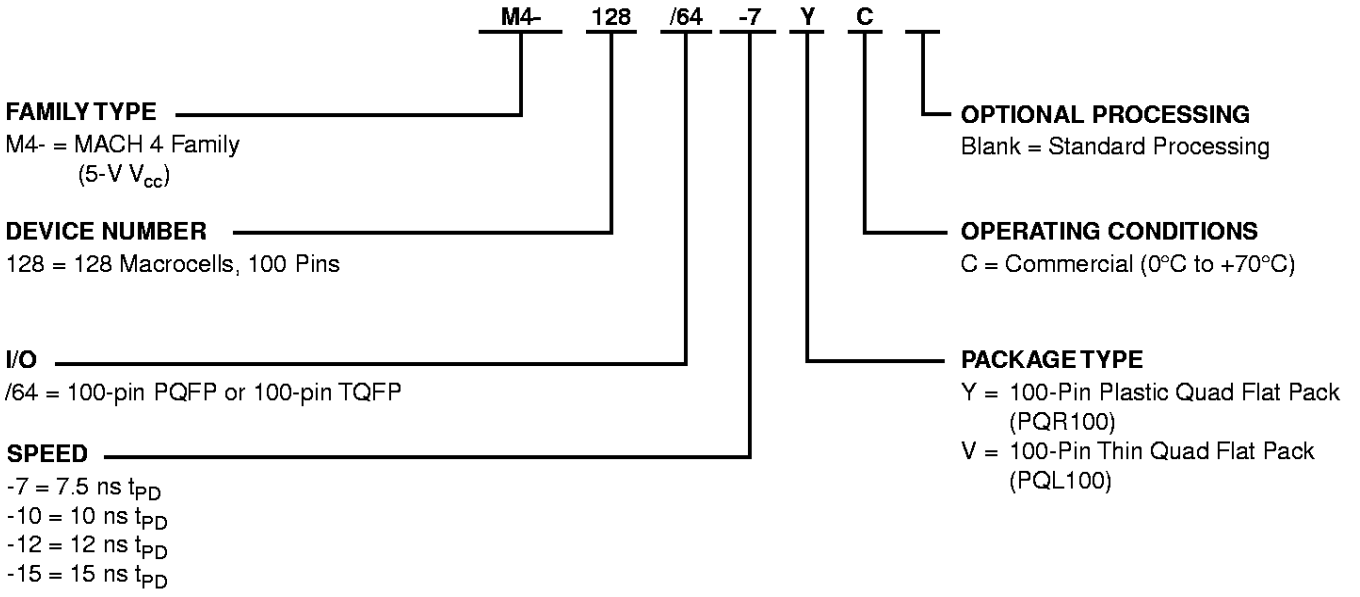
ORDERING INFORMATION

Commercial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
M4-128/64-7	YC, VC
M4-128/64-10	
M4-128/64-12	
M4-128/64-15	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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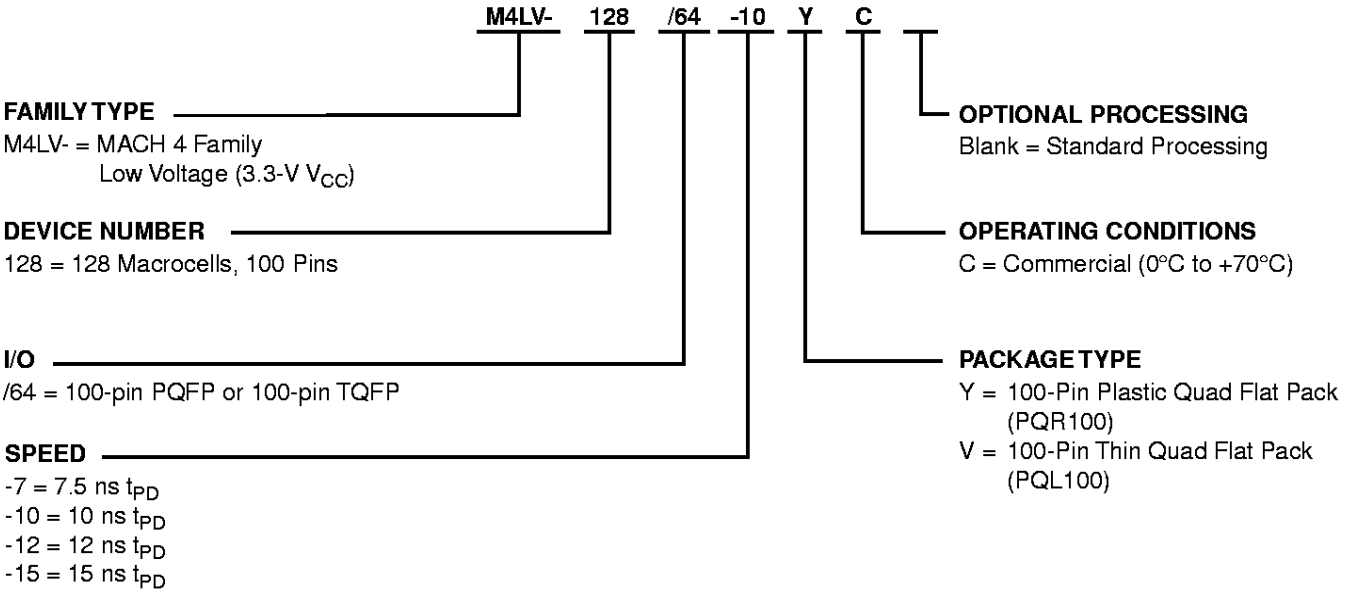

Valid Combinations	
M4LV-128/64-7	VC, YC
M4LV-128/64-10	
M4LV-128/64-12	
M4LV-128/64-15	

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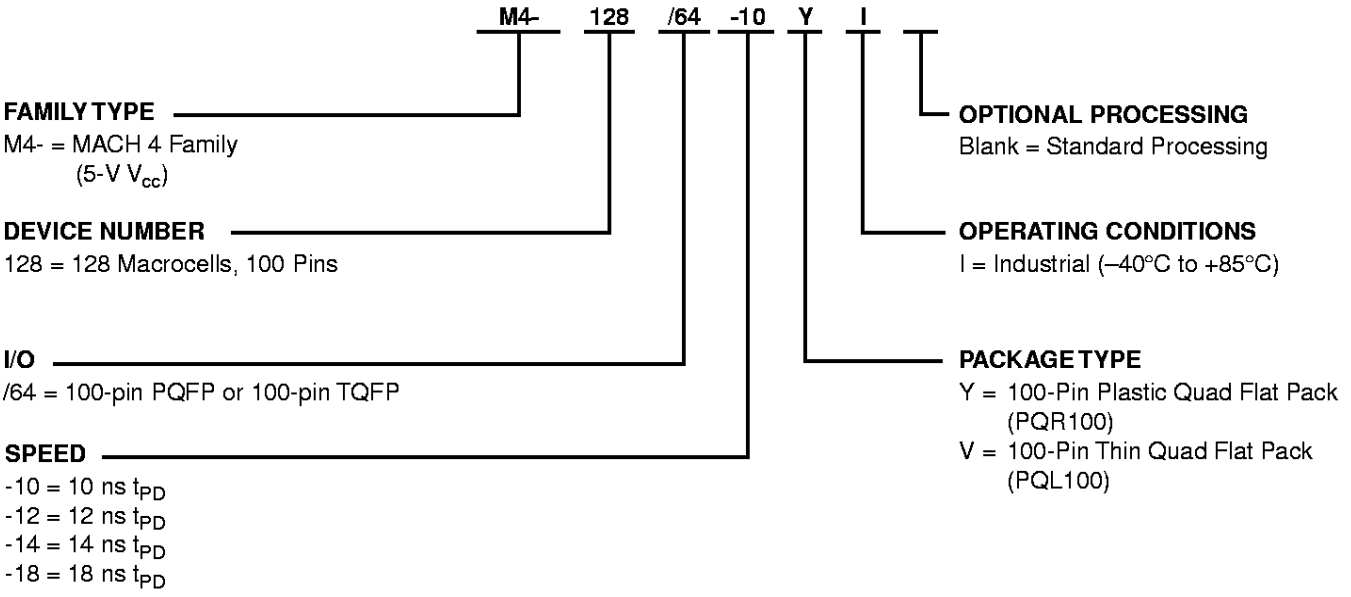

Valid Combinations	
M4-128/64-10	YI, VI
M4-128/64-12	
M4-128/64-14	
M4-128/64-18	

Valid Combinations

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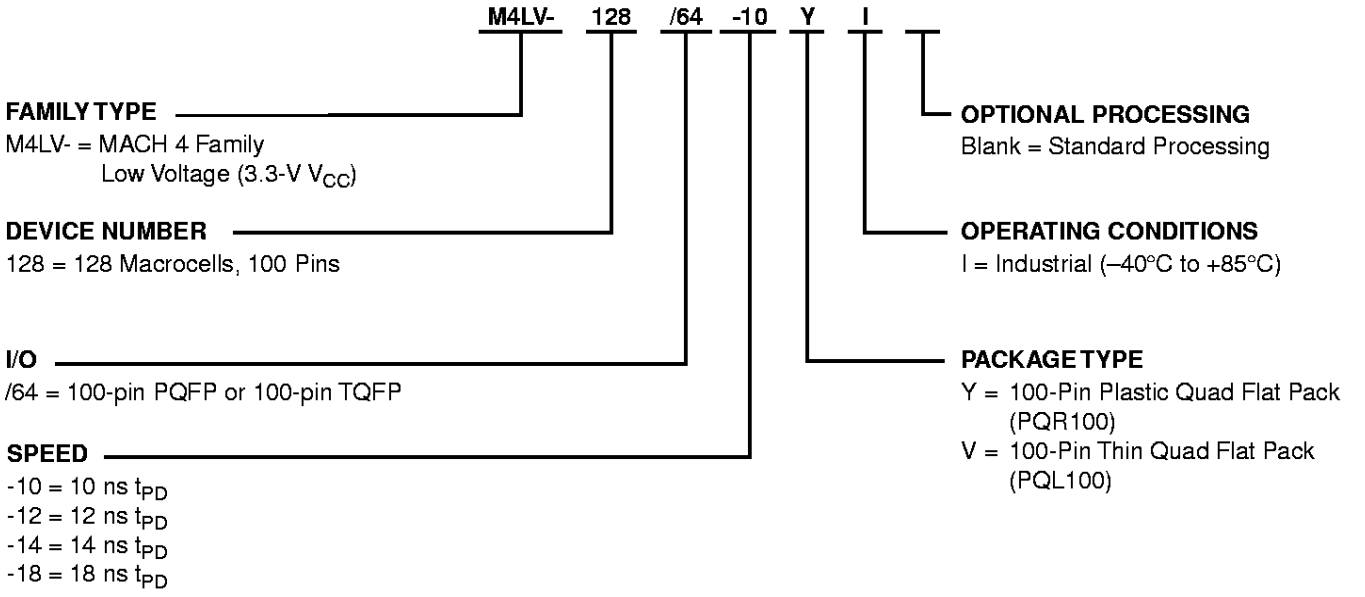


Valid Combinations	
M4LV-128/64-10	YI, VI
M4LV-128/64-12	
M4LV-128/64-14	
M4LV-128/64-18	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The M4-128 (M4LV-128) consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have bus-friendly latches. While it is always good design practice to tie unused pins high, the latches provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the M4-128 (M4LV-128) (Figure 1) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product terms are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The M4-128 (M4LV-128) central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The M4-128 (M4LV-128) product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the M4-128 (M4LV-128) takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms in synchronous mode, or 18 product terms in asynchronous mode. When product terms are routed away from a macrocell, all 5 product terms may be redirected, which precludes the use of the macrocell for logic generation. It is possible to redirect only 4 product terms, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. Emulating all flip-flop types with a D-type flip-flop is also made possible. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The M4-128 (M4LV-128) has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 2. Please refer to Figure 1 for macrocell and I/O pin numbers.

Table 2. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0,M1	I/O5,I/O6,I/O7,I/O0
M2,M3	I/O6,I/O7,I/O0,I/O1
M4, M5	I/O7,I/O0,I/O1,I/O2
M6,M7	I/O0,I/O1,I/O2,I/O3
M8, M9	I/O1,I/O2,I/O3,I/O4
M10,M11	I/O2,I/O3,I/O4,I/O5
M12, M13	I/O3,I/O4,I/O5,I/O6
M14,M15	I/O4,I/O5,I/O6,I/O7
I/O Pin	**Available Macrocells**
I/O0	M0,M1,M2,M3,M4,M5,M6,M7
I/O1	M2,M3,M4,M5,M6,M7,M8,M9
I/O2	M4,M5,M6,M7,M8,M9,M10,M11
I/O3	M6,M7,M8,M9,M10,M11,M12,M13
I/O4	M8,M9,M10,M11,M12,M13,M14,M15
I/O5	M10,M11,M12,M13,M14,M15,M0,M1
I/O6	M12,M13,M14,M15,M0,M1,M2,M3
I/O7	M14,M15,M0,M1,M2,M3,M4,M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the M4-128 (M4LV-128) consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1-1990. The JTAG standard defines input and output pins, logic control functions, and instructions. Vantis has incorporated this standard into the M4-128 (M4LV-128) device.

The JTAG standard was developed as a means of providing both board-level and device-level testing. Details on this feature can be found in the application note titled, *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices.*

5-V or 3.3-V In-System Programming

Another benefit from the JTAG circuitry that Vantis has derived is the ability to use the JTAG port for 5-V or 3.3-V in-system programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate PQFP or TQFP leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially, and it only requires the use of the Test Access Port. Use of the programming Enable pin (ENABLE*) is optional.

Details on this feature can also be found in the *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* application note.

Zero-Hold-Time Input Register

The M4-128 (M4LV-128) device has a zero-hold time (ZHT) fuse. This fuse controls the time delay associated with loading data into all I/O cell registers and latches in the M4-128 (4LV-128) device.

When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized.

This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Power-Down Mode

Each individual PAL block in the M4-128 (M4LV-128) features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slightly slower than those in the non-low-power PAL block. This feature allows speed critical signal paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

Bus-Friendly Inputs and I/Os

The M4-128 (M4LV-128) inputs and I/Os feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state and pulls the voltage away from the input threshold voltage. At power-up, the Bus-Friendly latches are reset to a logic level “1.” For an illustration of this configuration, please refer to the Input/Output Equivalent Schematics section.

Programmable Slew Rate

Each M4-128 (M4LV-128) I/O has an individually programmable output slew-rate control bit. Each output can be individually configured for the highest speed transition or for the lowest noise transition. In systems properly designed for high-speed applications, the fast slew-rate output option can be used to achieve the highest speed. However, the slower slew rate is more effective than the fast slew rate in keeping noise generation and ground bounce to the minimum level.

PCI Compliance

The M4-128 (M4LV-128) devices with speed grades -10 and -12 are compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The predictable timing of the M4-128 (M4LV-128) ensures compliance with the PCI timing specifications independent of the logic design fitting.

Safe for Mixed Supply Voltage Designs

The M4-128 (M4LV-128) is safe for mixed supply voltage system designs. The 5-V supply operation version device outputs will not drive above 3.3 V. Thus, it can safely drive any 3.3-V supply operation device. The 3.3-V supply operation version device inputs are 5-V tolerant.

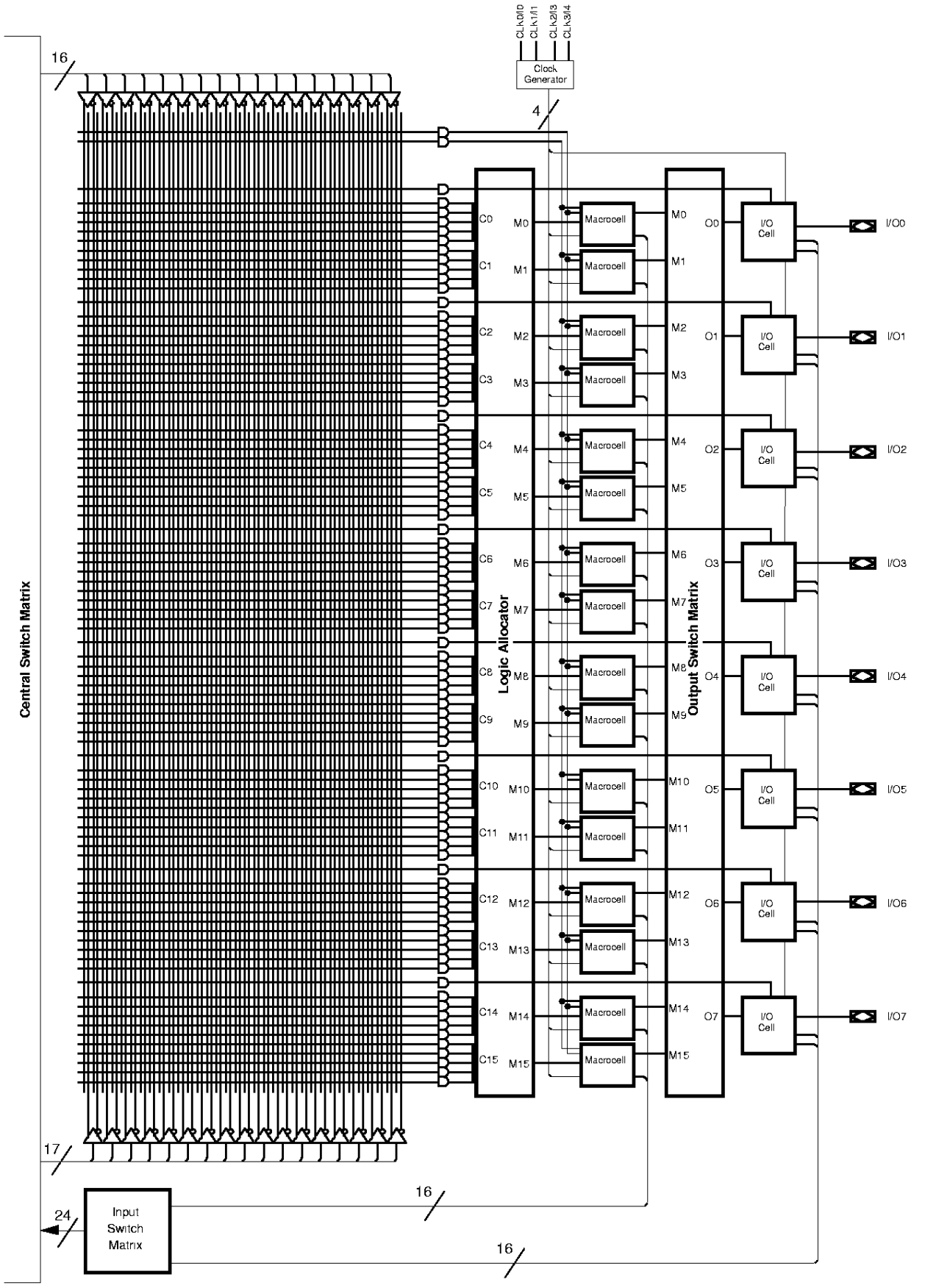


Figure 1. M4-128 (M4LV-128) PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +100°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = 0°C to +70°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	All PAL Blocks low-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		70		mA
		All PAL Blocks full-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		120		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	7.5	3	10	3	12	3	15	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	3.5		4		5		8		ns
				T-type	4.5		5		6		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				3.5		4		5		8		ns
t_{COA}	Product Term Clock to Output				4	9.5	4	12	4	14	4	18	ns
t_{WLA}	Product Term, Clock Width			LOW	4		5		8		9		ns
t_{WHA}				HIGH	4		5		8		9		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	74.0		62.5		52.6		38.5		MHz
				T-type	71.4		58.8		50.0		37		MHz
		Internal Feedback (f_{CNTA})		D-type	90.9		71.4		58.8		47.6		MHz
				T-type	83.3		66.7		55.6		45.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		125		100		62.5		55.6		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	5.5		6		7		10		ns
				T-type	6.5		7		8		11		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	5.5	2	6.5	2	8	2	10	ns
t_{WLS}	Global Clock Width			LOW	3		5		6		6		ns
t_{WHS}				HIGH	3		5		6		6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	90		80		66.7		50		MHz
				T-type	83.3		74.1		62.5		47.6		MHz
		Internal Feedback (f_{CNTS})		D-type	133		100		83.3		66.6		MHz
				T-type	117		90.9		76.9		62.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		166.7		100		83.3		88.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		4		5		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		-7		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{HLA}	Latch Data Hold Time Using Product Term Clock		4		4		5		8		ns
t_{GOA}	Product Term Gate to Output			11		13		16		19	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		4		5		6		9		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		6		7		8		10		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output		6			7.5		10		11	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		5		6		6		ns
t_{ICO}	Input Register Clock to Combinatorial Output			14		15.5		18		20	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	7		8		9		15		
		T-type	8		9		10		16		
t_{WICL}	Input Register Clock Width	LOW	4.5		5		6		6		ns
t_{WICH}		HIGH	4.5		5		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	110		100		83.3		83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			12		14		16		20	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			14		16		18		22	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		4		14		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		9		16		ns
t_{WIGL}	Input Latch Gate Width LOW		5		5		6		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			12		14		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			12		14		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		8		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	9.5	2	10	2	12	2	15	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			10		12		14		17	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns
t_{HIR}	Input Register Hold Time		3		3		3		4		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	3		3		3		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	7		8		9		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		12		14		16		19	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		16		18		20		23	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	11		13		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	12		15		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		18		20		22		25	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +100°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +4.5 V

DC Input Voltage . . . . . –0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = 0°C to +70°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . .0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
V_{OL}	Output LOW Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA
I_{CC}	Supply Current	All PAL Blocks low-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			70		mA
		All PAL Blocks full-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			120		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	7.5	3	10	3	12	3	15	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	3.5		4		5		8		ns
				T-type	4.5		5		6		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				3.5		4		5		8		ns
t_{COA}	Product Term Clock to Output				4		4	12	4	14	4	18	ns
t_{WLA}	Product Term, Clock Width			LOW	4		5		8		9		ns
t_{WHA}				HIGH	4		5		8		9		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	74.0		62.5		52.6		38.5		MHz
				T-type	71.4		58.8		50.0		37		MHz
		Internal Feedback (f_{CNTA})		D-type	90.9		71.4		58.8		47.6		MHz
				T-type	83.3		66.7		55.6		45.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		125		100		62.5		55.6		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	5.5		6		7		10		ns
				T-type	6.5		7		8		11		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	5.5	2	6.5	2	8	2	10	ns
t_{WLS}	Global Clock Width			LOW	3		5		6		6		ns
t_{WHS}				HIGH	3		5		6		6		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	90		80		66.7		50		MHz
				T-type	83.3		74.1		62.5		47.6		MHz
		Internal Feedback (f_{CNTS})		D-type	133		100		83.3		66.6		MHz
				T-type	117		90.9		76.9		62.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		166.7		100		83.3		88.3		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		4		5		8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				4		4		5		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		-7		-10		-12		-15		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{GOA}	Product Term Gate to Output			11		13		16		19	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		4		5		6		9		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		6		7		8		10		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output		6			7.5		10		11	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		5		6		6		ns
t_{ICO}	Input Register Clock to Combinatorial Output		14			15.5		18		20	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	7		8		9		15		
		T-type	8		9		10		16		
t_{WICL}	Input Register Clock Width	LOW	4.5		5		6		6		ns
t_{WICH}		HIGH	4.5		5		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	110		100		83.3		83.3		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			12		14		16		20	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			14		16		18		22	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		4		14		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		9		16		ns
t_{WIGL}	Input Latch Gate Width LOW		5		5		6		6		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			12		14		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			12		14		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		8		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	9.5	2	10	2	12	2	15	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			10		12		14		17	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns
t_{HIR}	Input Register Hold Time		3		3		3		4		ns
t_{SIL}	Input Latch Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIL}	Input Latch Hold Time	3		3		3		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	7		8		9		12		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches	12			14		16		19	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		16		18		20		23	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	11		13		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	12		15		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		18		20		22		25	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +100°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = –40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	All PAL Blocks low-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		70		mA
		All PAL Blocks full-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f = 1 MHz, T_A = 25°C (Note 5)		120		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-10		-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	10	3	12	3	14	3	18	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	4		5		8		10		ns
				T-type	5		6		9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				4		5		8		10		ns
t_{COA}	Product Term Clock to Output				4	12	4	14	4	18	4	20	ns
t_{WLA}	Product Term, Clock Width			LOW	5		8		9		10		ns
t_{WHA}				HIGH	5		8		9		10		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	62.5		52.6		38.5		33.3		MHz
				T-type	58.8		50.0		37		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	71.4		58.8		47.6		35.7		MHz
				T-type	66.7		55.6		45.4		34.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		100		62.5		55.6		50.0		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	6		7		10		12		ns
				T-type	7		8		11		13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	6.5	2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	5		6		6		7		ns
t_{WHS}				HIGH	5		6		6		7		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	80		66.7		50		41.7		MHz
				T-type	74.1		62.5		47.6		40.0		MHz
		Internal Feedback (f_{CNTS})		D-type	100		83.3		66.6		58.8		MHz
				T-type	90.9		76.9		62.5		55.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		100		83.3		88.3		71.4		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		5		8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				4		5		8		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		-10		-12		-14		-18		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{GOA}	Product Term Gate to Output			13		16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		9		11		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		7		8		10		12		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output			7.5		10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		6		7		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15.5		18		20		22	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	8		9		15		17		
		T-type	9		10		16		18		
t_{WICL}	Input Register Clock Width	LOW	5		6		6		7		ns
t_{WICH}		HIGH	5		6		6		7		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	100		83.3		83.3		71.4		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			14		16		20		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			16		18		22		24	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		14		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		16		18		ns
t_{WIGL}	Input Latch Gate Width LOW		5		6		6		7		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			14		16		20		22	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		12		15		17		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		10		15		17		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			14		16		20		22	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		12		15		17		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		15		17		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	10	2	12	2	15	2	17	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	10	2	12	2	15	2	17	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			12		14		17		20	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns
t_{HIR}	Input Register Hold Time		3		3		4		4		ns
t_{SIL}	Input Latch Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description	-10		-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIL}	Input Latch Hold Time	3		3		4		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	8		9		12		15		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		19		22	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		18		20		23		26	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	13		16		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	15		18		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		20		22		25		27	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –55°C to +100°C

Supply Voltage
with Respect to Ground . . . . . –0.5 V to +4.5 V

DC Input Voltage . . . . . –0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = –40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . .–40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
V_{OL}	Output LOW Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA
I_{CC}	Supply Current	All PAL Blocks low-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			70		mA
		All PAL Blocks full-power V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 3.3 V, f = 1 MHz, T_A = 25°C (Note 4)			120		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*
4. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-10		-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				3	10	3	12	3	14	3	18	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	4		5		8		10		ns
				T-type	5		6		9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				4		5		8		10		ns
t_{COA}	Product Term Clock to Output				4	12	4	14	4	18	4	20	ns
t_{WLA}	Product Term, Clock Width			LOW	5		8		9		10		ns
t_{WHA}				HIGH	5		8		9		10		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	62.5		52.6		38.5		33.3		MHz
				T-type	58.8		50.0		37		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	71.4		58.8		47.6		35.7		MHz
				T-type	66.7		55.6		45.4		34.4		MHz
		No Feedback (Note 3)	$1/(t_{WLA} + t_{WHA})$		100		62.5		55.6		50.0		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	6		7		10		12		ns
				T-type	7		8		11		13		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		0		ns
t_{COS}	Global Clock to Output				2	6.5	2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	5		6		6		7		ns
t_{WHS}				HIGH	5		6		6		7		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 2)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	80		66.7		50		41.7		MHz
				T-type	74.1		62.5		47.6		40.0		MHz
		Internal Feedback (f_{CNTS})		D-type	100		83.3		66.6		58.8		MHz
				T-type	90.9		76.9		62.5		55.5		MHz
		No Feedback (Note 3)	$1/(t_{WLS} + t_{WHS})$		100		83.3		88.3		71.4		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				4		5		8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				4		5		8		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		-10		-12		-14		-18		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{GOA}	Product Term Gate to Output			13		16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		9		11		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		7		8		10		12		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		0		ns
t_{GOS}	Gate to Output			7.5		10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		5		6		6		7		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15.5		18		20		22	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	8		9		15		17		
		T-type	9		10		16		18		
t_{WICL}	Input Register Clock Width	LOW	5		6		6		7		ns
t_{WICH}		HIGH	5		6		6		7		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	100		83.3		83.3		71.4		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			14		16		20		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			16		18		22		24	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		4		4		14		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		9		16		18		ns
t_{WIGL}	Input Latch Gate Width LOW		5		6		6		7		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			14		16		20		22	ns
t_{ARW}	Asynchronous Reset Width (Note 2)		10		12		15		17		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 2)		8		10		15		17		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			14		16		20		22	ns
t_{APW}	Asynchronous Preset Width (Note 2)		10		12		15		17		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 2)		8		8		15		17		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		2	10	2	12	2	15	2	17	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		2	10	2	12	2	15	2	17	ns
Input Register with Standard-Hold-Time Option											
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			12		14		17		20	ns
t_{SIR}	Input Register Setup Time		2		2		2		2		ns
t_{HIR}	Input Register Hold Time		3		3		4		4		ns
t_{SIL}	Input Latch Setup Time		2		2		2		2		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description	-10		-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIL}	Input Latch Hold Time	3		3		4		4		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		4		4		4		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	8		9		12		15		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		16		19		22	ns
Input Register with Zero-Hold-Time Option										
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		18		20		23		26	ns
t_{SIR}^{I}	Input Register Setup Time	6		6		6		6		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		6		6		6		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	13		16		16		16		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	15		18		18		18		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		20		22		25		27	ns
Power-Down Mode and Slow Slew Rate Option										
t_{LP}	Power-down mode delay adder. For macrocells in a power-down mode PAL block, this parameter must be added to: t_{PD}, t_{COA}, t_{SS}, t_{GOA}, t_{SLS}, t_{ICO}, t_{ICS}, t_{IGO}, t_{IGOL}, t_{IGSS}, t_{AR}, t_{ARR}, t_{AP}, t_{APR}, t_{EA}, t_{ER}, t_{PDL}, t_{SLLS}, t_{PDLL}		2.5		2.5		2.5		2.5	ns
t_{SLW}	Slow slew rate delay adder. For an output configured with slow slew rate option, this parameter must be added to: t_{PD}, t_{COA}, t_{COS}, t_{GOA}, t_{GOS}, t_{ICO}, t_{IGO}, t_{IGOL}, t_{AP}, t_{AR}, t_{PDL}, t_{PDLL}		2.5		2.5		2.5		2.5	ns

Notes:

1. *See Switching Test Circuit for test conditions.*
2. *These parameters are not 100% tested, but are evaluated at initial characterization.*
3. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

TYPICAL THERMAL CHARACTERISTICS

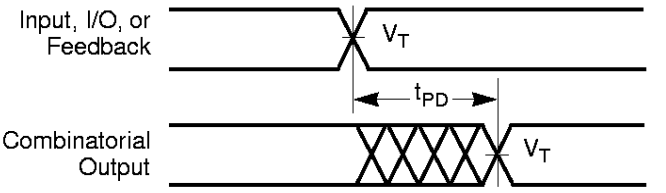
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Type		Unit
			PQFP	TQFP	
θ_{jc}	Thermal impedance, junction to case		7	7	°C/W
θ_{ja}	Thermal impedance, junction to ambient		43	48	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	36	38	°C/W
		400 lfpm air	32	33	°C/W
		600 lfpm air	30	30	°C/W
		800 lfpm air	28	25	°C/W

Plastic θjc Considerations

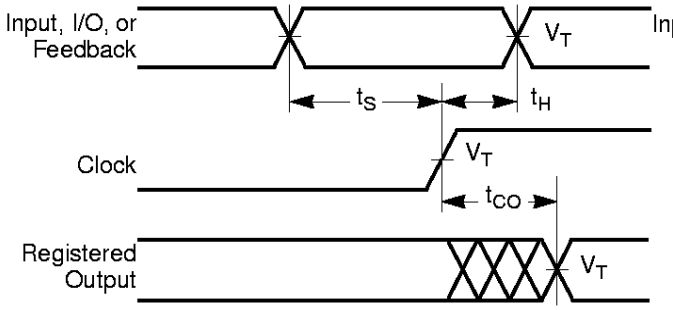
The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

SWITCHING WAVEFORMS



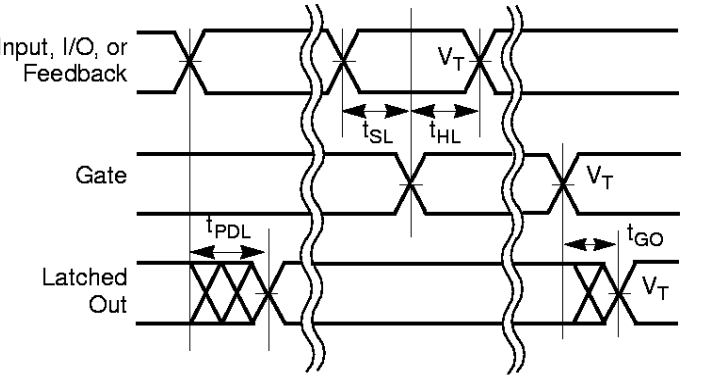
21443A-3

Combinatorial Output



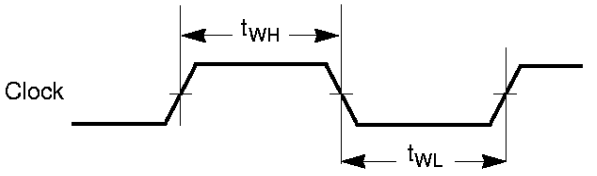
21443A-4

Registered Output



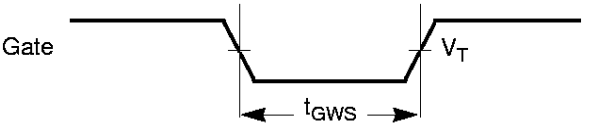
21443A-5

Latched Output



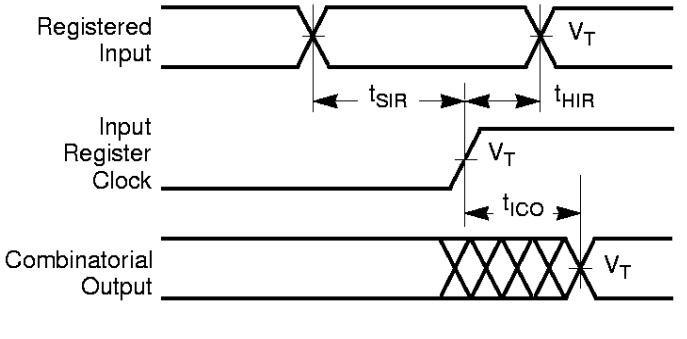
21443A-6

Clock Width



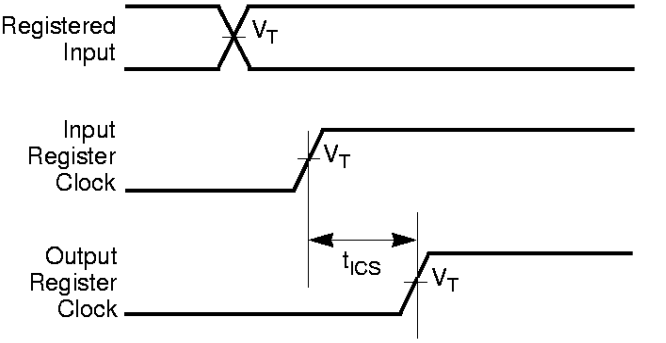
21443A-7

Gate Width



21443A-8

Registered Input



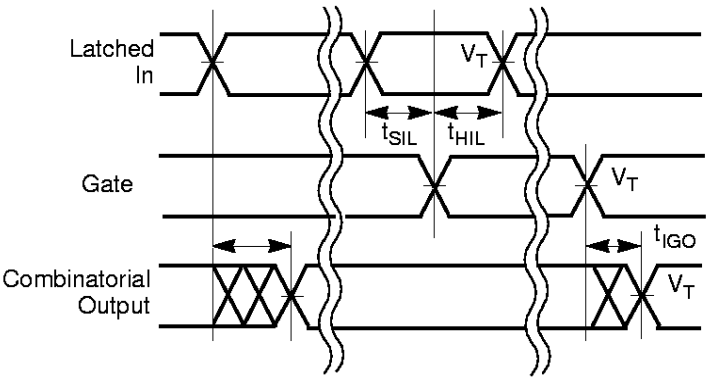
21443A-9

Input Register to Output Register Setup

Notes:

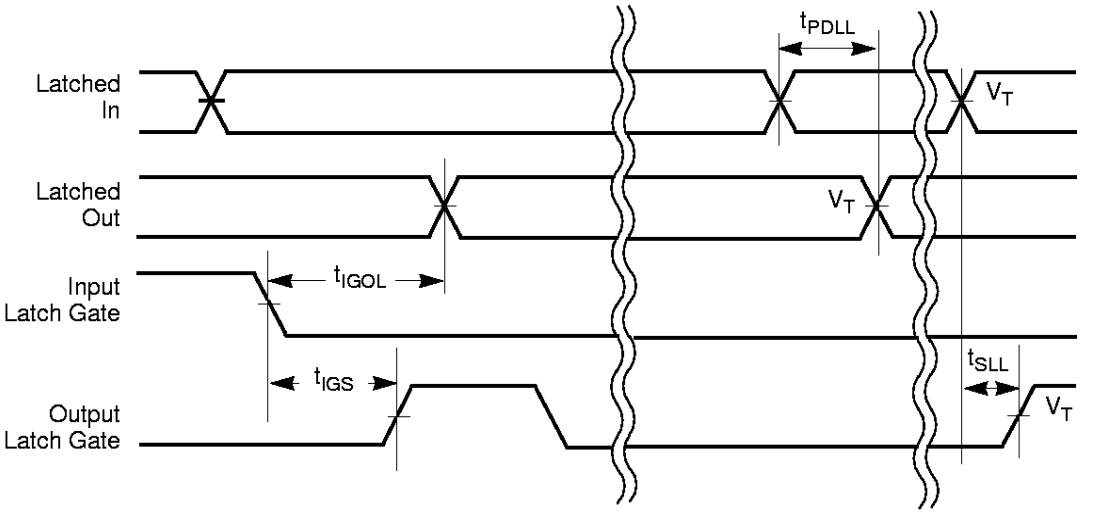
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



21443A-10

Latched Input



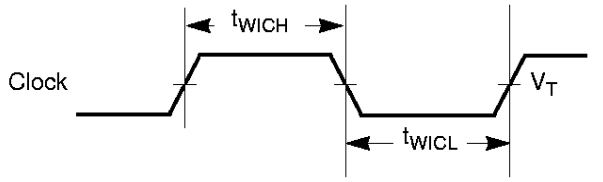
21443A-11

Latched Input and Output

Notes:

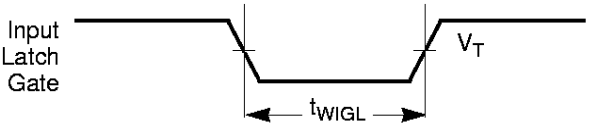
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



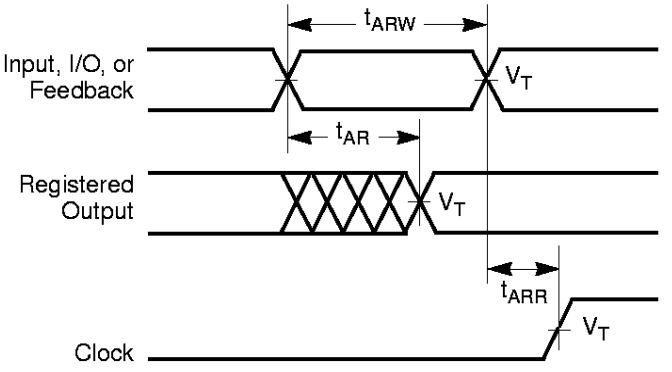
21443A-12

Input Register Clock Width



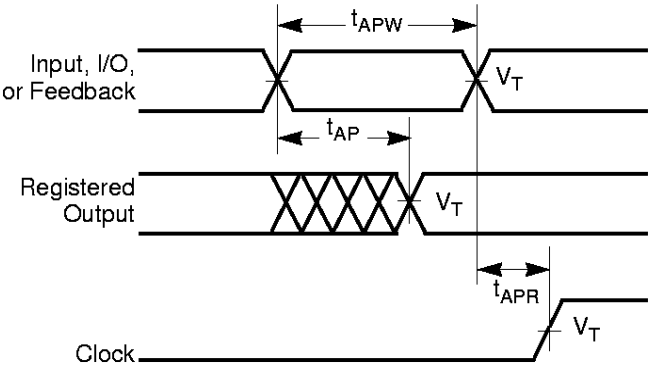
21443A-13

Input Latch Gate Width



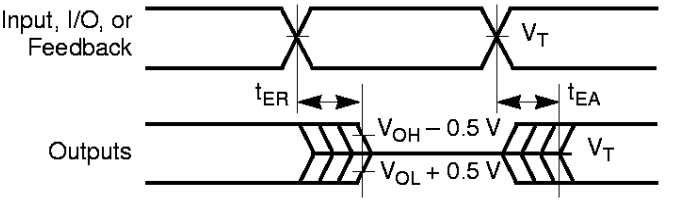
21443A-14

Asynchronous Reset



21443A-15

Asynchronous Preset



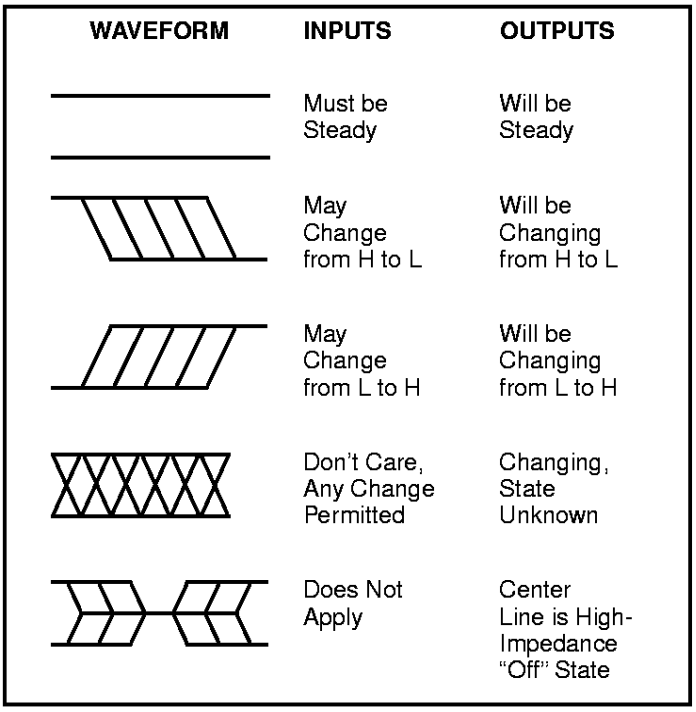
21443A-16

Output Disable/Enable

Notes:

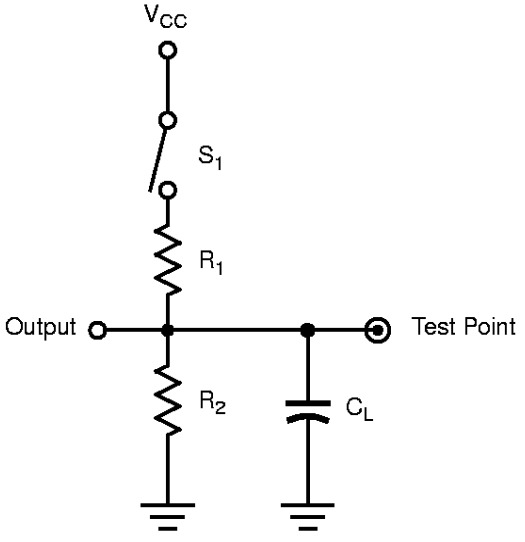
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



21443A-17

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF (30 pF)	300 Ω (1.6 KΩ)	390 Ω (1.6 KΩ)	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

Values in parentheses are for 3.3-V devices.

** Switching several outputs simultaneously should be avoided for accurate measurement.*

F_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

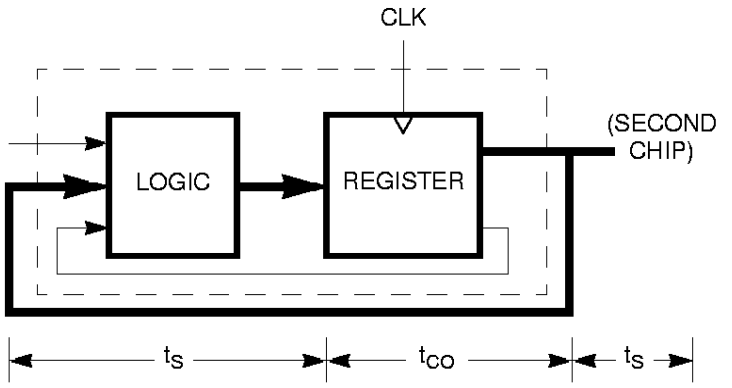
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f_{CNT}."

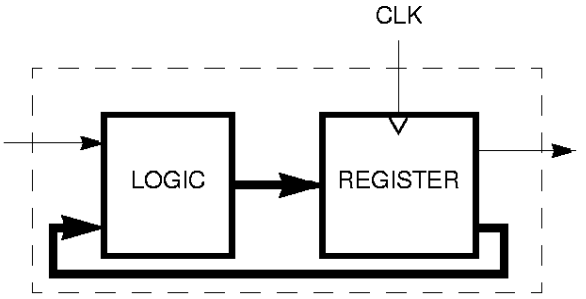
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

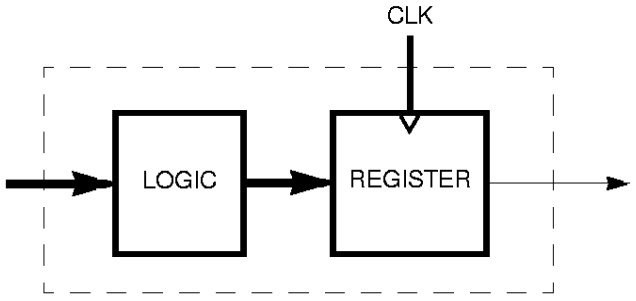
All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



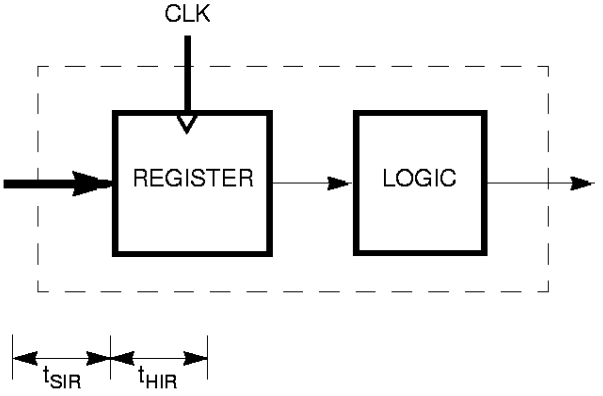
f_{MAX} External; $1/(t_S + t_{CO})$



f_{MAX} Internal (f_{CNT})



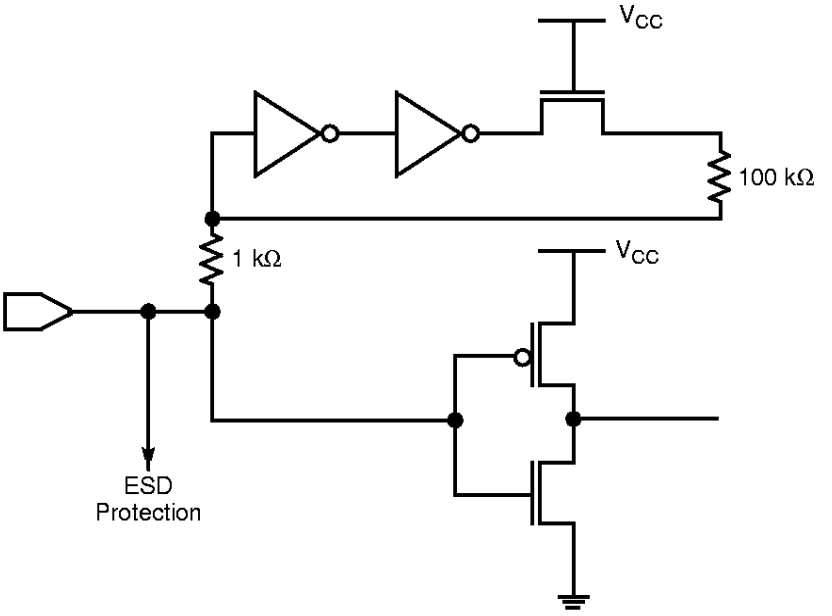
f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$



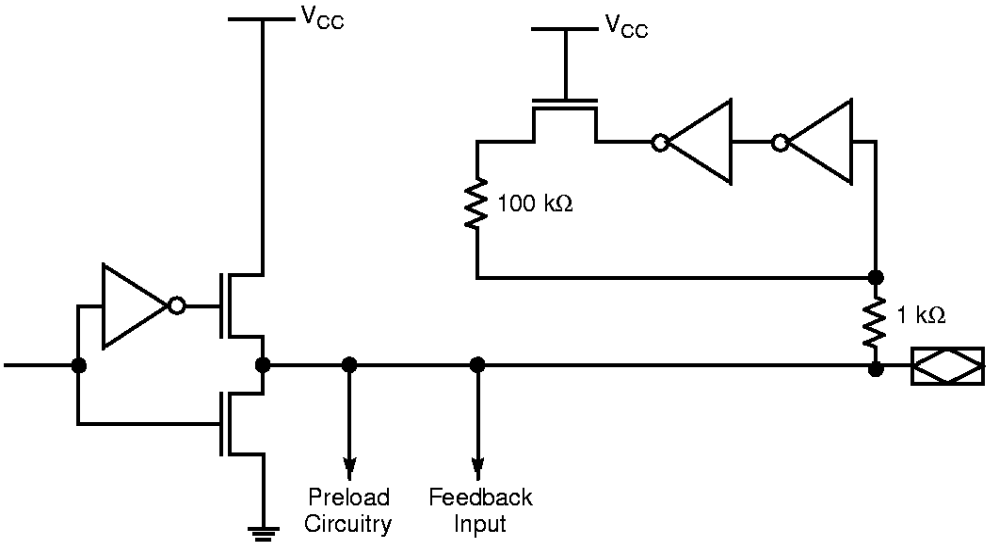
f_{MAXIR}; $1/(t_{SIR} + t_{HIR})$ or $1/(t_{WICL} + t_{WICH})$

21443A-18

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



I/O

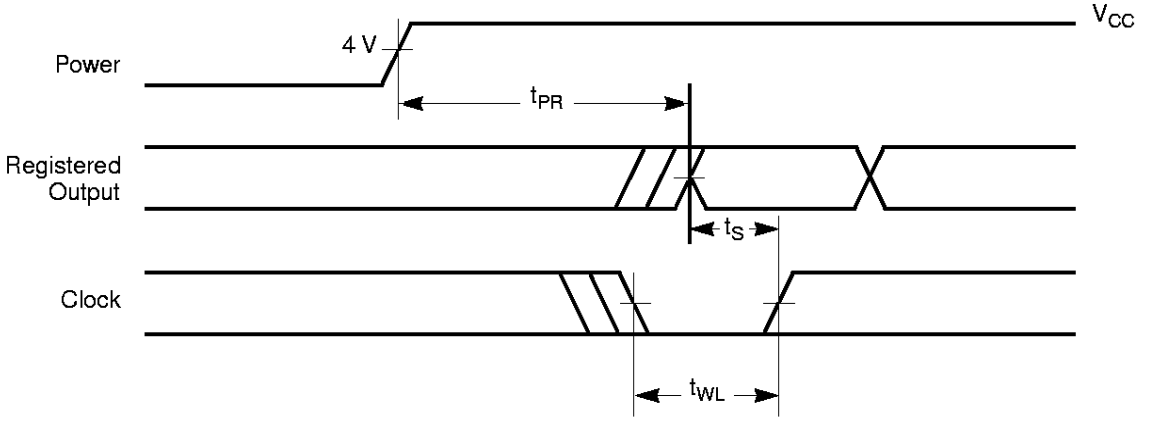
21443A-19

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



21443A-20

Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the Vantis FusionPLD Catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHXL Software
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	Vantis-ABEL Software Vantis-Synario Software
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	PLD Designer Verilog-XL, LeapFrog
Synario® Design Automation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Synario™ Software
ISDATA GmbH Daimlerstr. 51 D-76185 Karlsruhe, Germany (721) 75 10 87	LOG/iC2 LOG/iC Classic
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	SmartModel® Library
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	PLDSynthesis™ II AutologicII Synthesizer, QuickSim Simulator, QuickHDL Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	MicroSim DesignLab PLogic, PLSyn
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner-XL™ Software
SUSIE-CAD 10000 Nevada Highway, Suite 201 Boulder City, NV 89005 (702) 293-2271	SUSIE™ Simulator
Synopsys 700 E. Middlefield Rd. Mountain View, CA 94040	Design Compiler (Requires MINC PLDesigner-XL™) VSS Simulator

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (508) 480-0881	ViewPLD PureSpeed Simulator, ViewSim Simulator, VCS Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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APPROVED PROGRAMMERS (subject to change)

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MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 940 86 (408) 243-7000	Pilot-U84 MVP
BP Microsystems 1000 N. Post Oak Rd., Suite 225 Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600	BP1200 BP1400 BP2100 BP2200
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite™ Model 2900 Model 3900 AutoSite
Hi-Lo Systems 4F, No. 2, Sec. 5, Ming Shoh E. Road Taipei, Taiwan 2-764-0215 or Tribal Microsystems / Hi-Lo Systems 44388 South Grimmer Blvd. Fremont, CA 94538 (510) 623-8859	ALL-07 FLEX-700
SMS GmbH Im Grund 15 88239 Wangen Germany (49) 7522-97280	Sprint Expert Sprint Optima Multisite
Stag House Silver Court Watchmead, Welwyn Garden City Herfordshire UK AL7 1LT 707-332148	Stag Quazar Stag Eclipse
System General 1603A South Main Street Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Road, Shin Diau Taipei, Taiwan 2-917-3005	Turpro-1 Turpro-1/FX Turpro-1/TX

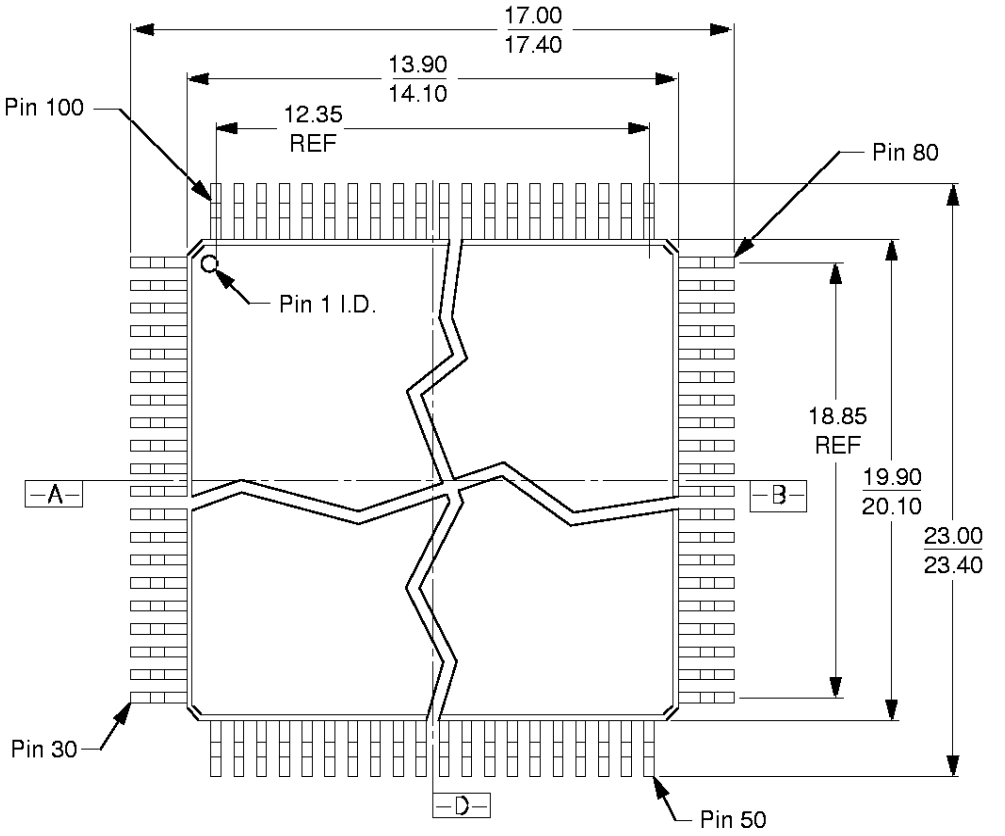
APPROVED ON-BOARD PROGRAMMERS

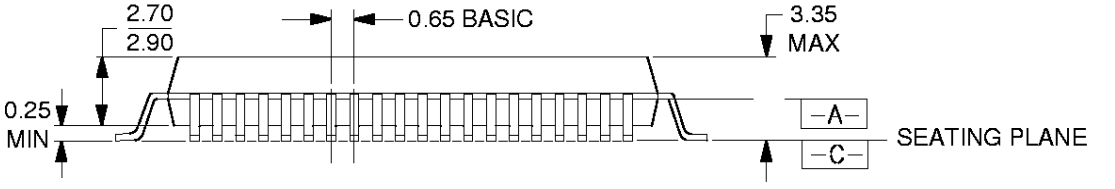
MANUFACTURER	PROGRAMMER CONFIGURATION
Corelis, Inc. 12607 Hidden Creek Way, Suite H Cerritos, California 70703 (310) 926-6727	JTAG PROG
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHPRO

PHYSICAL DIMENSIONS

PQR100

100-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



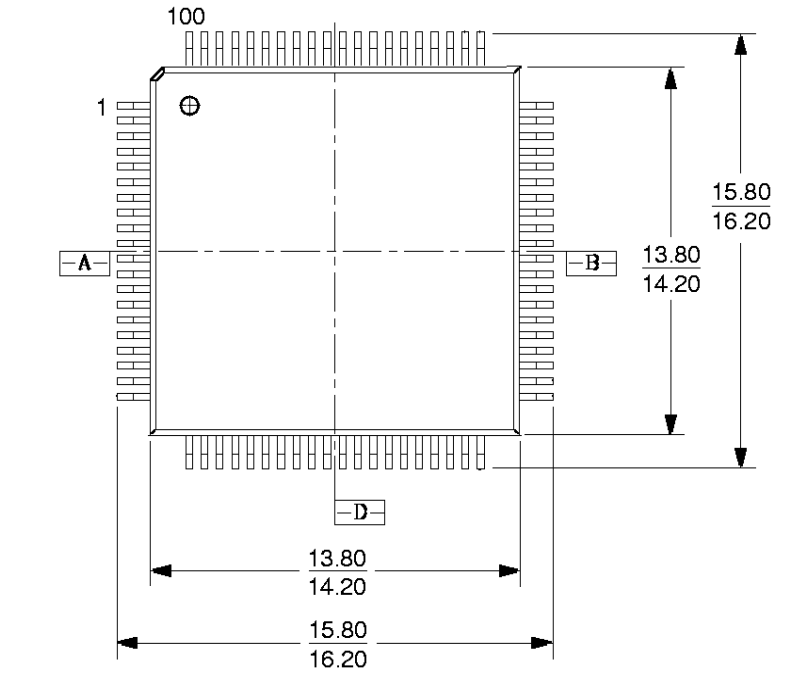


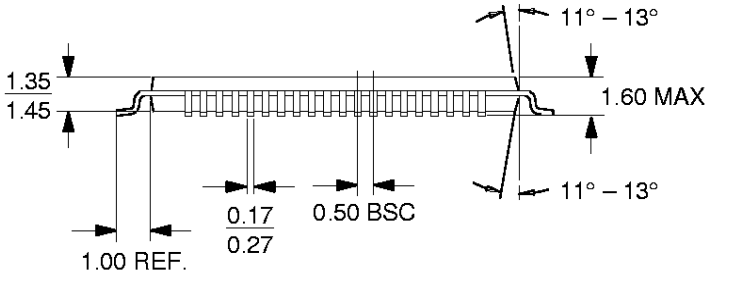
16-038-PQR-1_AH
PQR100
DP92
6-20-96 lv

PHYSICAL DIMENSIONS

PQL100

100-Pin Thin Quad Flat Pack; Trimmed and Formed (measured in millimeters)





16-038-PQT-2_AI
PQL100
9.3.96 lv