FDN306P

General Description

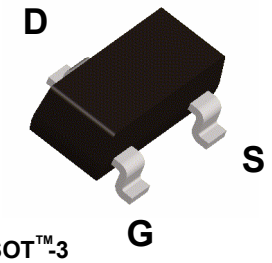
This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

Applications

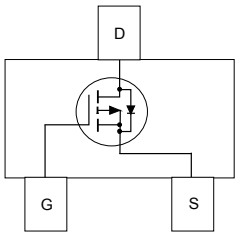
- Battery management
- Load switch
- Battery protection

Features

- –2.6 A, –12 V. $R_{DS(ON)}$ = 40 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 50 mΩ @ V_{GS} = –2.5 V
  $R_{DS(ON)}$ = 80 mΩ @ V_{GS} = –1.8 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- SuperSOT™ -3 provides low $R_{DS(ON)}$ and 30% higher power handling capability than SOT23 in the same footprint



SuperSOT™-3



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–12	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current – Continuous	(Note 1a)	–2.6	A
	– Pulsed		–10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
306	FDN306P	7''	8mm	3000 units

FDN306P

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 µA	–12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 µA,Referenced to 25°C		–3		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –10 V, V_{GS} = 0 V			–1	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –8 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.4	–0.6	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA,Referenced to 25°C		2.5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –2.6 A V_{GS} = –2.5 V, I_D = –2.3 A V_{GS} = –1.8V, I_D = –1.8 A V_{GS} = –4.5 V, I_D = –2.6A , T_J=125°C		30 39 54 40	40 50 80 54	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–10			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –2.6 A		10		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –6 V, V_{GS} = 0 V, f = 1.0 MHz		1138		pF
C_{oss}	Output Capacitance			454		pF
C_{rss}	Reverse Transfer Capacitance			302		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –6 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn–On Rise Time			10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			38	61	ns
t_f	Turn–Off Fall Time			35	56	ns
Q_g	Total Gate Charge	V_{DS} = –6 V, I_D = –2.6 A, V_{GS} = –4.5 V		12	17	nC
Q_{gs}	Gate–Source Charge			2		nC
Q_{gd}	Gate–Drain Charge			3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–0.42	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –0.42 (Note 2)		–0.6	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.

b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%