Synchronous Buck PWM Controller

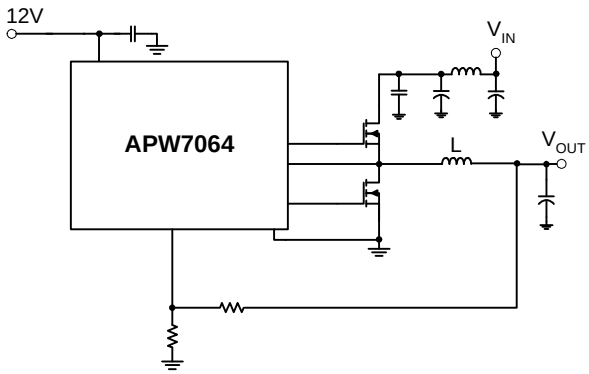
Features

- **Single 12V Power Supply Required**
- **Fast Transient Response**
  - 0~90% Duty Ratio
- **1.2V Reference with 1% Accuracy**
- **Shutdown Function by Controlling COMP Pin Voltage**
- **Internal Soft-Start (5.1ms) Function**
- **Voltage Mode PWM Control Design**
- **Under-Voltage Protection**
- **200kHz Fixed Switching Frequency**
- **SOP-8P Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Graphics Card**
- **Mother Board**
- **SMPS**

Typical Application Circuit



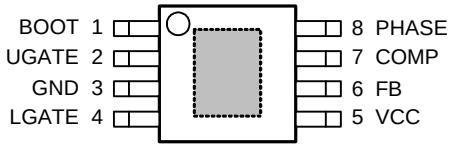
General Description

The APW7064 uses fixed 200kHz switching frequency, voltage mode, synchronous PWM controller which drives dual N-channel MOSFETs. The device integrates the control, monitoring and protection functions into a single package, provides one controlled power output with under-voltage protection.

The APW7064 provides excellent regulation for output load variation. The internal 1.2V temperature-compensated reference voltage is designed to meet the requirement of low output voltage applications. An built-in digital soft-start with fixed soft-start interval prevents the output voltage from overshoot as well as limiting the input current.

The APW7064 with excellent protection functions: POR and UVP. The Power-On-Reset (POR) circuit can monitor V_{CC} supply voltage exceeds its threshold voltage while the controller is running, and a built-in digital soft-start provides output with controlled voltage rise. The Under-Voltage Protection (UVP) monitors the voltage of FB pin for short-circuit protection. When the V_{FB} is less than 50% of V_{REF} (0.6V), the controller will shutdown the IC directly.

Pin Configuration



SOP-8P
APW7064

= Thermal Pad
(connected to GND plane for better heat dissipation)

Ordering and Marking Information

APW7064 □□□ – □□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code KA : SOP-8P Temperature Range E : -20 to 70 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7064 KA : APW7064 XXXXX	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC to GND	-0.3 to +16	V
V_{BOOT}	BOOT to PHASE	-0.3 to +16	V
V_{UGATE}	UGATE to PHASE <400ns pulse width >400ns pulse width	-5 to V_{BOOT} +5 -0.3 to V_{BOOT} +0.3	V
V_{LGATE}	LGATE to PGND <400ns pulse width >400ns pulse width	-5 to V_{CC}+5 -0.3 to V_{CC}+0.3	V
V_{PHASE}	PHASE to GND <200ns pulse width >200ns pulse width	-10 to +30 -2 to 16	V
V_{COMP}, V_{FB}	COMP, FB to GND	-0.3 to +7	
T_J	Junction Temperature Range	-20 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air SOP-8P	80	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage	10.8 to 13.2	V
V_{OUT}	Converter Output Voltage	1.2 to 5	V
V_{IN}	Converter Input Voltage	2.9 to 13.2	V

Recommended Operating Conditions (Cont.)

Symbol	Parameter	Rating	Unit
I_{OUT}	Converter Output Current	0 to 30	A
T_A	Ambient Temperature Range	-20 to 70	°C
T_J	Junction Temperature Range	-20 to 125	°C

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC} = 12V, and T_A =-20 ~ 70°C. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7064			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Nominal Supply Current	UGATE and LGATE Open	-	5	10	mA
	VCC Shutdown Supply Current	UGATE, LGATE = GND	-	1	2	mA
POWER-ON-RESET						
	Rising VCC Threshold		9	9.5	10	V
	Falling VCC Threshold		7.5	8	8.5	V
	COMP Shutdown Threshold		-	1.2	-	V
	COMP Shutdown Hysteresis		-	0.1	-	V
OSCILLATOR						
F_{OSC}	Free Running Frequency		170	200	230	kHz
ΔV_{OSC}	Ramp Amplitude		-	1.6	-	V_{P-P}
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Measured at FB Pin	-	1.2	-	V
	Accuracy	T_A =-20~70°C	-1.0	-	+1.0	%
ERROR AMPLIFIER						
Gain	Open Loop Gain	R_L=10k, C_L=10pF (Note 3)	-	88	-	dB
GBWP	Open Loop Bandwidth	R_L=10k, C_L=10pF (Note 3)	-	15	-	MHz
SR	Slew Rate	R_L=10k, C_L=10pF (Note 3)	-	6	-	V/µs
	FB Input Current	V_{FB} = 0.8V (Note 3)	-	0.1	1	µA
V_{COMP}	COMP High Voltage		-	5.5	-	V
V_{COMP}	COMP Low Voltage		-	0	-	V
I_{COMP}	COMP Source Current	V_{COMP}=2V	-	5	-	mA
I_{COMP}	COMP Sink Current	V_{COMP}=2V	-	5	-	mA
GATE DRIVERS						
I_{UGATE}	Upper Gate Source Current	V_{BOOT} = 12V, V_{UGATE} -V_{PHASE} = 2V	-	2.6	-	A
I_{UGATE}	Upper Gate Sink Current	V_{BOOT} = 12V, V_{UGATE} -V_{PHASE} = 2V	-	1.05	-	A
I_{LGATE}	Lower Gate Source Current	V_{CC} = 12V, V_{LGATE} = 2V	-	4.9	-	A
I_{LGATE}	Lower Gate Sink Current	V_{CC} = 12V, V_{LGATE} = 2V	-	1.4	-	A
R_{UGATE}	Upper Gate Source Impedance	V_{BOOT} = 12V, I_{UGATE} = 0.1A	-	2	3	Ω
R_{UGATE}	Upper Gate Sink Impedance	V_{BOOT} = 12V, I_{UGATE} = 0.1A	-	1.6	2.4	Ω
R_{LGATE}	Lower Gate Source Impedance	V_{CC} = 12V, I_{LGATE} = 0.1A	-	1.3	1.95	Ω

Electrical Characteristics (Cont.)

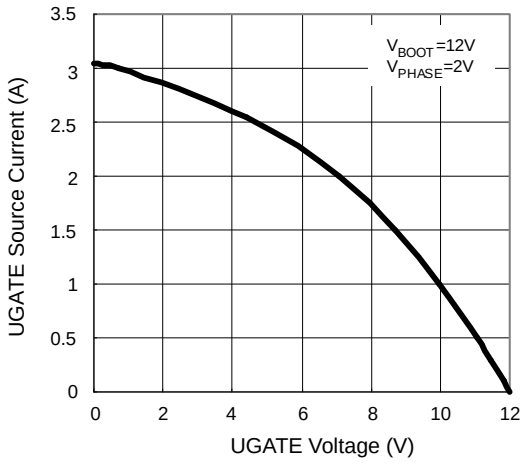
Unless otherwise specified, these specifications apply over V_{CC} = 12V, and T_A =-20 ~ 70°C. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7064			Unit
			Min.	Typ.	Max.	
GATE DRIVERS (CONT.)						
R_{LGATE}	Lower Gate Sink Impedance	V_{CC} = 12V, I_{LGATE} = 0.1A	-	1.25	1.88	Ω
T_D	Dead Time		-	20	-	ns
PROTECTIONS						
V_{UVP}	Under-Voltage Threshold Trip Point	Percent of V_{REF}	45	50	55	%
SOFT-START						
T_{SS}	Soft-Start Interval		4.4	5.1	6	ms

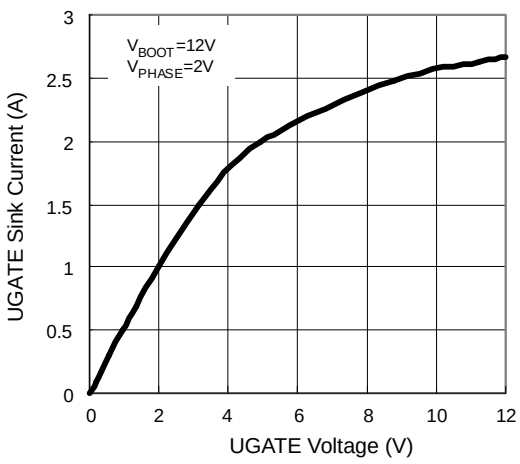
Note 3: Guaranteed by design.

Typical Operating Characteristics

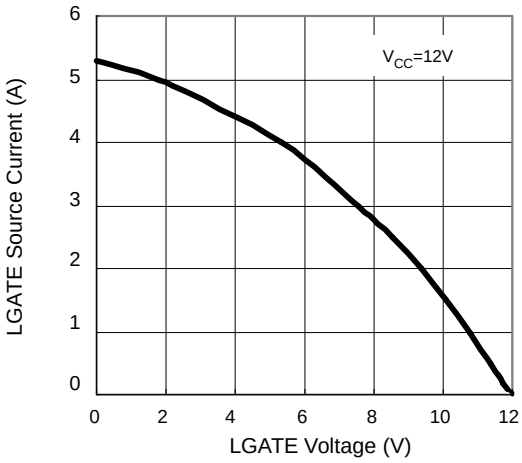
UGATE Source Current vs. UGATE Voltage



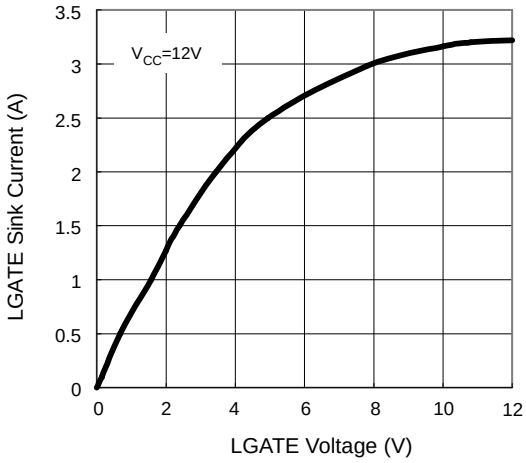
UGATE Sink Current vs. UGATE Voltage



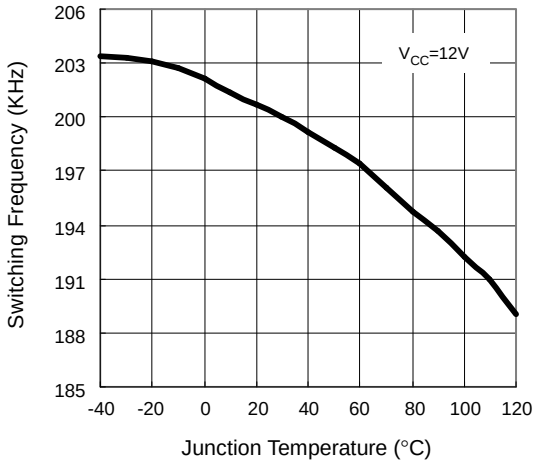
LGATE Source Current vs. LGATE Voltage



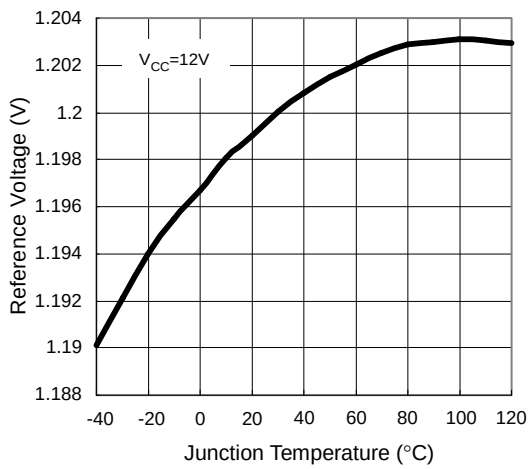
LGATE Sink Current vs. LGATE Voltage



Switching Frequency vs. Junction Temperature

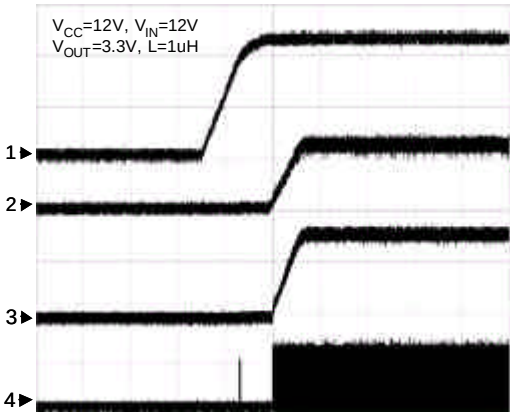


Reference Voltage vs. Junction Temperature



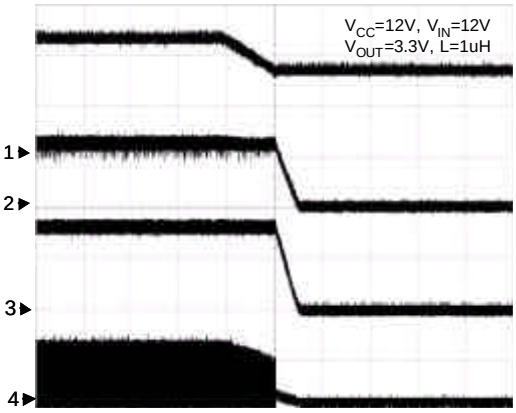
Operating Waveforms

Power On



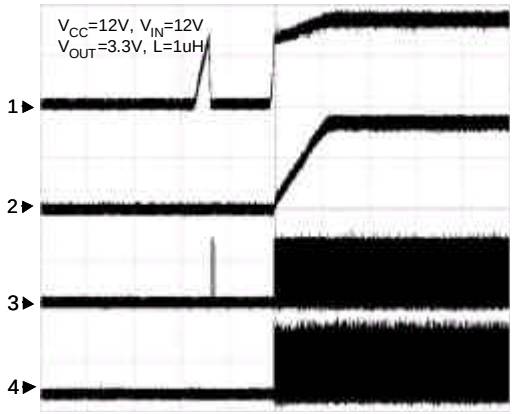
CH1: V_{CC} (5V/div)
CH2: V_{FB} (1V/div)
CH3: V_{OUT} (2V/div)
CH4: U_{GATE} (20Vdiv)
Time: 10ms/div

Power Off



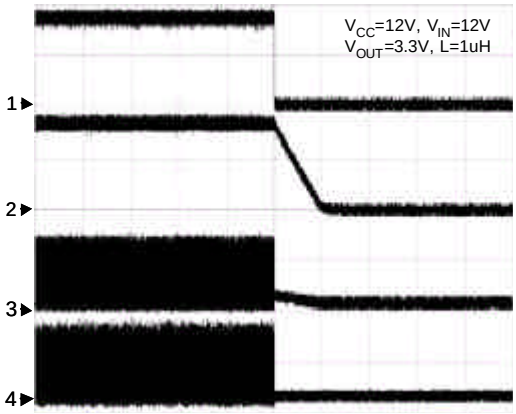
CH1: V_{CC} (5V/div)
CH2: V_{FB} (1V/div)
CH3: V_{OUT} (2V/div)
CH4: U_{GATE} (20Vdiv)
Time: 10ms/div

EN (EN=V_{CC})



CH1: V_{COMP} (1V/div)
CH2: V_{OUT} (2V/div)
CH3: U_{GATE} (20V/div)
CH4: L_{GATE} (10Vdiv)
Time: 5ms/div

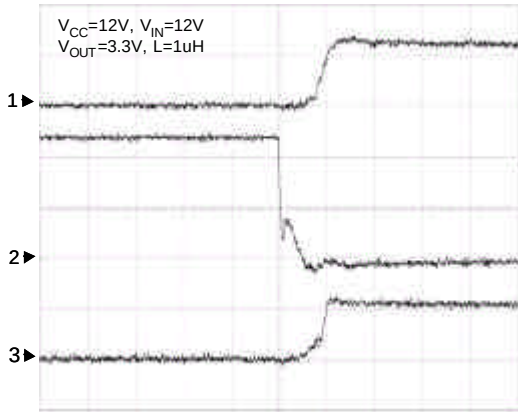
Shutdown (EN=GND)



CH1: V_{COMP} (1V/div)
CH2: V_{OUT} (2V/div)
CH3: U_{GATE} (20V/div)
CH4: L_{GATE} (10Vdiv)
Time: 5ms/div

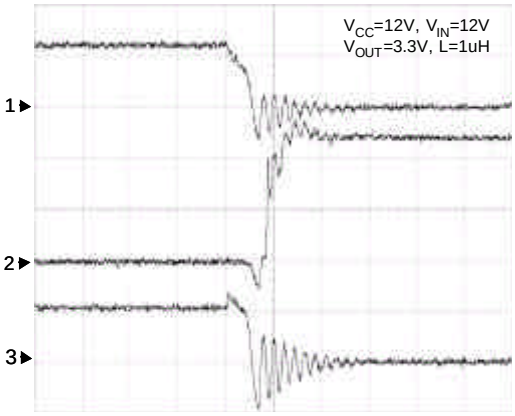
Operating Waveforms (Cont.)

UGATE Rising



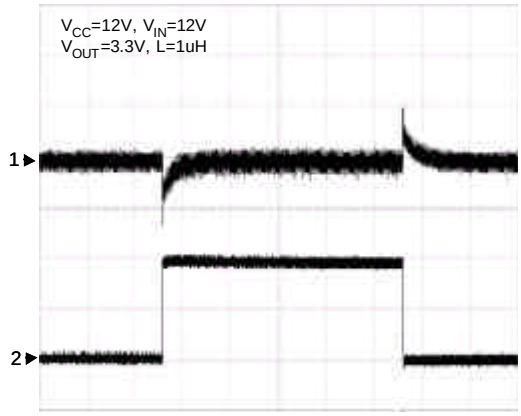
CH1: U_{GATE} (20V/div)
CH2: L_{GATE} (5V/div)
CH3: V_{PHASE} (10V/div)
Time: 50ns/div

UGATE Falling



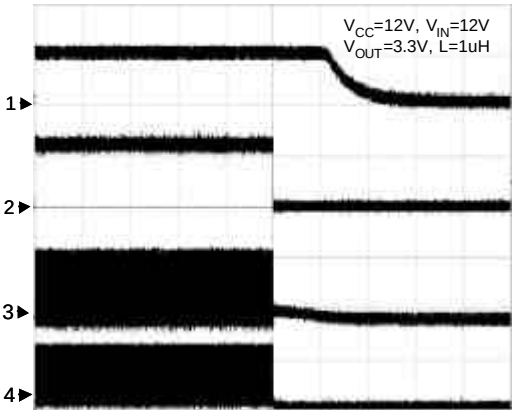
CH1: U_{GATE} (20V/div)
CH2: L_{GATE} (5V/div)
CH3: V_{PHASE} (10V/div)
Time: 50ns/div

Load Transient Response



CH1: V_{OUT} (200mV/div)
CH2: I_{OUT} (5A/div)
Time: 1ms/div

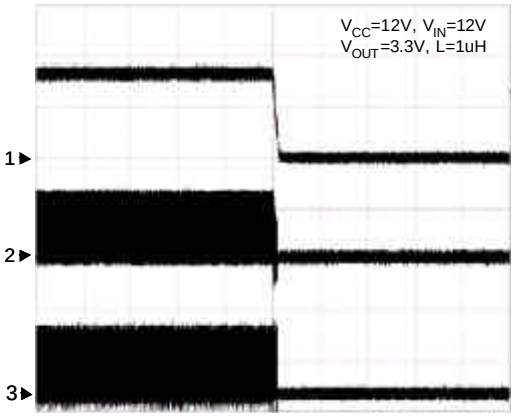
Under Voltage Protection



CH1: I_{OUT}(10A/div)
CH2: V_{FB} (1V/div)
CH3: U_{GATE} (20V/div)
CH4: L_{GATE}(10V/div)
Time: 1ms/div

Operating Waveforms (Cont.)

Short Test

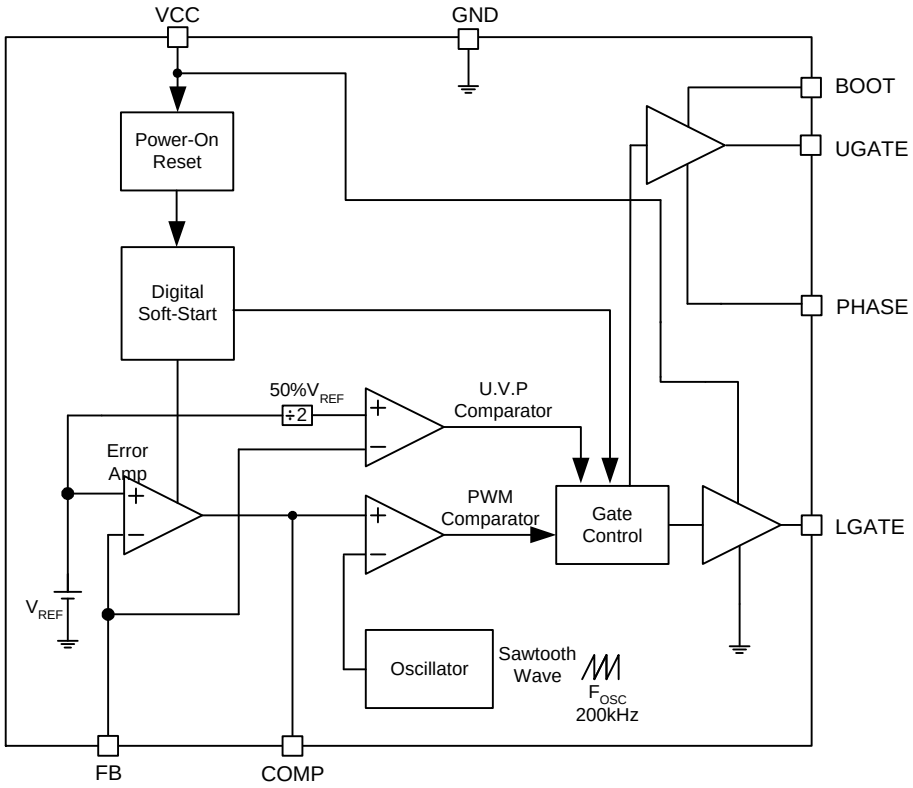


CH1: V_{OUT} (2V/div)
CH2: U_{GATE} (20V/div)
CH3: L_{GATE} (10V/div)
Time: 2ms/div

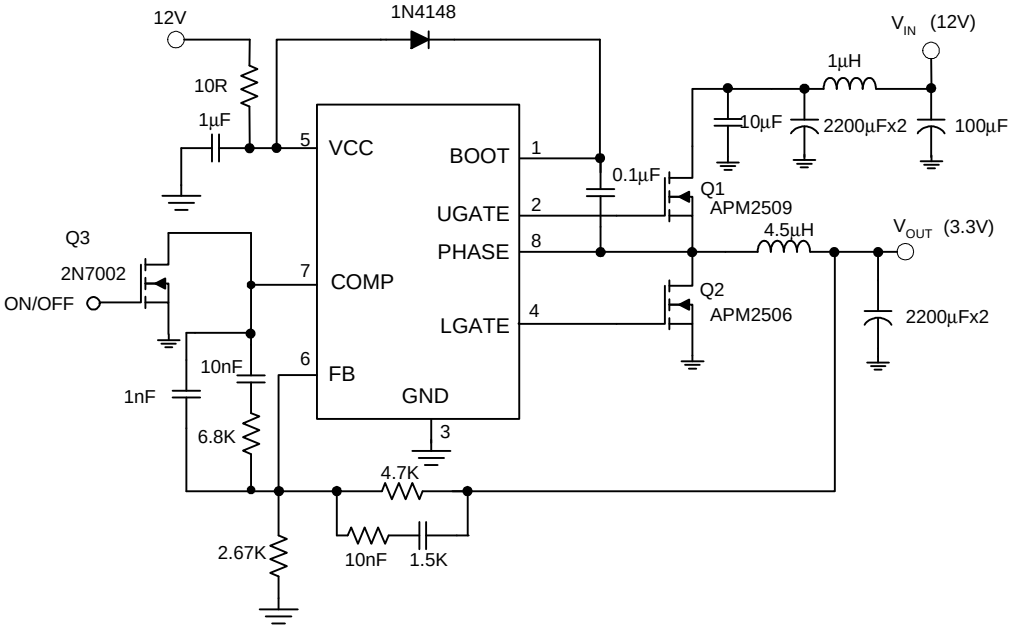
Pin Description

PIN		FUNCTION
NO.	NAME	
1	BOOT	A bootstrap circuit with a diode connected to VCC is used to create a voltage suitable to drive a logic-level N-channel MOSFET.
2	UGATE	Connect this pin to the high-side N-channel MOSFET gate. This pin provides gate drive for the high-side MOSFET.
3	GND	The GND terminal provides return path for the IC bias current and the low-side MOSFET driver pull-low current. Connect the pin to the system ground via very low impedance layout on PCBs.
4	LGATE	Connect this pin to the low-side N-channel MOSFET gate. This pin provides gate drive for the low-side MOSFET.
5	VCC	Connect this pin to a 12V supply voltage. This pin provides bias supply for the control circuitry and the low-side MOSFET driver. The voltage at this pin is monitored for the Power-On-Reset (POR) purpose. It is recommended that a decoupling capacitor (1 to 10μF) be connected to GND for noise decoupling.
6	FB	This pin is the inverting input of the internal error amplifier. Connect this pin to the output (V_{OUT}) of the converter via an external resistor divider for closed-loop operation. The output voltage set by the resistor divider is determined using the following formula: $V_{OUT} = 1.2 \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$ where R_{OUT} is the resistor connected from V_{OUT} to FB, and R_{GND} is the resistor connected from FB to GND. The FB pin is also monitored for under voltage events.
7	COMP	This pin is the output of PWM error amplifier. It is used to set the compensation components. In addition, if the pin is pulled below 1.2V, it will disable the device.
8	PHASE	This pin is the return path for the upper gate driver. Connect this pin to the upper MOSFET source.

Block Diagram



Typical Application Circuit



Function Description

Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7064 continually monitors the input supply voltage (V_{CC}) and the COMP pin. The supply voltage (V_{CC}) must exceed its rising POR threshold voltage. The POR function initiates soft-start operation after VCC and COMP voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{CC} are equivalent and the +12V power source must exceed the rising VCC threshold. The POR function inhibits operation at disabled status (V_{COMP} is less than 1.2V). With both input supplies above their POR thresholds, the device initiates a soft-start interval.

Soft-Start

The APW7064 has a built-in digital soft-start to control the output voltage rise and limit the current surge during the start-up. In Figure 1, when V_{CC} exceeds rising POR threshold voltage, it will delay 1024/Fosc seconds and then begin soft-start. During soft-start, an internal ramp connected to the one of the positive inputs of the Gm amplifier rises up from 0V to 2V to replace the reference voltage (1.2V) until the ramp voltage reaches the reference voltage. The soft-start interval is decided by the oscillator frequency (200kHz). The formulation is given by:

$$T_{delay} = t_2 - t_1 = 1024/F_{OSC} = 5.1ms$$

$$T_{soft-start} = t_3 - t_2 = 1024/F_{OSC} = 5.1ms$$

Figure 2. shows more detail of the FB voltage ramp. The FB voltage soft-start ramp is formed with many small steps of voltage. The voltage of one step is about 18.75mV in V_{FB}, and the period of one step is about $16/F_{OSC}$. This method provides a controlled voltage rise and prevents the large peak current to charge output capacitor.

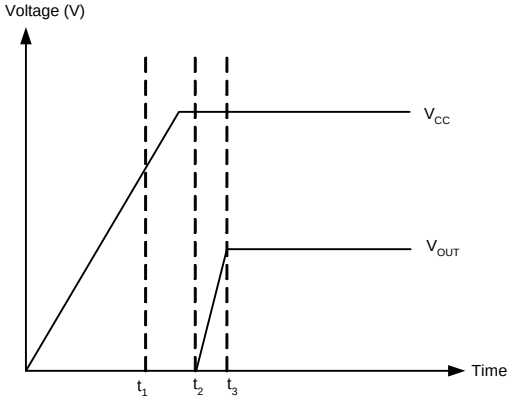


Figure 1.Soft-Start Interval

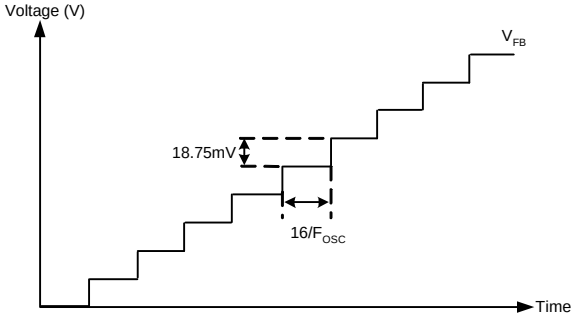


Figure 2.The Controlled Stepped FB Voltage During Soft-Start

Shutdown and Enable

Pulling the COMP voltage to GND by an open drain transistor, shown in typical application circuit, shutdown the APW7064 PWM controller. In shutdown mode, the UGATE and LGATE turn off and pull to PHASE and GND respectively.

Under Voltage Protection

The FB pin is monitored during converter operation by the internal Under Voltage (UV) comparator. If the FB voltage drops below 50% of the reference voltage (50% of 1.2V = 0.6V), a fault signal is internally generated, and the device turns off both high-side and low-side MOSFET and the converter's output is latched to be floating.

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 1.2V. The output voltage is determined by:

$$V_{OUT} = 1.2 \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

Where R_{OUT} is the resistor connected from V_{OUT} to FB and R_{GND} is the resistor connected from FB to GND.

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

where F_S is the switching frequency of the regulator.

Although increase of the inductor value reduces the ripple current and voltage, a tradeoff will exist between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be parallel to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1µF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. There are two components of loss in the MOSFETs: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following:

$$P_{UPPER} = I_{OUT}^2(1+T_C)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_S$$

$$P_{LOWER} = I_{OUT}^2(1+T_C)(R_{DS(ON)})(1-D)$$

Where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$
F_S is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFETs have conduction loss while the upper MOSFET include an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Application Information (Cont.)

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V_{OUT} should be added. The compensation network is shown in Figure 6. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1+s\times ESR\times C_{OUT}}{s^2\times L\times C_{OUT}+s\times ESR\times C_{OUT}+1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L\times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

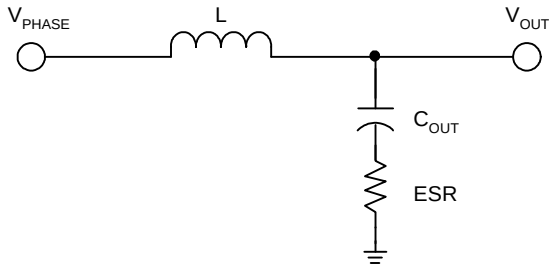


Figure 3. The Output LC Filter

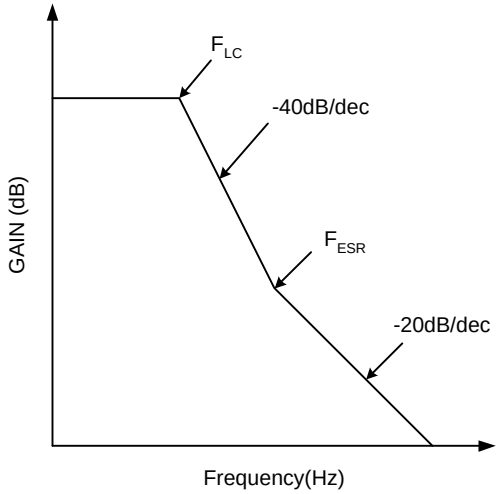


Figure 4. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 5. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

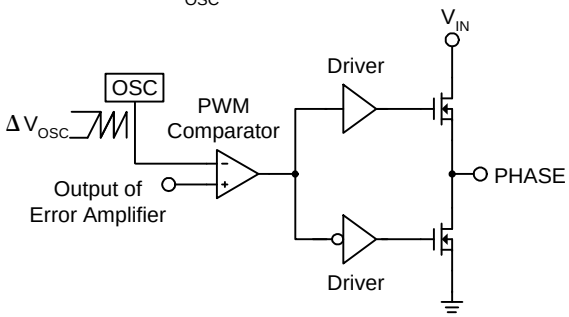


Figure 5. The PWM Modulator

The compensation network is shown in Figure 6. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1}//\left(R2+\frac{1}{sC2}\right)}{R1//\left(R3+\frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1\times R3\times C1}\times\frac{\left(s+\frac{1}{R2\times C2}\right)\times\left(s+\frac{1}{(R1+R3)\times C3}\right)}{s\left(s+\frac{C1+C2}{R2\times C1\times C2}\right)\times\left(s+\frac{1}{R3\times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

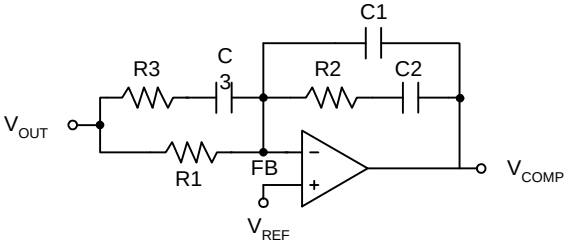


Figure 6. Compensation Network

Application Information (Cont.)

PWM Compensation (Cont.)

The closed loop gain of the converter can be written as:

$GAIN_{LC}$ X $GAIN_{PWM}$ X $GAIN_{AMP}$

Figure 7. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1.Choose a value for R1, usually between 1K and 5K.

2.Select the desired zero crossover frequency

F_O : (1/5 ~ 1/10) X F_S > F_O > F_{ESR}

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3.Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

F_{Z1} = 0.75 X F_{LC}

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4.Set the pole at the ESR zero frequency F_{ESR}:

F_{P1} = F_{ESR}

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5.Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

F_{P2} = 0.5 X F_S

F_{Z2} = F_{LC}

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

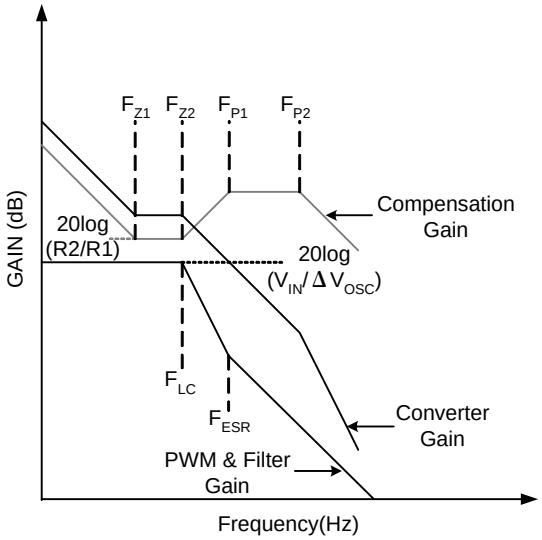


Figure 7. Converter Gain and Frequency

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 200kHz,the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short, wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Figure 8. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.

- The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.

- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.

- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).

- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.

- The drain of the MOSFETs (V_{IN} and PHASE nodes) should be a large plane for heat sinking.

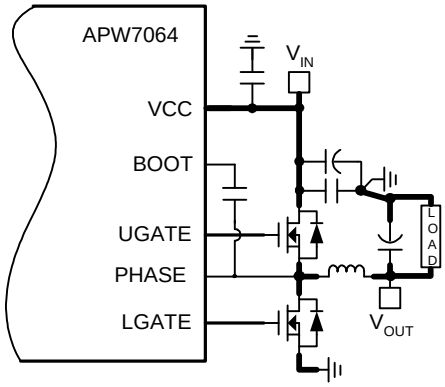
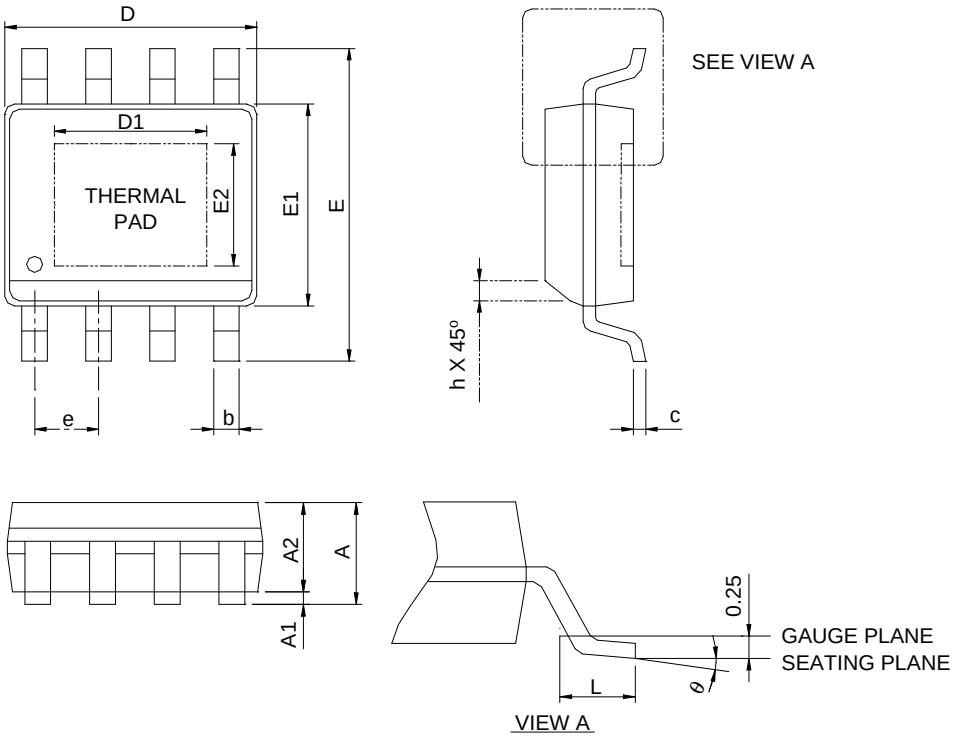


Figure 8. Layout Guidelines

Package Information

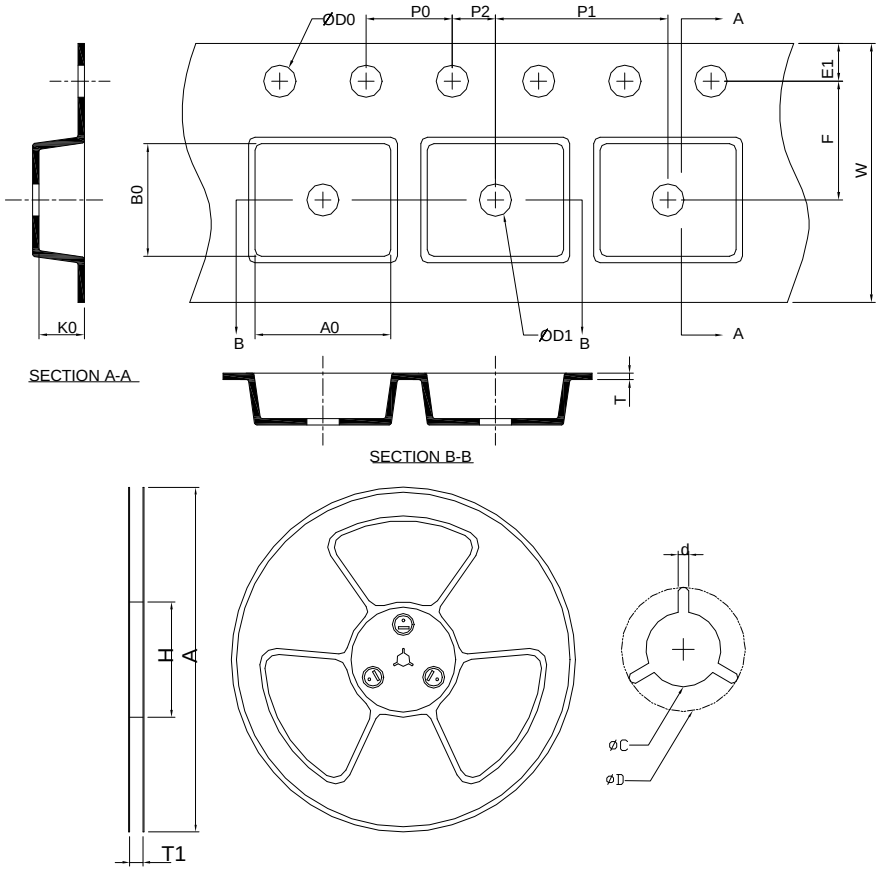
SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

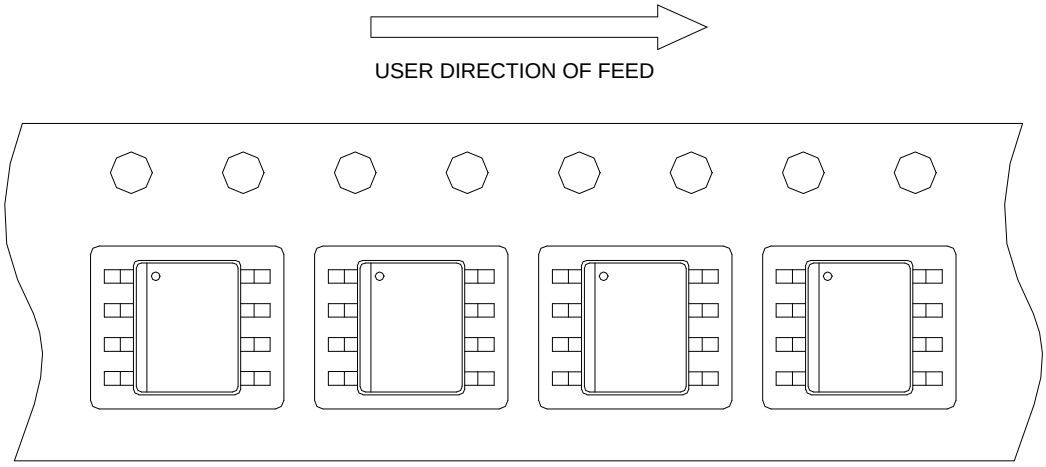
(mm)

Devices Per Unit

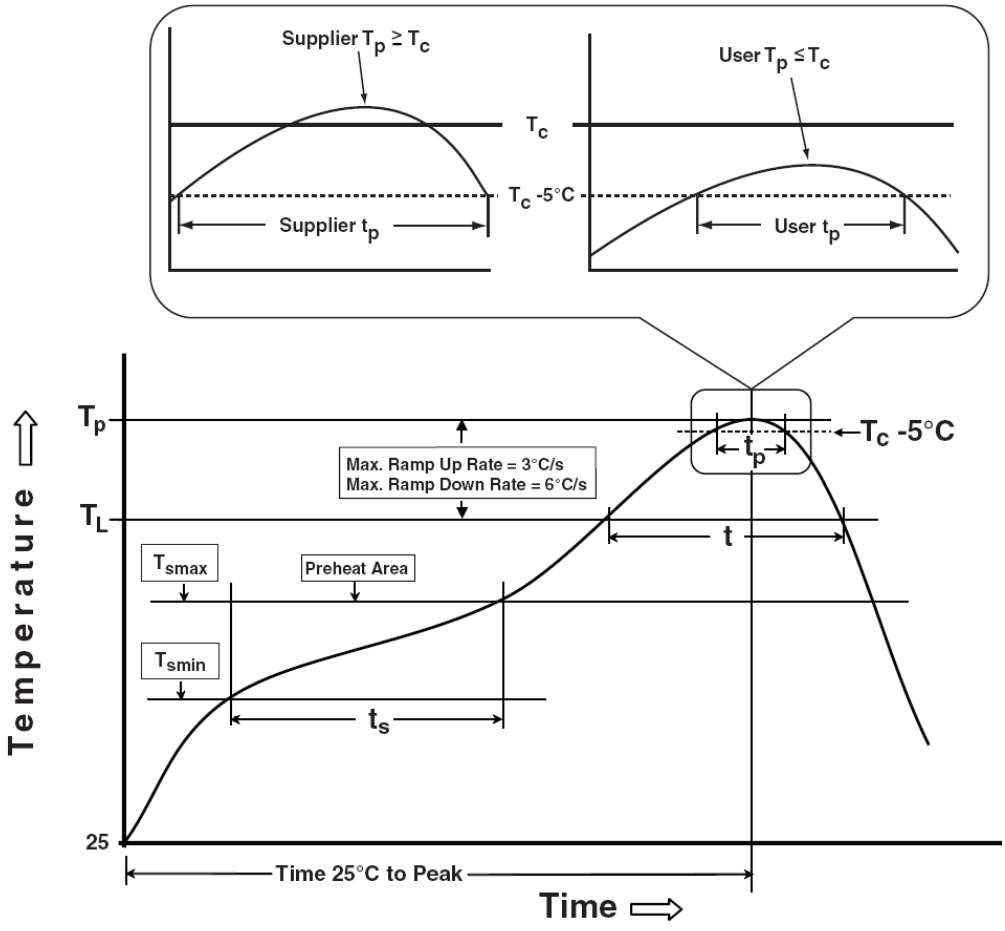
Package Type	Unit	Quantity
SOP-8P	Tape & Reel	2500

Taping Direction Information

SOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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