S1C33L15

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CMOS 32-bit Application Specific Controller

- 32-bit RISC CPU-Core Optimized for SoC (EPSON S1C33 PE) (Max. 90 MHz operation)
- 1KB Instruction Cache and 1KB Data Cache
- 100KB RAM (including cache and battery backup RAM)
- Programmable Operating Clock using PLL
  (division ratio: 1/1 to 1/16, multiplication rate: ×1 to ×16)
- Hardware Multimedia Accelerator (64-bit internal processing)
- Multifunctional Calculation Module
  (multiply and accumulation, matrix, and vector computations)
- I^2S Audio Interface with One Input and One Output Channel (supports 24-bit format)
- 16-ch. DMA Controller (triggered with peripheral circuits)
- SDRAM Controller with Burst Control
- Abundant Serial Interfaces (UART × 2ch., FSIO (serial I/F with FIFO, supports IrDA1.0) × 2ch., EFSIO(extended serial I/F with FIFO, supports ISO7816 mode/IrDA1.0) × 2ch., SPI × 4ch., DCSIO (I^2C bus master I/F emulator) × 4ch.)
- 4ch. of 16-bit PWM Control Timers with IGBT Control Function
- 4ch. of 8-bit programmable timers
- NAND Flash Interface
- Infrared Remote Controller
- 16M/64K-color TFT, 64K-color STN, and Monochrome STN LCD Controller
  Max. resolution by internal VRAM (80KB)
  : 320 × 240, 8 bpp (256 colors)
  Max. resolution by external memory
  : 640 × 480, 24 bpp (full color)
  Two-screen overlay display by Picture-in-Picture (PIP)

■ DESCRIPTIONS

The S1C33L15 is a high performance 32-bit controller with 16M/64K TFT/64K CSTN LCD controller and hardware arithmetic accelerator for multimedia applications. It is suitable for use in applications with an LCD panel and audio functions, such as electronic dictionaries, audio players, image viewers, and mobile equipment.
The S1C33L15 supports various small to middle-size LCD panels, not only 256-color QVGA display by using the 100KB internal memory but also full-color VGA display by using a large external memory. Also it has a hardware PIP function that overlays one image on another to lighten the load on the drawing process in the application. This makes it possible to simply create the LCD panel display routine. The hardware arithmetic accelerator and the I^2C interface for input/output can be used for decode processing of various audio formats. The on-chip interface modules, MMC controller, NAND Flash controller and SPI, can be used for image display or audio player applications using media cards. Furthermore, the abundant interfaces and remote controller are used to realize electronic equipment that supports various user interfaces.
The S1C33L15 not only operates as an LCD control processor on a standalone basis but also it can be used as an LCD controller by connecting it to an external host processor via the host processor interface (HIF).
The S1C33L15 is equipped with the 32-bit RISC CPU core C33, 2KB instruction/data caches, 100KB RAM, DMA controller, memory controller (SRAM/SDRAM), various timers, real-time clock and general-purpose I/O ports as its basic functions, so it can also be used as a high performance general-purpose CPU.
These S1C33L15 functions are implemented by EPSON SoC (System on Chip) design technology using 0.18 µm Multi-Vth. CMOS Process.

■ FEATURES

●Technology
- 0.18 µm AL-4-Layers Vth. Mixed CMOS process technology

●CPU
- EPSON original C33 PE 32-bit RISC CPU-Core with AMBA bus, optimized for SoC
- The maximum operating-clock frequency: 90 MHz
- Internal two-stage pipeline
- Instruction set: 125 instructions (16-bit fixed length)
- Cache: 1 KB of instruction cache + 1 KB of data cache
- Memory space
  - Up to 4 GB (32-bit address space) accessible

●Embedded Memory (RAM)
- 16 KB IRAM1
  Can be used as high-speed general-purpose RAM. 2 KB used for cache. Not accessible by UDMA.
- 64 KB IRAM2
  Can be used as general-purpose RAM or VRAM. Accessible by the CPU, LCDC, HIF, and UDMA.
- 16 KB IRAM3
  Can be used as general-purpose RAM or VRAM. Accessible by the CPU, LCDC, HIF, and UDMA.
- 2 KB DSTRAM
  Can be used as a general-purpose RAM. 256 bytes used for debugging. Accessible by the CPU and UDMA.
- 2 KB BBRAM
  Can be used retain data with a power supply separated from the system.

●Mini Cache Controller (miniCache)
- 4-way set associative method 1 KB instruction cache and the 1 KB data cache
- LRU replacement algorithm
- Automatic lock function during debug mode and the interrupt process of specified priority
- Write-through function with 1-word buffer

* A part of IRAM1 is used for cache memory.

●LCD Controller (LCDC)
- Supports color TFT panels of up to 24 bits and color/monochrome STN LCD panels of up to 16 bits.
- Supports typical resolutions up to VGA class, including 640 x 480 (VGA) and 320 x 240 (QVGA) (settings can be made to suit the target panel).
- Supports displays of up to a maximum of 16 M colors (TFT), 64 K colors (color STN), and 16- to 2-grayscale (monochrome STN).
- Setup example using internal VRAM (80 KB): 320 x 240, 8 bpp (256 colors)
- Setup example using external memory: 640 x 480, 24 bpp (full color)
- Picture-in-Picture (PIP) with Magic Color function (specified color transparency) enables two-screen overlay display control (8/16 bpp modes)
- Picture-in-Picture (PIP) function enables two screen overlay display control (32 bpp mode)
- Provides a look-up table (LUT) function to control the intensity/grayscale level.

●Universal DMA Controller (UDMA)
- Two channels of high-speed DMA and up to 14 channels of table DMA
- Dual-address transfer (specifying source and destination addresses)
- Can specify single or successive transfer mode.
- High-performance burst transfer function coupled with SDRAM controller
- Programmable transfer unit by specifying one or four bytes, one or four half words, or one or four words.
- Built-in DMA trigger system with link function.
- Can select software triggers or hardware triggers of various peripheral circuits

●SRAM Controller (SRAMC)
- Max. 8 chip enable signals are available to connect external devices.
- Allows connection of Flash ROM, SRAM, and other external devices (such as an LCD driver).
- 24-bit address bus and 8/16-bit selectable data bus
- Programmable bus access wait cycle (1 to 15 cycles)
- Supports little endian access
- Memory mapped I/O
- A part of memory space (area 6) is reserved for on-chip peripheral modules.

- Supports either A0 or BS (Bus Strobe) access type
- Supports external wait request via the #WAIT pin

●SDRAM Controller (SDRAMC)

- Max. 90 MHz 16-bit SDRAM interface
- Supports 16 M bits (2 MB) to 512 M bits (64 MB) SDRAM
- Incorporates IQB (Instruction Queue Buffer) and DQB (Data Queue Buffer).
- Optimized multi access request reduces average read latency.
- Selectable CAS latency from 1, 2 and 3
- Supports burst transfer
- Selectable synchronous clock from the same frequency and the double frequency as CPU clock.
- Built-in 12-bit auto-refresh counter
- Intelligent self-refresh function for low power operation

●High-level Calculation Module (Calculation module)

- Vector calculation (addition/subtraction/multiplication)
- Sum-of-products operation (MAC)
- Matrix operation (2 x 2, 3 x 3, 4 x 4)
- Affine transformation (3 x 3 + 3)
- Butterfly operation
- Supports signed 32-bit integers, unsigned 32-bit integers, and 32-bit fixed-point numbers with saturation.

●I^2S Audio interface (I2S)

- Supports for universal audio I^2S bus interface.
- Internal I^2S interface with 1 input channel and 1 output channel
- Supports data formats up to 24 bits.
- The output channel can be used to control the DAC device clock, word clock and bit clock respectively (an external clock can be used).
- FIFO (24 bits x 2 channels x 4) provided for each of the I/O channels
- Supports DMA transfer.

* Connection to an external DAC/ADC device is required in order to output audio signals to speakers or earphones or to input sound from a microphone.

●Host Processor Interface (HIF)

- 8-bit asynchronous interface allows external host processor to control S1C33L15 peripheral circuits.
- Hardware semaphore enables mutual exclusion.

●Clock Management Unit (CMU)

- Selectable system clock source (from OSC3, PLL, and OSC1)
- Can control on/off of the OSC3 and OSC1 oscillator circuits
- Can control the system clock division ratio (1/1 to 1/32) and the PLL frequency multiplication rate (x 1 to x 16)
- Clock control during the standby mode (SLEEP or HALT mode)
- Can control external bus clock and the divide-by ratio between the clocks of internal core and peripheral circuit

●Interrupt Controller (ITC)

- 16 channels of interrupt control reserved for S1C33 PE core
- Supports 48 channels of interrupt sources (some are reserved for system use).

●Watchdog Timer (WDT)

- 30-bit watchdog timer to generate an NMI (Non Maskable Interrupt) or a reset
- Programmable watchdog timer overflow period (NMI or reset interrupt period)
- The watchdog timer overflow signal can be output outside the IC.

●16-bit Timer (T16)

- Four channels of 16-bit timer/counter with PWM control function
- Digital DAC function is available using the PWM output and external RC filter
- Incorporates four channels of output comparator allowing for the IGBT control

●8-bit Timer (T8)

- Four channels of programmable 8-bit timer/counter

* Up to two channels are used as a baud rate counter for serial interface (UART).

●Serial Interface (UART, SIF, and EFSIO)

UART

- Two channels of UART
- Supports full-duplex communication with built-in 2-bytes receive data buffer and 1-byte transmit buffer.
- Transfer rate: 150 to 115200 bps, data length: 7 or 8 bits, parity mode: even, odd, or no parity, stop bit: 1 or 2 bits
- Parity error, framing error, and overrun error detectable

SIF (Serial Interface)

- 2 channels of clock sync./async. serial interface
- Contains 4 bytes of receive data buffer and 2 bytes of transmit data buffer for each channel
- Built-in IrDA 1.0 interface.
- Equipped with a baud-rate generator (12-bit programmable timer).

EFSIO (Extended Serial Interface with FIFO

- 2 channels of clock sync./async. serial interface
- Includes FIFO (4 bytes of receive data buffer and 2 bytes of transmit data buffer are available for each channel).
- Built-in IrDA 1.0 interface.
- Contains a baud-rate generator (12-bit timer).
- Supports ISO7816 mode.
  - Alternative data sequence(MSB first or LSB first)
  - Supports memory card interface compatible with ISO7816-3 T=0 & T=1 protocol
  - Programmable baud-rate and guard-time settings
  - Supports ISO7816 acknowledge and automatic repeat transmission

●SPI (Serial Peripheral Interface)

- Four channels of SPI
- Supports both master and slave modes.
- Data length: eight bits fixed (MSB first)
- Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
- Supports receive bit mask function and DMA transfer.

●DCSIO (I^2C Master Emulator)

- Four channels of I/O ports with a serial shifter
- Can emulate the I^2C master
- Detects I/O level to drive a state machine
- Emulates single-wire or double-wire communication protocol with software
- Supports DMA transfer.

●Real-Time Clock (RTC)

- Contains time counters (seconds, minutes, and hours) and calendar counters (days, days of the week, months, and year).
- The counters can be read and written by BCD data.
- Selectable from 24-hour and 12-hour modes
- Operable on an independent power supply (RTCVDD = 1.8 V typical) separated from system power (LVDD)
- Provides the WAKEUP output pin and #STBY input pin to control standby/wakeup

●General-Purpose I/O Ports Control (GPIO)

- Can control up to 96 I/O ports.
- Can control built-in pull-up resistors by setting resisters (excepts some ports).

* I/O ports are shared with other peripheral circuit pins (for interfaces and timers). The number of actual I/O ports available depends on the peripheral circuit used.

●SLC/MLC NAND Flash Interface for Reed-Solomon EDC (CARD)

- 8-bit SLC/MLC NAND Flash can be controlled.
- Built-in hardware Reed-Solomon EDC calculation for SLC/MLC NAND Flash

* The hardware Reed-Solomon ECC calculation function supports error detection only.

- Provides SmartMedia control (#SMRD and #SMWR can be generated).
- Supports NAND Flash booting.

●Infrared Remote Controller (REMC)

- Internal infrared remote controller with 1 input channel and 1 output channel
- The duty factor and pulse width can be configured in bit units to support various logical formats via software control.

* A connection to an infrared receiver module is required to receive infrared remote control signals.

●Operating Voltage

- Core voltage (LVDD): 1.65 to 1.95 V (1.8 V typical)
- I/O voltage (HVDD): 2.70 to 3.60 V (3.3 V typical)
- SDRAM voltage (BUSVDD): 2.30 to 3.60 V (3.3 V typical)
- RTC voltage (RTCVDD): 1.65 to 1.95 V (1.8 V typical)
- PLL voltage (PLLVDD): 1.65 to 1.95 V (1.8 V typical)

●Operating Temperature

- -40 to 85 deg. C

●Current Consumption

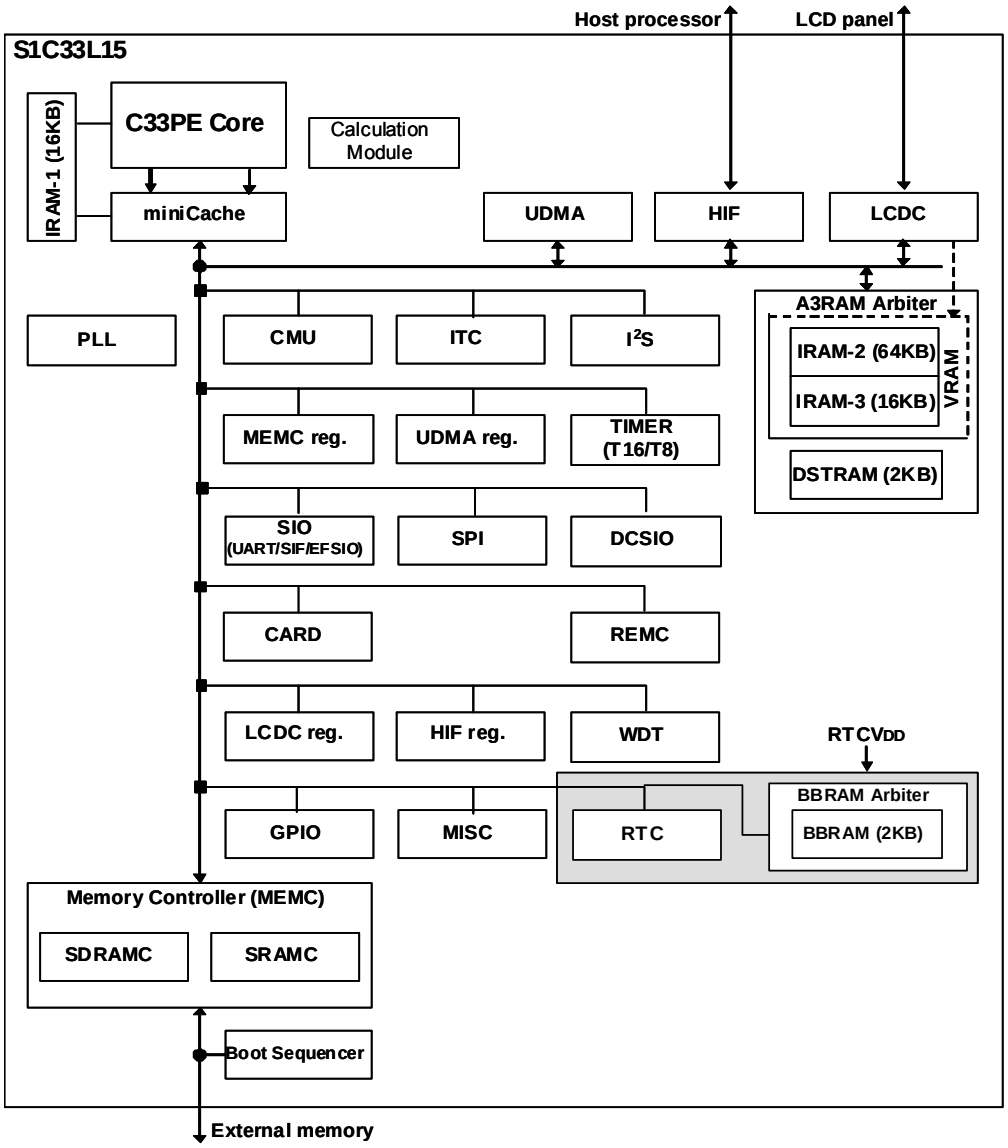
- In SLEEP mode: 1.0 µA *1
- In HALT mode: 3.5 mA *2
- During execution: 103.5 mA *3

*1 While only RTC is operating (Power is supplied only to RTCVDD and not supplied to all others)
*2 When PLL = Off, and all clocks are set to 48 MHz
*3 When PCLK = 45 MHz, MCLK = SDCLK = 90 MHz, and the clock is supplied to all peripheral circuits.
* By controlling the clocks through the Clock Management Unit, power consumption can be reduced.

●Shipping Form

- PFBGA12U-180 (12 mm x 12 mm x 1.2 mm, and 0.8 mm pitch between balls)
- QFP20-184pin (20 mm x 20 mm x 1.4 mm, and 0.4 mm pitch between pins)
- Chip

■ Block Diagram



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