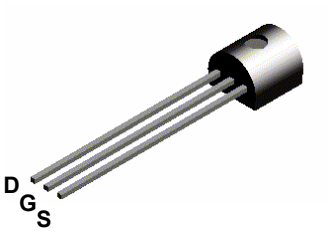
NDF0610 / NDS0610

General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 180mA DC and can deliver pulsed currents up to 1A. This product is particularly suited to low voltage applications requiring a low current high side switch.

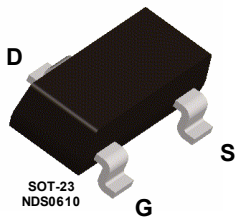
Features

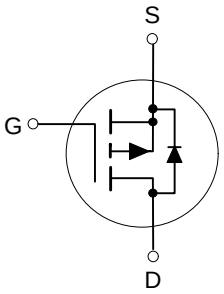
- -0.18 and -0.12A, -60V. $R_{DS(ON)}$ = 10Ω
- Voltage controlled p-channel small signal switch
- High density cell design for low $R_{DS(ON)}$
- TO-92 and SOT-23 packages for both through hole and surface mount applications
- High saturation current



TO-92

NDF0610





Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	NDF0610	NDS0610	Units
V_{DSS}	Drain-Source Voltage	-60		V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	-60		V
V_{GSS}	Gate-Source Voltage - Continuous	±20		V
	- Nonrepetitive (t_P < 50 µs)	±30		V
I_D	Drain Current - Continuous	-0.18	-0.12	A
	- Pulsed	-1		
P_D	Maximum Power Dissipation T_A = 25°C	0.8	0.36	W
	Derate above 25°C	5	2.9	mW/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
T_L	Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds	300		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	350	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -10 µA	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-200	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			10	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-10	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -1 mA	-1	-2.4	-3.5	V
		T_J = 125°C	-0.6	-2.1	-3.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.5 A		3.6	10	Ω
		T_J = 125°C		5.9	16	
		V_{GS} = -4.5 V, I_D = -0.25 A		5.2	20	
		T_J = 125°C		7.9	30	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -10 V	-0.6	-1.6		A
		V_{GS} = -4.5 V, V_{DS} = -10 V		-0.35		
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -0.1 A	70	170		mS
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz		40	60	pF
C_{oss}	Output Capacitance			11	25	pF
C_{rss}	Reverse Transfer Capacitance			3.2	5	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -25 V, I_D = -0.18 A, V_{GS} = -10 V, R_{GEN} = 25 Ω		7	10	nS
t_r	Turn - On Rise Time			5	15	nS
$t_{D(off)}$	Turn - Off Delay Time			13	15	nS
t_f	Turn - Off Fall Time			10	20	nS
Q_g	Total Gate Charge	V_{DS} = -48 V, I_D = -0.5 A, V_{GS} = -10 V		1.43		nC
Q_{gs}	Gate-Source Charge			0.6		nC
Q_{gd}	Gate-Drain Charge			0.25		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source Current				-0.18	A
I_{SM}	Maximum Pulse Source Current (Note 1)				-1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.5 A (Note 1)		-1.2	-1.5	V
		T_J = 125°C		-0.98	-1.3	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -0.5 A, dI_F/dt = 100 A/µs		40		ns
I_{rr}	Reverse Recovery Current			2.8		A

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.