



# SPN05T10

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN05T10 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN05T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

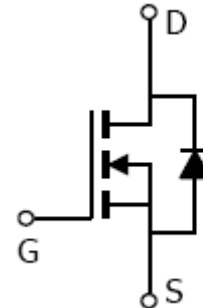
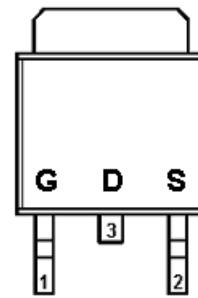
- ◆ 100V/2A,  $R_{DS(ON)} = 320m\Omega @ V_{GS} = 10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252 package design

### APPLICATIONS

- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch

### PIN CONFIGURATION

TO-252



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN05T10T252RGB	TO-252	SPN05T10

※ SPN05T10T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

( $T_A=25^{\circ}\text{C}$  Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate –Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current( $T_J=150^{\circ}\text{C}$ )	$I_D$	$T_A=25^{\circ}\text{C}$	6	A
		$T_A=70^{\circ}\text{C}$	4.6	
Pulsed Drain Current	$I_{DM}$	9	A	
Power Dissipation	$P_D$	40	W	
Operating Junction Temperature	$T_J$	-55/150	$^{\circ}\text{C}$	
Storage Temperature Range	$T_{STG}$	-55/150	$^{\circ}\text{C}$	
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62	$^{\circ}\text{C}/\text{W}$	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

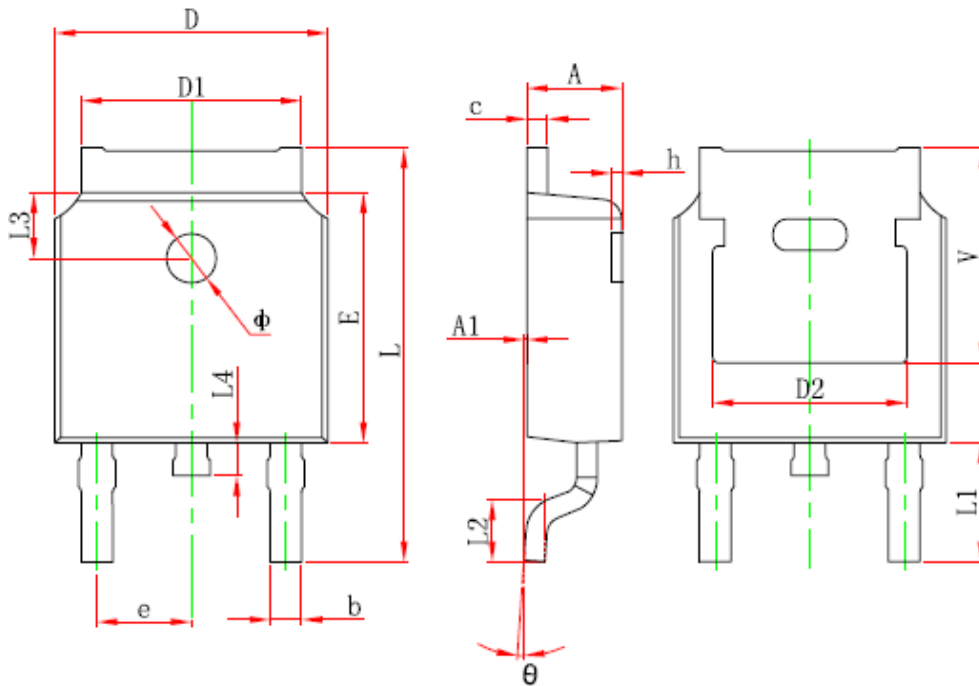
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	2.0	2.5	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS} = 10V$	2.2			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D=2A$		0.30	0.32	$\Omega$
		$V_{GS} = 4.5V, I_D=1A$		0.31	0.34	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=2A$		2.4		S
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS} = 0V$			1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=50V, V_{GS}=10V$ $I_D= 2A$		9	13	nC
Gate-Source Charge	$Q_{gs}$			2		
Gate-Drain Charge	$Q_{gd}$			1.4		
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		508		pF
Output Capacitance	$C_{oss}$			29		
Reverse Transfer Capacitance	$C_{rss}$			16.5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, I_D=2A,$ $V_{GEN}=10V, R_G=3.3\Omega$		2		nS
	$t_r$			21.5		
Turn-Off Time	$t_{d(off)}$			11.2		
	$t_f$			18.8		



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### TO-252 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	



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