Intel386™ CX EMBEDDED MICROPROCESSOR

- Static Intel386™ CPU Core
  - Low Power Consumption
  - Operating Power Supply 2.7V to 5.5V
  - Operating Frequency 12 MHz at 2.7V to 3.3V; 20 MHz at 3.0V to 3.6V; 25 MHz at 4.5V to 5.5V
- Transparent Power-Management System Architecture
  - Intel System Management Mode Architecture Extension for Truly Compatible Systems
  - Power Management Transparent to Operating Systems and Application Programs
  - Programmable Power-Management Modes
- Clock Freeze Mode Allows Clock Stopping at Any Time
- Full 32-Bit Internal Architecture
  - 8-, 16-, 32-Bit Data Types
  - 8 General Purpose 32-Bit Registers
- Runs Intel386 Architecture Software in a Cost Effective 16-Bit Hardware Environment
  - Runs Same Applications and Operating Systems as the Intel386 SX and Intel386 DX Processors
  - Object Code Compatible with 8086, 80186, 80286, and Intel386 Processors
- High Performance 16-Bit Data Bus
  - 12, 20, 25 MHz Clock
  - Two-Clock Bus Cycles
  - Address Pipelining Allows Use of Slower, Inexpensive Memories
- Integrated Memory Management Unit (MMU)
  - Virtual Memory Support
  - Optional On-Chip Paging
  - 4 Levels of Hardware-Enforced Protection
  - MMU Fully Compatible with Those of the 80286 and Intel386 DX Processors
- Virtual 8086 Mode Allows Execution of 8086 Software in a Protected and Paged System
- Large Uniform Address Space
  - 64 Megabyte Physical
  - 64 Terabyte Virtual
  - 4 Gigabyte Maximum Segment Size
- Numerics Support with Intel387™ SX and Intel387 SL Math Coprocessors
- On-Chip Debugging Support Including Breakpoint Registers
- Complete System Development Support
- High-Speed CHMOS Technology
- Two Package Types
  - 100-Pin Plastic Quad Flatpack
  - 100-Pin Shrink Quad Flatpack

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The Intel386 CX embedded microprocessor is a 32-bit, fully static CPU with a 16-bit external data bus, a 26-bit external address bus, and Intel's System Management Mode (SMM). The Intel386 CX CPU brings the vast software library of the Intel386 architecture to embedded systems. It provides the performance benefits of 32-bit programming with the cost savings associated with 16-bit hardware systems.

September 1993
Order Number: 272418-001

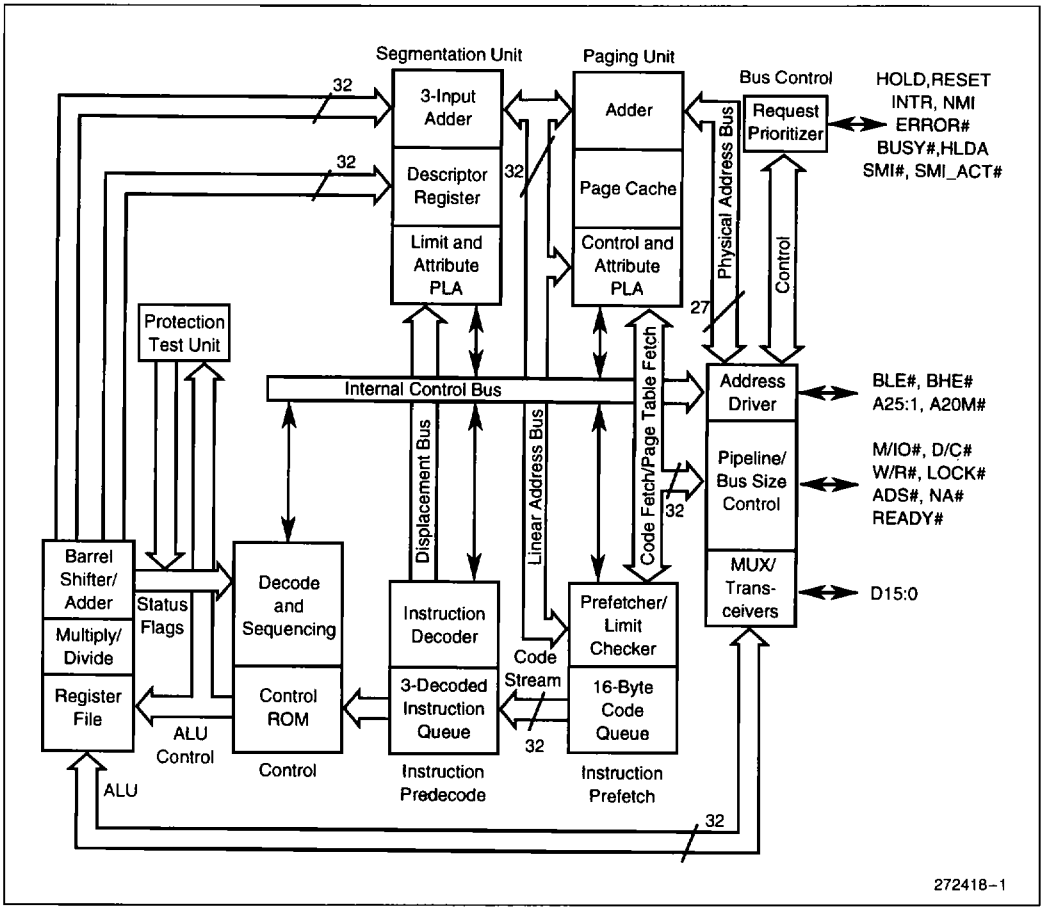

Figure 1. Intel386™ CX Microprocessor Block Diagram

1.0 PIN ASSIGNMENT

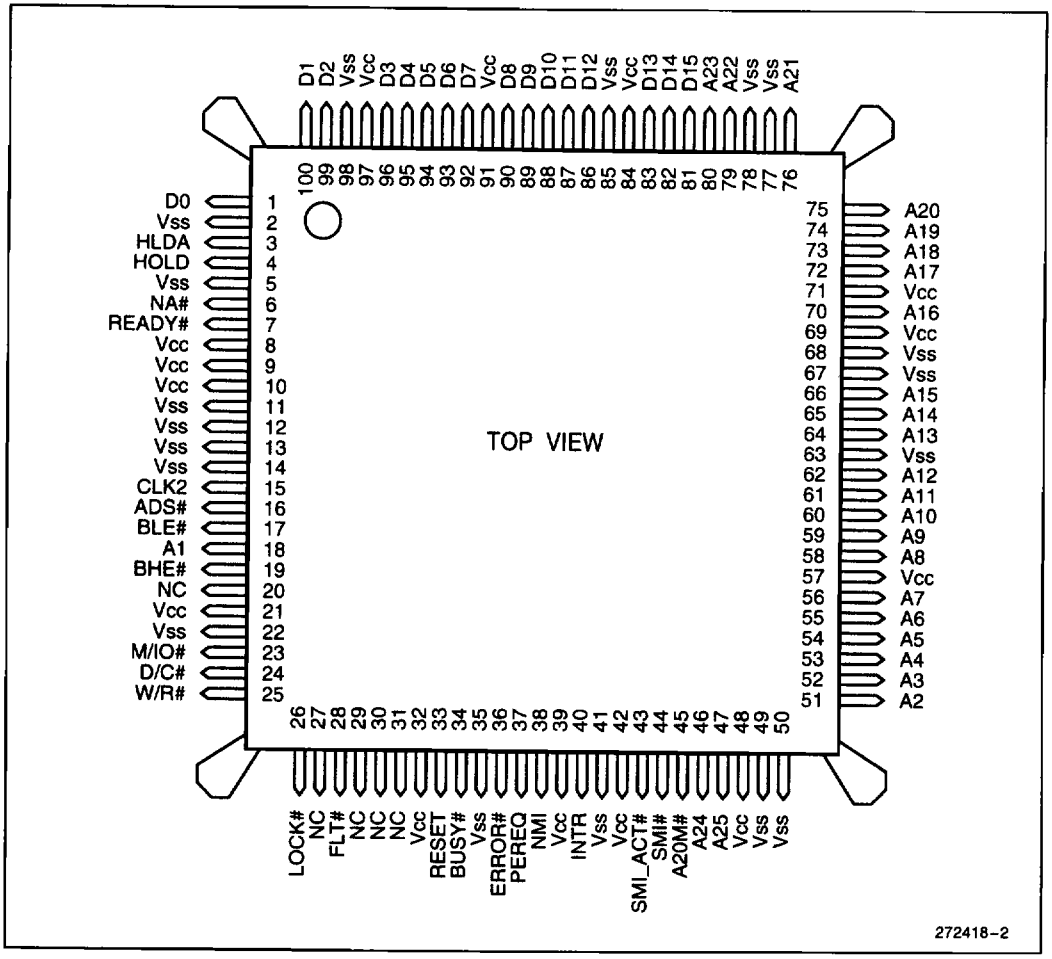

Figure 2. Intel386™ CX Microprocessor Pin Assignment (PQFP and SQFP)

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Table 1. Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	D0	26	LOCK#	51	A2	76	A21
2	V_{SS}	27	NC	52	A3	77	V_{SS}
3	HLDA	28	FLT#	53	A4	78	V_{SS}
4	HOLD	29	NC	54	A5	79	A22
5	V_{SS}	30	NC	55	A6	80	A23
6	NA#	31	NC	56	A7	81	D15
7	READY#	32	V_{CC}	57	V_{CC}	82	D14
8	V_{CC}	33	RESET	58	A8	83	D13
9	V_{CC}	34	BUSY#	59	A9	84	V_{CC}
10	V_{CC}	35	V_{SS}	60	A10	85	V_{SS}
11	V_{SS}	36	ERROR#	61	A11	86	D12
12	V_{SS}	37	PEREQ	62	A12	87	D11
13	V_{SS}	38	NMI	63	V_{SS}	88	D10
14	V_{SS}	39	V_{CC}	64	A13	89	D9
15	CLK2	40	INTR	65	A14	90	D8
16	ADS#	41	V_{SS}	66	A15	91	V_{CC}
17	BLE#	42	V_{CC}	67	V_{SS}	92	D7
18	A1	43	SMI_ACT#	68	V_{SS}	93	D6
19	BHE#	44	SMI#	69	V_{CC}	94	D5
20	NC	45	A20M#	70	A16	95	D4
21	V_{CC}	46	A24	71	V_{CC}	96	D3
22	V_{SS}	47	A25	72	A17	97	V_{CC}
23	M/IO#	48	V_{CC}	73	A18	98	V_{SS}
24	D/C#	49	V_{SS}	74	A19	99	D2
25	W/R#	50	V_{SS}	75	A20	100	D1

2.0 PIN DESCRIPTIONS

Table 2 lists the Intel386 CX Microprocessor pin descriptions. The following definitions are used in the pin descriptions:

\# The named signal is active low.
I Input signal.
O Output signal.
I/O Input and Output signal.
P Power pin.
G Ground pin.

Table 2. Pin Descriptions

Symbol	Type	Pin	Name and Function
A20M#(1)	I	45	**Address 20 Mask** controls the A20 address signal. When A20M# is low, the CPU masks off (forces low) the internal A20 physical address signal. This enables the CPU to run software that was developed using the 8086 address "wraparound" techniques. When A20M# is high, A20 is available on the address bus. While the bus is floating, A20M# has no effect on the A20 address signal. A20M# should be deasserted during SMM if the SMM handler accesses more than 1 Mbyte of memory.
A25:1(2)	O	47–46, 80–79, 76–72, 70, 66, 64, 62–58, 56–51, 18	**Address Bus** outputs physical memory or port I/O addresses.
ADS#	O	16	**Address Status** indicates that the processor is driving a valid bus-cycle definition and address onto its pins (W/R#, D/C#, M/IO#, BHE#, BLE#, and A25:1).
BHE#	O	19	**Byte High Enable** indicates that the processor is transferring a high data byte.
BLE#	O	17	**Byte Low Enable** indicates that the processor is transferring a low data byte.
BUSY#	I	34	**Busy** indicates that the math coprocessor is busy.
CLK2	I	15	**CLK2** provides the fundamental timing for the device.
D/C#	O	24	**Data/Control** indicates whether the current bus cycle is a data cycle (memory or I/O) or a control cycle (interrupt acknowledge, halt, or code fetch). When D/C# is high, the bus cycle is a data cycle; when D/C# is low, the bus cycle is a control cycle.

NOTES:
1. This pin supports the additional features of the Intel386 CX Microprocessor; it is not present on the Intel386 SX Microprocessor.
2. The A25:24 pins support the additional features of the Intel386 CX Microprocessor; they are not present on the Intel386 SX Microprocessor.

Table 2. Pin Descriptions (Continued)

Symbol	Type	Pin	Name and Function
D15:0	I/O	81–83, 86–90, 92–96, 99–100, 1	**Data Bus** inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles.
ERROR#	I	36	**Error** indicates that the math coprocessor has an error condition.
FLT#	I	28	**Float** forces all bidirectional and output signals, including HLDA, to a high-impedance state.
HLDA	O	3	**Bus Hold Acknowledge** indicates that the CPU has surrendered control of its local bus to another bus master.
HOLD	I	4	**Bus Hold Request** allows another bus master to request control of the local bus.
INTR	I	40	**Interrupt Request** is a maskable input that causes the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle.
LOCK#	O	26	**Bus Lock** prevents other system bus masters from gaining control of the system bus while it is active (low).
M/IO#	O	23	**Memory/IO** indicates whether the current bus cycle is a memory cycle or an input/output cycle. When M/IO# is high, the bus cycle is a memory cycle; when M/IO# is low, the bus cycle is an I/O cycle.
NA#	I	6	**Next Address** requests address pipelining.
NC		20, 27, 29–31	**No Connection** should always be left unconnected. Connecting a NC pin may cause the processor to malfunction or cause your application to be incompatible with future steppings of the device.
NMI	I	38	**Non-Maskable Interrupt Request** is a non-maskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge function.
PEREQ	I	37	**Processor Extension Request** indicates that the math coprocessor has data to transfer to the processor.
READY#	I	7	**Bus Ready** indicates that the current bus cycle is finished and the external device is ready to accept more data from the processor.

NOTES:
1. This pin supports the additional features of the Intel386 CX Microprocessor; it is not present on the Intel386 SX Microprocessor.
2. The A25:24 pins support the additional features of the Intel386 CX Microprocessor; they are not present on the Intel386 SX Microprocessor.

Table 2. Pin Descriptions (Continued)

Symbol	Type	Pin	Name and Function
RESET	I	33	**RESET** suspends any operation in progress and places the processor into a known reset state.
SMI#(1)	I	44	**System Management Interrupt** invokes System Management Mode (SMM). SMI# is the highest priority interrupt. It is latched on its falling edge and it forces the CPU into SMM upon completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# cannot interrupt LOCKed bus cycles or a currently executing SMM. If the processor receives a second SMI# while it is in SMM, it will latch the second SMI# on the SMI# falling edge. However, the processor must exit SMM by executing a Resume instruction (RSM) before it can service the second SMI#.
SMI_ACT#(1)	O	43	**System Management Interrupt Active** indicates that the processor is operating in System Management Mode (SMM). It is asserted when the processor initiates an SMM sequence and remains asserted (low) until the processor executes the Resume instruction (RSM).
W/R#	O	25	**Write/Read** indicates whether the current bus cycle is a write cycle or a read cycle. When W/R# is high, the bus cycle is a write cycle; when W/R# is low, it is a read cycle.
V_{CC}	P	8–10, 21, 32, 39, 42, 48, 57, 69, 71, 84, 91, 97	**System Power** provides the nominal DC supply input.
V_{SS}	G	2, 5, 11–14, 22 35, 41, 49–50, 63, 67–68, 77–78, 85, 98	**System Ground** provides the 0V connection from which all inputs and outputs are measured.

NOTES:
1. This pin supports the additional features of the Intel386 CX Microprocessor; it is not present on the Intel386 SX Microprocessor.
2. The A25:24 pins support the additional features of the Intel386 CX Microprocessor; they are not present on the Intel386 SX Microprocessor.

3.0 DESIGN CONSIDERATIONS

This section describes the Intel386 CX Microprocessor's instruction set and its component and revision identifiers.

3.1 Instruction Set

The Intel386 CX Microprocessor uses the same instruction set as the Intel386 SX Microprocessor with the following exceptions.

The Intel386 CX Microprocessor has one new instruction (RSM). This Resume instruction causes the processor to exit System Management Mode (SMM). RSM requires 338 clocks per instruction (CPI).

The Intel386 CX Microprocessor requires more clock cycles than the Intel386 SX Microprocessor to execute some instructions. Table 3 lists these instructions and the Intel386 CX Microprocessor CPI. For the equivalent Intel386 SX Microprocessor CPI, refer to the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).

3.2 Component and Revision Identifiers

To assist users, the microprocessor holds a component identifier and revision identifier in its DX register after reset. The upper 8 bits of DX hold the component identifier, 23H. (The lower nibble, 03H, identifies the Intel386 Architecture, while the upper nibble, 02H, identifies the second member of the Intel386 Microprocessor family.)

The lower 8 bits of DX hold the revision level identifier. The revision identifier will, in general, chronologically track those component steppings that are intended to have certain improvements or distinction from previous steppings. The revision identifier will track that of the Intel386 CPU whenever possible. However, the revision identifier value is not guaranteed to change with every stepping revision or to follow a completely uniform numerical sequence, depending on the type or intent of the revision or the manufacturing materials required to be changed. Intel has sole discretion over these characteristics of the component. The initial revision identifier for the Intel386 CX Microprocessor is 09H.

Table 3. Intel386™ CX Microprocessor Clocks Per Instruction

Instruction	Clock Count		
	Virtual 8086 Mode[1]	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode[3]
POPA		28	35
IN:			
Fixed Port	27	14	7/29
Variable Port	28	15	8/29
OUT:			
Fixed Port	27	14	7/29
Variable Port	28	15	9/29
INS	30	17	9/32
OUTS	31	18	10/33
REP INS	31 + 6n[2]	17 + 6n[2]	10 + 6n/32 + 6n[2]
REP OUTS	30 + 8n[2]	16 + 8n[2]	10 + 8n/31 + 8n[2]
HLT		7	7
MOV C0, reg		10	10

NOTES:
1. The clock count values in this column apply if I/O permission allows I/O to the port in virtual 8086 mode. If the I/O bit map denies permission, exception fault 13 occurs; see clock counts for the INT 3 instruction in the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).
2. n = the number of times repeated.
3. When two clock counts are listed, the smaller value refers to a register operand and the larger value refers to a memory operand.

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4.0 DC SPECIFICATIONS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .....−65°C to +150°C
Case Temperature Under Bias...−65°C to +110°C
Supply Voltage with Respect to V_{SS}..−0.5V to 6.5V
Voltage on Other Pins .....−0.5V to V_{CC} + 0.5V

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

OPERATING CONDITIONS*

Digital Supply Voltage (V_{CC}) .....2.7V to 5.5V
Case Temperature
Under Bias (T_{CASE}) .....0°C to 100°C
Operating Frequency (F_{OSC}) .....0 MHz to 25 MHz

Table 4. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{IL}	Input Low Voltage	−0.5	0.3 V_{CC}	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{ILC}	CLK2 Input Low Voltage	−0.3	+0.8	V	
V_{IHC}	CLK2 Input High Voltage	V_{CC} − 0.6 V_{CC} − 0.8	V_{CC} + 0.3 V_{CC} + 0.3	V V	V_{CC} = 2.7V to 3.6V V_{CC} = 4.5V to 5.5V
V_{OL}	Output Low Voltage I_{OL} = 2 mA I_{OL} = 0.5 mA		 0.4 0.2	 V V	
V_{OH}	Output High Voltage I_{OH} = −0.5 mA I_{OH} = −0.1 mA	 V_{CC} − 0.4 V_{CC} − 0.2		 V V	 V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 3.6V
I_{LI}	Input Leakage Current (for all pins except PEREQ, BUSY#, FLT#, ERROR#, A20M#, SMI#)		±15	μA	0 ≤ V_{IN} ≤ V_{CC}
I_{IH}	Input Leakage Current (PEREQ)		150 300	μA μA	V_{IH} = 2.2V, V_{CC} = 2.7V V_{IH} = 5.4V, V_{CC} = 5.5V(1)
I_{IL}	Input Leakage Current (BUSY#, FLT#, ERROR#, A20M#, and SMI#)		 −120 −130	 μA μA	(Note 2) V_{IL} = 0.45V, V_{CC} = 5.5V V_{IL} = 0.1V, V_{CC} = 5.5V

NOTES:
1. PEREQ input has an internal weak pull-down resistor.
2. BUSY#, FLT#, SMI#, A20M and ERROR# inputs each have an internal weak pull-up resistor.
3. I_{CC} max and I_{CCF} max measurement at worst-case frequency, V_{CC} and temperature, with 50 pF output load.
4. I_{CC} typ and I_{CCF} typ are measured at nominal V_{CC} and are not fully tested.
5. Not fully tested.

Table 4. DC Characteristics (Continued)

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_{LO}	Output Leakage Current		±15	μA	$0.45V \le V_{OUT} \le V_{CC}$
I_{CC}	Supply Current				(Notes 3, 4)
	CLK2 = 50 MHz, CLK = 25 MHz		280	mA	typ = 210 mA
	CLK2 = 40 MHz, CLK = 20 MHz		160	mA	typ = 120 mA
	CLK2 = 24 MHz, CLK = 12 MHz		100	mA	typ = 70 mA
I_{CCF}	Standby Current (Freeze Mode)				(Notes 3, 4)
	CLK2 = 50 MHz, CLK = 25 MHz		TBD	μA	I_{CCF} typ = 20 μA, V_{CC} = 5V
	CLK2 = 40 MHz, CLK = 20 MHz		TBD	μA	I_{CCF} typ = 10 μA, V_{CC} = 3.3V
	CLK2 = 24 MHz, CLK = 12 MHz		TBD	μA	I_{CCF} typ = 10 μA, V_{CC} = 3V
C_{IN}	Input Capacitance		10	pF	F_C = 1 MHz(5)
C_{OUT}	Output or I/O Capacitance		12	pF	F_C = 1 MHz(5)
C_{CLK}	CLK2 Capacitance		20	pF	F_C = 1 MHz(5)

NOTES:
1. PEREQ input has an internal weak pull-down resistor.
2. BUSY#, FLT#, SMI#, A20M and ERROR# inputs each have an internal weak pull-up resistor.
3. I_{CC} max and I_{CCF} max measurement at worst-case frequency, V_{CC} and temperature, with 50 pF output load.
4. I_{CC} typ and I_{CCF} typ are measured at nominal V_{CC} and are not fully tested.
5. Not fully tested.

5.0 AC SPECIFICATIONS

Table 5 lists output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the CLK2 rising edge crossing the $V_{CC}/2$ level.

Figure 3 shows the measurement points for AC specifications. Inputs must be driven to the indicated voltage levels when AC specifications are measured. Output delays are specified with minimum and maximum limits measured as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs ADS#, W/R#, D/C#, MI/O#, LOCK#, BHE#, BLE#, A25:1, HLDA and SMI_ACT# change only at the beginning of phase one. D15:0 (write cycles) change only at the beginning of phase two.

The READY#, HOLD, BUSY#, ERROR#, PEREQ, FLT#, A20M# and D15:0 (read cycles) inputs are sampled at the beginning of phase one. The NA#, INTR, SMI# and NMI inputs are sampled at the beginning of phase two.

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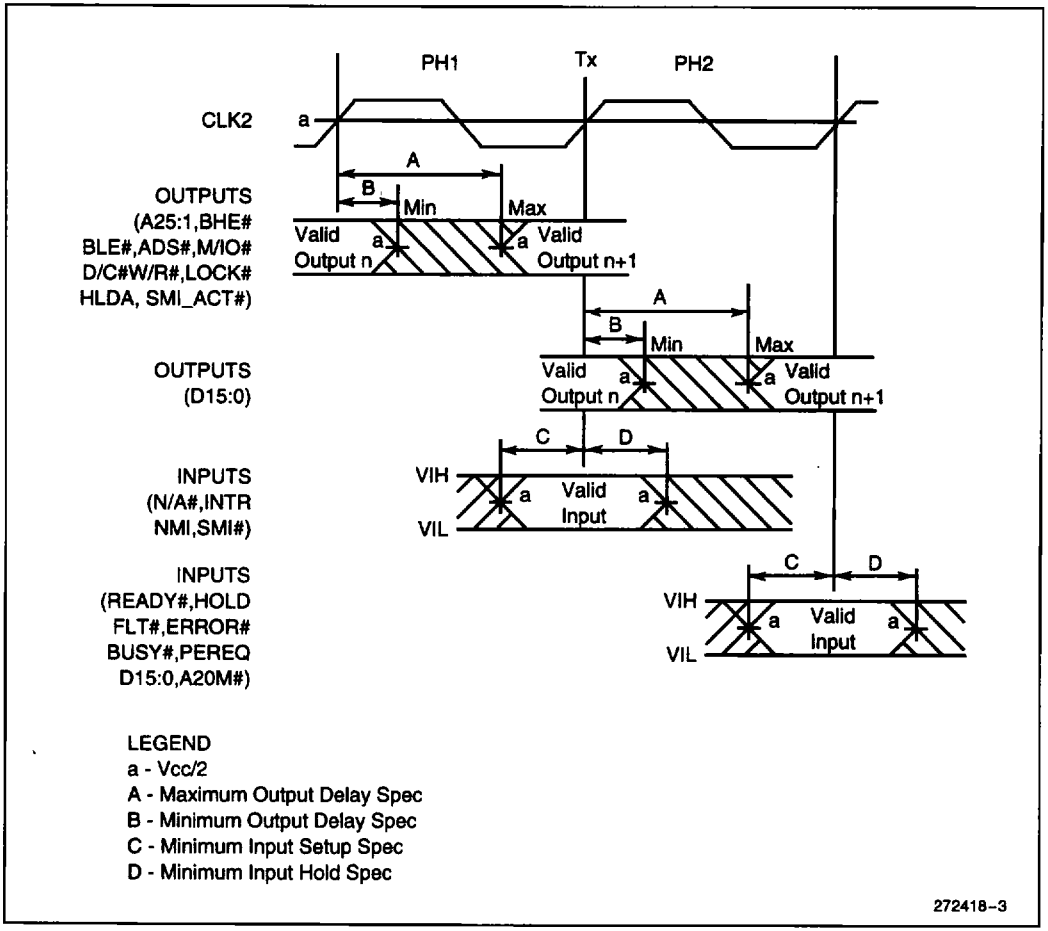

Figure 3. Drive Levels and Measurement Points for AC Specifications

Table 5. AC Characteristics

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		12 MHz 2.7V to 3.3V		Test Conditions(1)
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
	Operating Frequency	0	25	0	20	0	12.5	MHz(2)
t1	CLK2 Period	20		25		40		
t2a	CLK2 High Time	7		8		11		at $V_{CC}/2$(3)
t2b	CLK2 High Time	4		5		7		at V_{CC} − 0.8V for HV, at V_{CC} − 0.6V for LV(3)
t3a	CLK2 Low Time	7		8		11		at $V_{CC}/2$(3)
t3b	CLK2 Low Time	5		6		9		at 0.8V(3)
t4	CLK2 Fall Time		7		8		8	V_{CC} − 0.8V to 0.8V for HV, V_{CC} − 0.6V to 0.8V for LV(3)
t5	CLK2 Rise Time		7		8		8	0.8V to V_{CC} − 0.8V for HV, 0.8V to V_{CC} − 0.6V for LV(3)
t6	A25:1 Valid Delay	4	17	4	30	4	42	C_L = 50 pF(4)
t7	A25:1 Float Delay	4	30	4	32	4	45	(Note 5)

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For the LV products, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

Table 5. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		12 MHz 2.7V to 3.3V		Test Conditions(1)
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
t8	BHE#, BLE#, LOCK# Valid Delay	4	17	4	30	4	36	C_L = 50 pF(4)
t8a	SMI_ACT# Valid Delay	4	17	4	26	4	33	C_L = 50 pF(4)
t9	BHE#, BLE#, LOCK# Float Delay	4	30	4	32	4	40	(Note 5)
t10	W/R#, M/IO#, D/C#, ADS# Valid Delay	4	17	4	26	4	33	C_L = 50 pF(4)
t11	W/R#, M/IO#, D/C#, ADS# Float Delay	4	30	4	30	4	35	(Note 5)
t12	D15:0 Write Data Valid Delay	4	23	4	38	4	50	C_L = 50 pF(4)
t13	D15:0 Write Data Float Delay	4	22	4	27	4	35	(Note 5)
t14	HLDA Valid Delay	4	22	4	28	4	33	C_L = 50 pF(4)
t15	NA# Setup Time	5		5		7		
t16	NA# Hold Time	3		12		21		
t19	READY#, A20M# Setup Time	9		12		19		
t20	READY#, A20M# Hold Time	4		4		4		
t21	D15:0 Read Setup Time	7		9		9		

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For the LV products, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

Table 5. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		12 MHz 2.7V to 3.3V		Test Conditions(1)
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
t22	D15:0 Read Hold Time	5		6		6		
t23	HOLD Setup Time	9		17		26		
t24	HOLD Hold Time	3		5		7		
t25	RESET Setup Time	8		12		15		
t26	RESET Hold Time	3		4		6		
t27	NMI, INTR Setup Time	6		16		16		(Note 6)
t27a	SMI# Setup Time	6		16		16		(Note 6)
t28	NMI, INTR Hold Time	6		16		16		(Note 6)
t28a	SMI# Hold Time	6		16		16		(Note 6)
t29	PEREQ, ERROR#, BUSY#, FLT# Setup Time	6		14		16		(Note 6)
t30	PEREQ, ERROR#, BUSY#, FLT# Hold Time	5		5		5		(Note 6)

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For the LV products, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.

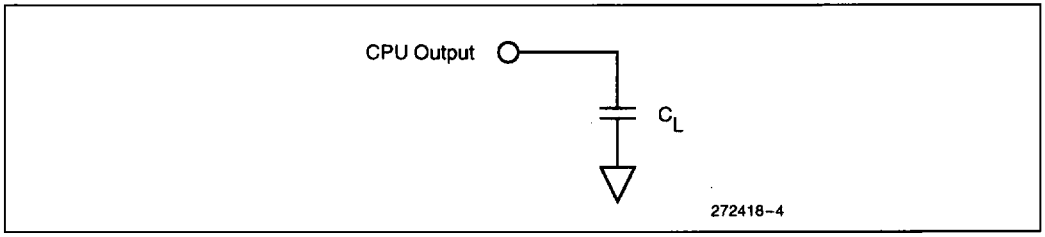

Figure 4. AC Test Loads

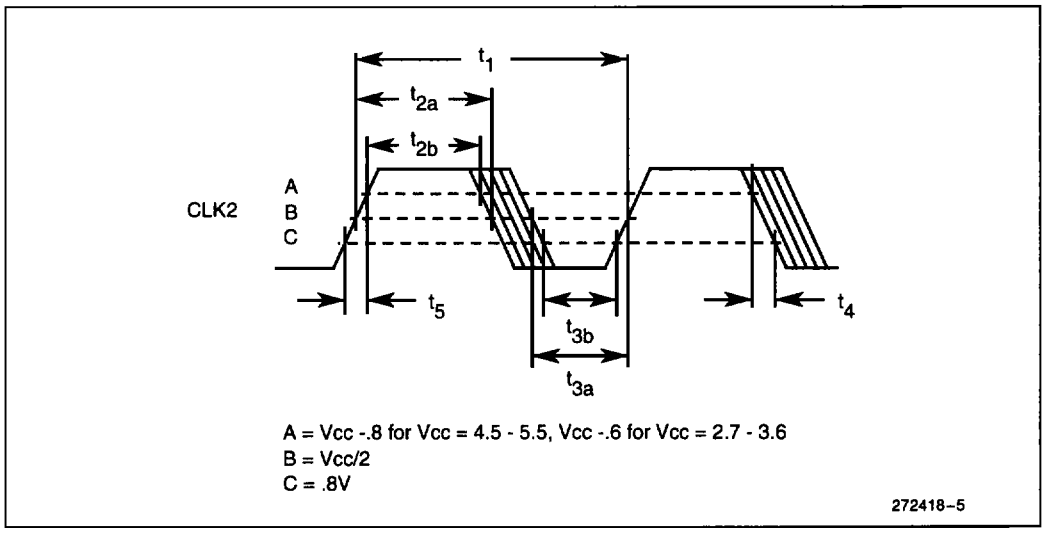

Figure 5. CLK2 Waveform

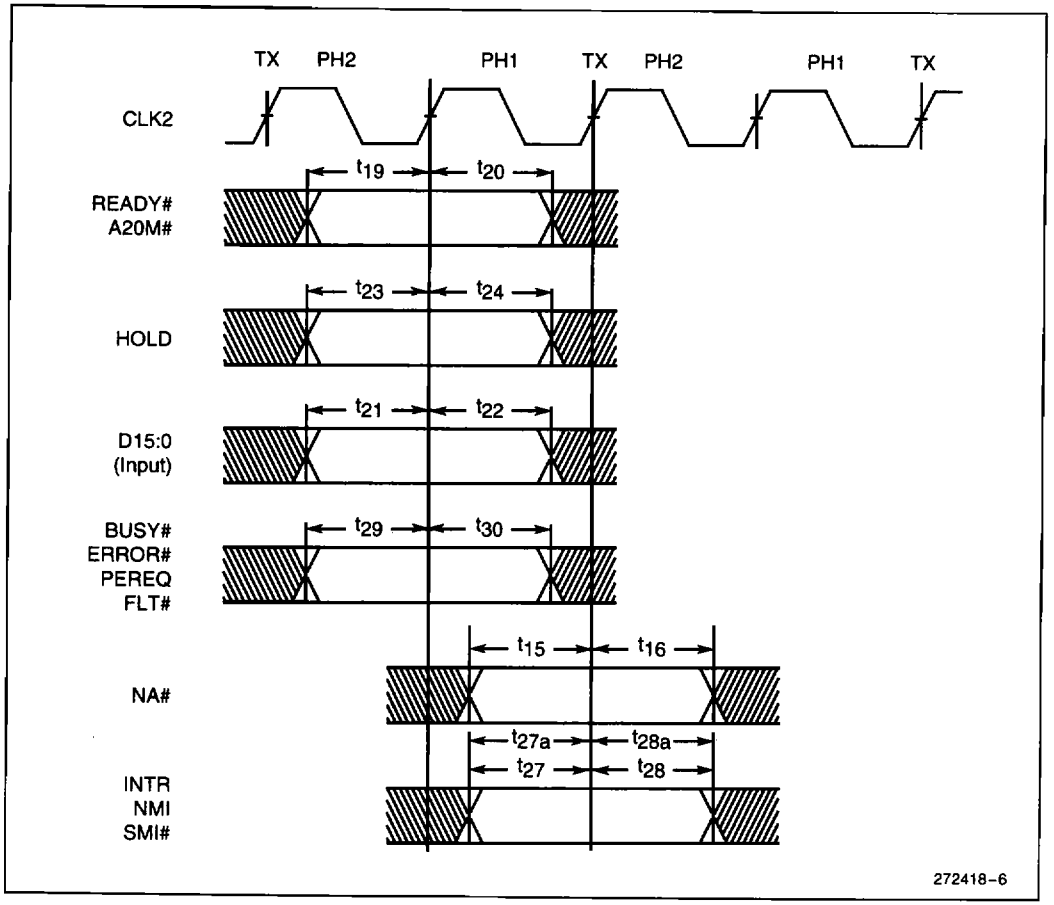

Figure 6. AC Timing Waveforms—Input Setup and Hold Timing

4

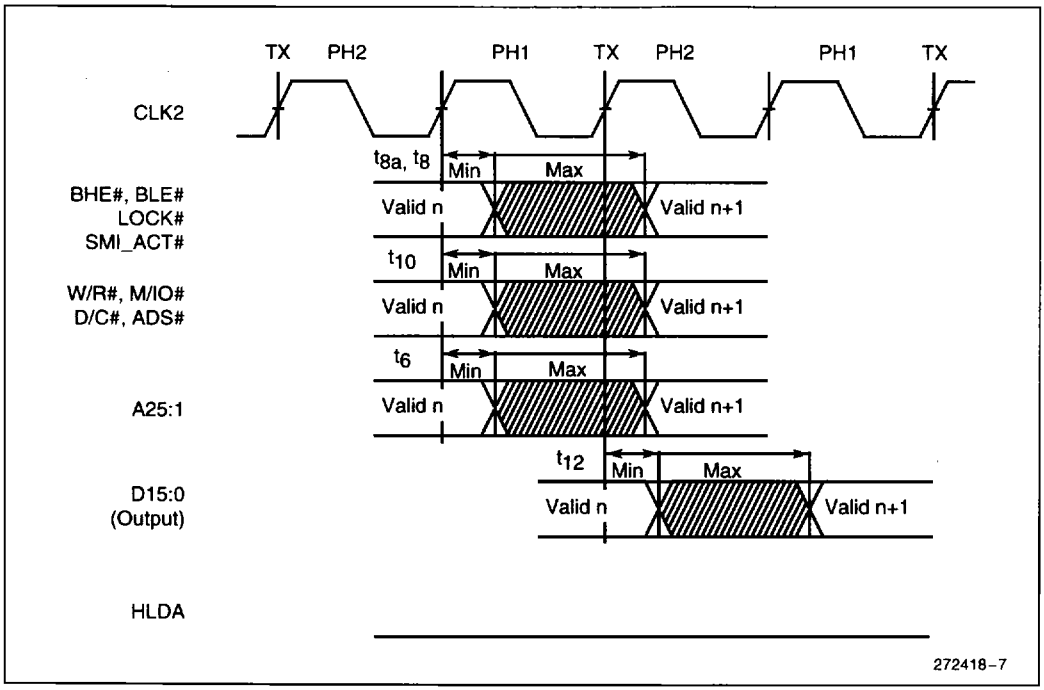

Figure 7. AC Timing Waveforms—Output Valid Delay Timing

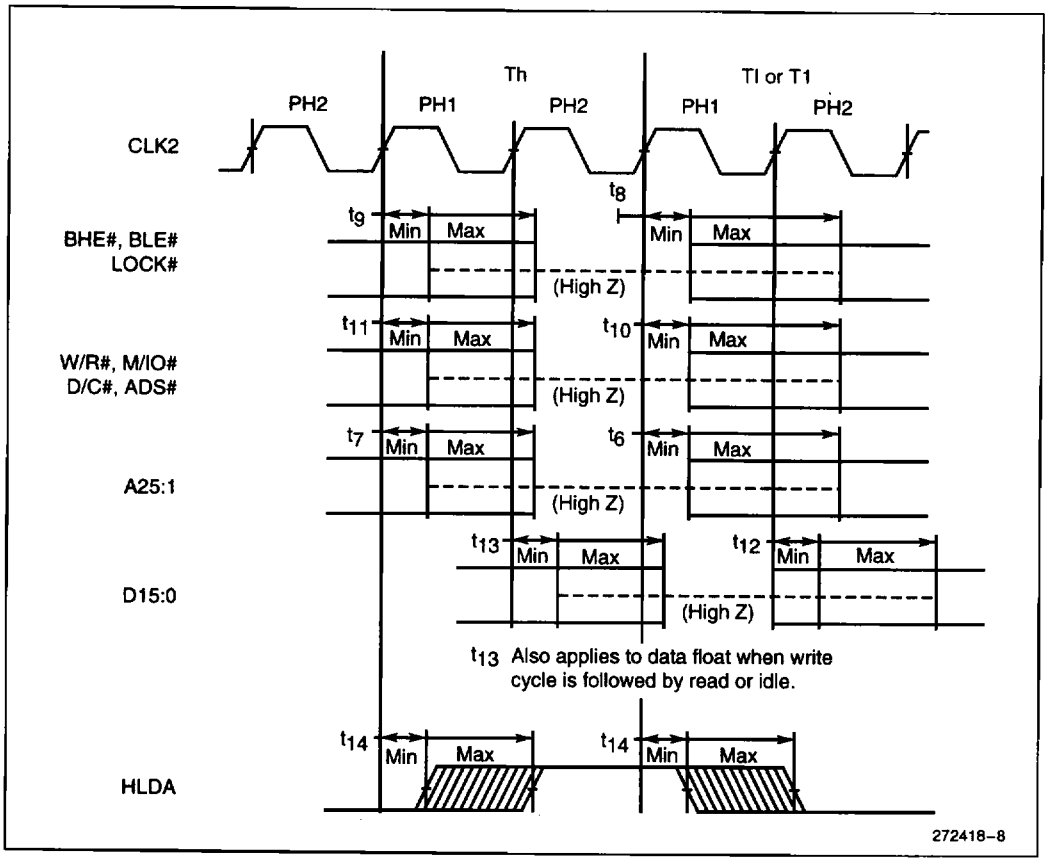

Figure 8. AC Timing Waveforms—Output Float Delay and HLDA Valid Delay Timing

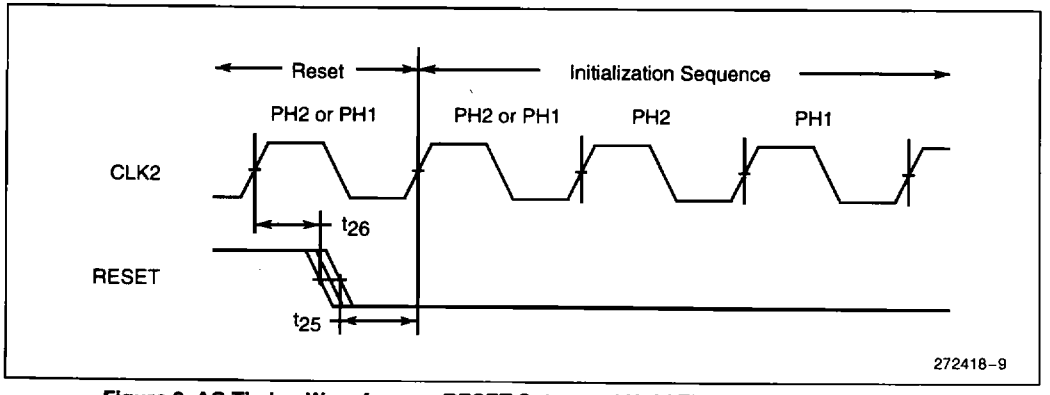

Figure 9. AC Timing Waveforms—RESET Setup and Hold Timing and Internal Phase