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HMP9701A

November 1998

AC'97 Audio Codec

Features

- **Compliant with the Audio Codec '97 Standard**
- **High Fidelity 16-Bit ΣΔ Converters**
  - **DAC SNR 87dB**
  - **ADC SNR 85dB**
- **Additional A/D for Microphone Pass-Through**
- **AC Link Serial Interface Compatible with AC'97 Digital Controllers**
- **Fixed 48kHz Sampling Rate**
- **6 Channel Input Mixer**
- **Programmable Powerdown Modes**
- **48 Lead TQFP Package**
- **Single +5V Supply**

Applications

- **Multimedia PC Applications**
  - **Desk Top PCs**
  - **Notebook PCs**
  - **PCI Sound Cards**
  - **Motherboards**
- **Video Conferencing**
- **Speaker Phones**

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Description

The HMP9701A is the next generation PC based audio codec solution. The HMP9701A is compliant to the new AC'97 standard and, as such, interfaces to any AC'97 compliant digital controller. The HMP9701A offers the designer a solution to satisfy the demand for flexibility and improved High Fidelity sound in a PC environment. As part of the AC'97 PC audio standard architecture, the HMP9701A helps pave the way for PC'97 compliant desktop, portable and entertainment PCs with a cost effective high-quality audio solution.

As the analog front end of the AC'97 chipset, the HMP9701A accepts line level audio inputs from seven different sources and converts the analog audio to 16-bit digital streams of either stereo or mono data. The 48 kss data is transmitted to the controller via the AC'97 standard five wire interface. The controller sends digital audio data to the HMP9701A to be converted to analog stereo or monaural line output using two DACs.

We include an additional ADC to be used for Acoustic Echo Canceling needed for video conferencing applications. This ADC has a dedicated microphone input. It has the same high quality performance as the stereo ADCs. The small 48 lead TQFP (Thin 1.5mm and 7mm x 7mm footprint Quad Flat Package) makes it easy to locate the analog codec close to the analog sources. Thus, reducing noise and lowering the cost of implementation.

Ordering Information

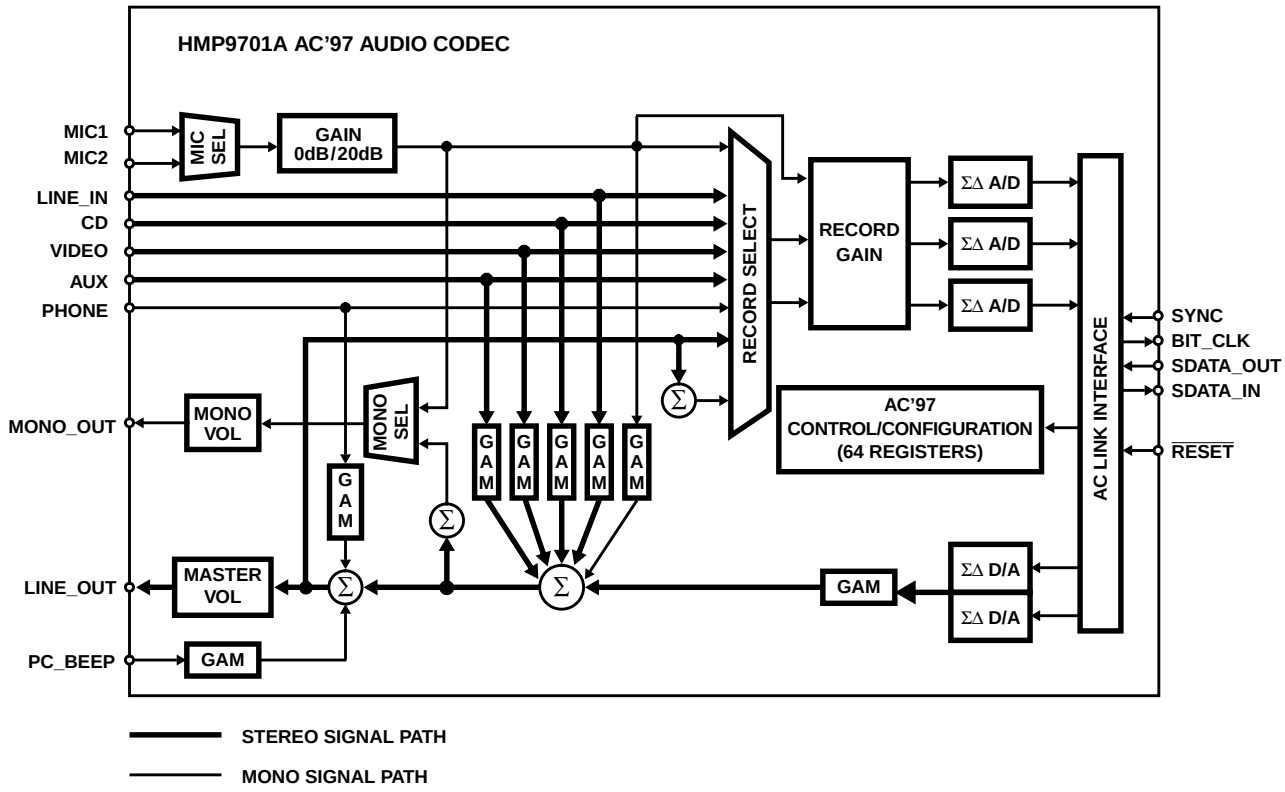
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HMP9701ACN	0 to 70	48 Ld TQFP†	Q48.7x7A
HMP9701EVAL2	PCI Bus Evaluation Board (Includes codec)		

† TQFP is also known as PQFP and MQFP.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4473.1**

Functional Block Diagram



Functional Description

The HMP9701A is a full-duplex stereo audio codec compliant to the AC'97 Codec specification. This component is designed for use in multimedia and business personal computers. The codec includes full duplex stereo converters, a mic pass through ADC, complete on-chip anti-alias filtering, and a 5 channel analog mixer with programmable gain and attenuation.

Analog Inputs

The HMP9701A has 4 stereo inputs (LINE_IN, CD, VIDEO, and AUX), two microphone level inputs (MIC1 and MIC2), and one mono line level input (PHONE). A multiplexer is provided to independently select the right and left record sources from the analog inputs listed above. In addition, the output stereo mix (LINE_OUT) or its mono equivalent may also be selected as a record source. A gain block is available to amplify the MIC inputs by 20dB to compensate for the difference between line levels and typical condenser microphone levels.

Besides being fed to the Record Select Mux, all analog inputs can be mixed (see Analog Mixer) with the stereo output from the Playback DACs. Note: all analog inputs except PHONE and PC_BEEP can be output on MONO_OUT.

There is a dedicated analog input, PC_BEEP, for the standard "Beep" signal provided on most PC/Compatible computers for power on self test and boot audio status indication. This input is mixed into each channel of the stereo line outputs.

Record ADCs

The HMP9701A provides 3 ΣΔ ADCs to record one dedicated microphone input and 2 user selectable analog inputs. The user selectable analog inputs are routed to the stereo ADCs via an programmable Input Multiplexer. The multiplexer is programmed to select the 2 record channels via the Record Select register (1Ah).

Each of the record channels pass through a programmable gain block before each ADC. The record gain for each channel is set individually and ranges from 0dB to 22.5dB in 1.5dB increments (see Record Gain Registers 1Ch and 1Eh). The gain block can also be used to mute each channel. Note: an additional gain block provides 20dB of gain on the MIC channel if activated (see MIC Volume register 0Eh).

The HMP9701A uses oversampling ΣΔ ADCs which only require a single pole passive filter for anti-alias filtering. The filter for the left, right and MIC channels is realized by placing a 1nF capacitor between the AFILT1, AFILT2, and AFILT3 pins and analog ground respectively.

Playback DACs

The HMP9701A uses oversampling single bit ΣΔ DACs to convert the stereo playback sample to an analog line level output. The output of the DACs pass through internal reconstruction filters that do not require any external components.

Analog Mixer

The Analog Mixer generates two outputs, one stereo and one mono. The stereo output is used to drive LINE_OUT and is composed of a stereo mix of all analog input sources and the audio output from the DACs. The mono output drives MONO_OUT, and it is user selectable as either MIC only or a mono mix of all the analog and PCM sources except the PHONE and PC_BEEP inputs.

The inputs to the analog mixer pass through gain/attenuate/mute (GAM) blocks. Each gain block provides volume control from -34.5dB to +12dB in 1.5dB increments (see Input Volume Registers 0Ch - 18h). Additionally, the GAM blocks can be used to mute individual mixer inputs. An additional gain of 20dB is provided for the selected MIC input. Note: for best SNR performance, the GAM block for the DAC output should be used to control PCM analog volume rather than digitally attenuating the DAC PCM input to take advantage of full resolution conversions.

Clocking

The HMP9701A derives it's internal clock from an externally attached 24.576MHz crystal. The crystal and 2 capacitors are attached to the XTL_IN and XTL_OUT pins, and it should be fundamental-mode/parallel resonant with a load capacitor as specified by the crystal manufacturer (typically 12-30pF). For an example circuit, refer to the Typical Application Schematic.

An external CMOS clock may be connected to XTL_IN instead of a crystal. If this external clocking option is used, XTL_OUT should be left floating. Please Note: No capacitors are used on the crystal pins in this mode.

The HMP9701A divides the clock source by 2 to derive the BIT_CLK provided to the companion digital controller. The digital controller should divide the provided BIT_CLK by 256 to generate the 48kHz SYNC signal used to define the audio frame transmitted over the serial digital interface (See Serial Digital Interface Section)

Serial Digital Interface

Audio Data Format

The HMP9701A supports 16-bit 2's complement linear PCM data for record and playback. The 16-bit 2's complement format (also called 16-bit signed format) is the standard method of representing 16-bit digital audio. This format gives 96dB theoretical dynamic range and is the standard for compact disk audio players. This format uses the value -32768 (8000h) to represent minimum analog amplitude while 32767 (7FFFh) represents maximum analog amplitude.

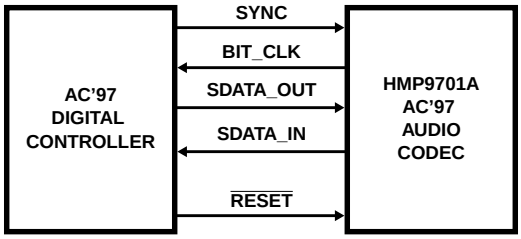


FIGURE 1. HMP9701A CONNECTION TO AC'97 CONTROLLER

Digital Serial Interface (AC Link)

The HMP9701A is linked to an AC'97 digital controller via a 5 pin digital serial interface as shown in Figure 1. This interface, the AC-link, supports bidirectional, fixed rate, serial data streams. The data transfers are based on a time division multiplexed (TDM) protocol that provides for multiple input and output audio streams together with control and status data. The AC-link protocol is based on incoming and outgoing audio frames which are each divided into 12 data slots as shown in Figure 2. The HMP9701A allocates data slots for 2 PCM playback channels, 2 PCM record channels, codec control, codec status, and a PCM microphone record channel. The remaining unused time slots are reserved.

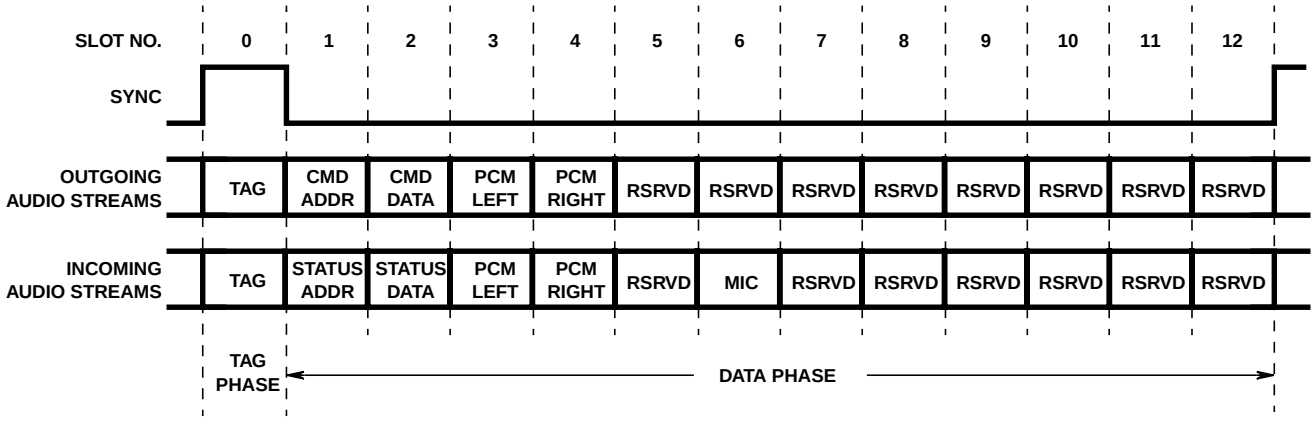


FIGURE 2. AC LINK BIDIRECTIONAL DATA FRAME

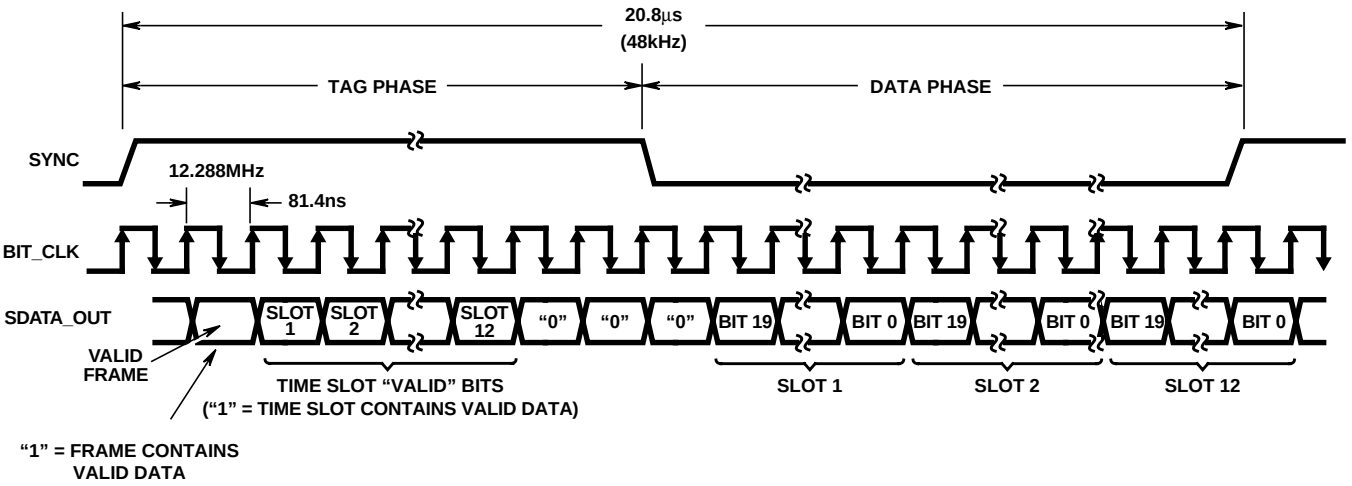


FIGURE 3. AC LINK AUDIO OUTPUT FRAME

The HMP9701A generates a serial bit clock (BIT_CLK) at 12.288MHz for synchronous data transfers on the AC Link. Data is output on SDATA_IN by the rising edge of BIT_CLK, and serial data is sampled on SDATA_OUT by the falling edge of BIT_CLK. An audio frame transfer is initiated by the assertion of SYNC for the 16 BIT_CLK's comprising the Tag Phase of the audio frame. The SYNC signal must be asserted at a fixed 48kHz rate, and it can be derived by dividing down the BIT_CLK.

The tag phase is a 16-bit data slot (Slot 0) wherein each bit is a data valid flag for an associated time slot within the current audio frame. A "1" in a given bit position of Slot 0 indicates that the corresponding time slot within the audio frame contains valid data. If the HMP9701A "tags" a slot invalid, it will set the data bits comprising that slot to zero.

AC Link Output Frame (SDATA_OUT)

The audio output frame contains data targeted for the HMP9701A's DAC inputs, and control registers. This data is transmitted in slots 1 through 4 of the audio frame as shown in Figure 2. The tag slot, Slot 0, is a special reserved time slot containing 16 bits that tell the AC-link interface circuitry the validity of the following data slots.

The HMP9701A is synchronized to the beginning of a new audio output frame when SYNC makes a low to high transition and is sampled low by the falling edge of BIT_CLK as shown in Figure 3. On the next rising of BIT_CLK, the AC'97 controller drives SDATA_OUT with the first bit of slot 0 (Valid Frame bit) which is then sampled by the HMP9701A on the subsequent falling edge of BCLK. The controller drives the remaining audio frame bits out on SDATA_OUT with each rising edge of BCLK, and the HMP9701A samples these bits on the subsequent falling edge.

The first bit of the output audio frame (Slot 0, bit 15) flags the validity of the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The HMP9701A monitors the next 4-bit positions to determine whether the data in the control and PCM output data slots is valid. The remaining 8 bits in Slot 0 are ignored as they are associated with reserved data slots.

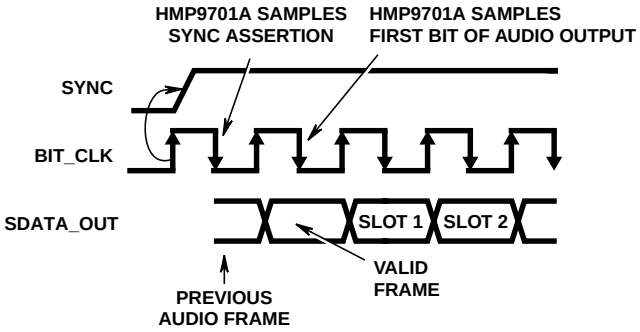


FIGURE 4. START OF AUDIO OUTPUT FRAME

The 20-bit data word in each time slot must be transmitted MSB first. If the data word targeted for a time slot is less than 20 bits, the data word must be MSB justified in the most significant bits of the time slot with the unused bits set to zero. For example, an 8-bit audio sample would be transmitted in bits 19-12 of the time slot with the trailing 12 bits set to zero. The MSB of the audio sample would map to bit 19 of the time slot. Note: for the playback of mono audio streams, the digital controller must send the same sample to each PCM output channel.

Audio Output Slot 1: Control Address

The bits in Slot 1 are used to access the 16-bit control/status registers within the HMP9701A. The address space allocated in slot 1 allows up to 64 sixteen bit registers, however, only the even registers are valid (see Control/Status register section for a complete register map). The control registers are read/writable to provide more robust testability. A read or write command is initiated by setting the Read/Write bit (Bit 19) in Slot 1. A complete bit map for Slot 1 is given in the Table 1. Note: control data will only be loaded into the target registers if Slot 2 (Control Data) is flagged as being valid.

TABLE 1. BIT MAP FOR SLOT 1: CONTROL ADDRESS

BITS	DESCRIPTION	COMMENT
19	Read/Write	1 = Read, 0 = Write
18:12	Control Register Index	Identifies the Target Control Register
11:0	Reserved	Set to “0”

Audio Output Slot 2: Control Data

This Slot is used to deliver the 16-bit control data if the current control register access is a write operation (Bit 19 of Slot 1 is set to “0”). The bit map for Slot 2 is given in Table 2.

TABLE 2. BIT MAP FOR SLOT 2: CONTROL DATA

BITS	DESCRIPTION	COMMENT
19:4	Control Register Write Data	Set to “0” if Read operation
3:0	Reserved	Set to “0”

Audio Output Slot 3: PCM Playback Left Channel

This time slot contains the audio sample that will be input to the left channel DAC. The HMP9701A DAC resolution is 17 bits. All audio samples of 17 or less bits should be MSB justified within the 20-bit frame, and the trailing bits should be set to “0”. Audio samples greater than 17 bits will be rounded to 17 bits.

TABLE 3. BIT MAP FOR SLOT 3: PCM PLAYBACK LEFT CHANNEL

BITS	DESCRIPTION	COMMENT
19:0	PCM Audio Sample for Left Channel	Set unused bit positions to “0”

Audio Output Slot 4: PCM Playback Right Channel

This time slot contains the audio sample that will be input to the right channel DAC. The DAC’s resolution is 17 bits. All audio samples of 17 or less bits should be MSB justified within the 20-bit frame, and the trailing bits should be set to “0”. Audio samples greater than 17 bits will be rounded to 17 bits.

TABLE 4. BIT MAP FOR SLOT 4: PCM PLAYBACK RIGHT CHANNEL

BITS	DESCRIPTION	COMMENT
19:0	PCM Audio Sample for Right Channel	Set unused bit positions to “0”

Audio Output Slots 5-12: Reserved

Audio output slots 5-12 are reserved for future use and should be set to “0” for proper operation.

AC Link Input Frame (SDATA_IN)

The audio input frame contains captured audio samples and codec status for output onto the AC-Link. The codec status is transmitted in slots 1 and 2, and the 16-bit captured audio samples are returned in slots 3, 4 and 6 as shown in Figure 2. As before, the tag slot, Slot 0, is a special reserved time slot containing 16 bits that tell the AC-link interface circuitry the validity of the following data slots.

The HMP9701A starts a new audio input frame when SYNC makes a low to high transition and is sampled low by the falling edge of BIT_CLK as shown in Figures 5 and 6. On the next rising edge of BIT_CLK, the HMP9701A drives SDATA_IN with the first bit of slot 0 (Codec Ready bit). The HMP9701A drives the remaining audio frame bits out on SDATA_IN with each rising edge of BIT_CLK. Note: SYNC must be synchronous to BIT_CLK.

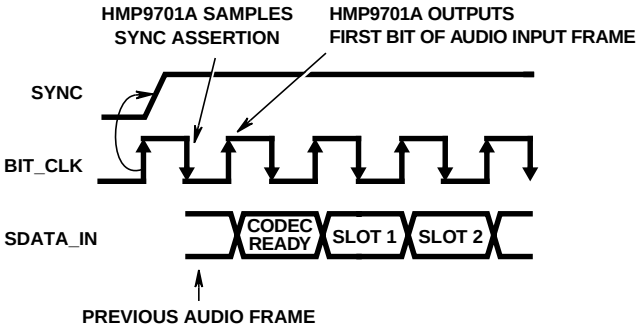


FIGURE 5. START OF AUDIO INPUT FRAME

The first bit of an input audio frame (Slot 0, bit 15) indicates whether the HMP970’s AC Link is functional. If the “Codec Ready” bit is a 0, the HMP9701A is not ready for normal operation. If the “Codec Ready” bit is “1”, the HMP9701A is ready to perform control and status register transfers. At this point, it is the responsibility of the digital controller to examine the Powerdown Control/Status register (see Control Register Section) to determine the operational state of the codec subsections. The 12 bits following the “Codec Ready” Bit in Slot 0 identify which of the 12 time slots contain valid data.

The HMP9701A outputs each time slots data word MSB first on SDATA_IN. All non-valid bit positions (for active or inactive time slots) are stuffed with 0’s by the HMP9701A.

Input Audio Slot 1: Status Address

This slot echoes the index of the control register whose contents are returned in slot 2. The data in this register is the result of a control register read operation initiated by an Output Audio Frame transfer.

TABLE 5. BIT MAP FOR SLOT 1: STATUS ADDRESS

BITS	DESCRIPTION	COMMENT
19	Reserved	Stuffed with 0
18:12	Control Register Index	Echo of Control Register Index for which data is being returned
11:0	Reserved	Stuffed with 0’s

Input Audio Slot 2: Status Data

This slot delivers control register read data.

TABLE 6. BIT MAP FOR SLOT 1: STATUS DATA

BITS	DESCRIPTION	COMMENT
19:4	Control Register Read Data	Stuffed with 0's if slot tagged invalid
3:0	Reserved	Stuffed with 0's

Input Audio Slot 3: PCM Record Left Channel

This slot contains an audio sample captured by the left channel ADC. The resolution of the ADC is 16 bits and is MSB justified in the 20-bit slot.

TABLE 7. BIT MAP FOR SLOT 3: LEFT CHANNEL RECORD DATA

BITS	DESCRIPTION	COMMENT
19:4	PCM Record Sample Left Channel	16-Bit audio sample from Left Record ADC
3:0	Reserved	Stuffed with 0's

Input Audio Slot 4: PCM Record Right Channel

This slot contains an audio sample captured by the right channel ADC. The resolution of the ADC is 16 bits and is MSB justified in the 20-bit slot.

TABLE 8. BIT MAP FOR SLOT 4: RIGHT CHANNEL RECORD DATA

BITS	DESCRIPTION	COMMENT
19:4	PCM Record Sample Right Channel	16-Bit audio sample from Right Record ADC
3:0	Reserved	Stuffed with 0's

Input Audio Slot 6: Microphone Record Channel

This slot contains an audio sample captured by the dedicated microphone ADC. The resolution of the ADC is 16 bits and is MSB justified in the 20-bit slot. This input allows higher performance echo cancellation algorithms in speaker phone applications.

TABLE 9. BIT MAP FOR SLOT 6: MICROPHONE RECORD DATA

BITS	DESCRIPTION	COMMENT
19:4	PCM Record Sample Microphone Channel	16-Bit Audio Sample From Dedicated Microphone ADC
3:0	Reserved	Stuffed with 0's

Slots 5, 7-12: Reserved

Audio input slots 5, and 7-12 are reserved, and they are set to "0".

Low Power Modes

The HMP9701A may be put in a programmable powerdown state to reduce power when no activity is required. The state of powerdown is controlled by the Powerdown Register (26h). This register provides 6 commands to powerdown various sections of the HMP9701A. A summary of the power down commands is given in Table 10 with a more complete description given in the Control Register Section. Note, the HMP9701A is a fully static design which will preserve the contents of the internal control registers if the internal clock is stopped.

TABLE 10. SUMMARY OF POWERDOWN REGISTER (26H)

BIT	FUNCTION
PR0	Input Mux and ADC Powerdown
PR1	DAC Powerdown
PR2	Analog Mixer Powerdown (V_{REF} On)
PR3	Analog Mixer Powerdown (V_{REF} Off)
PR4	Digital Interface (AC-Link) Powerdown (External CLK Off)
PR5	Internal CLK Disable

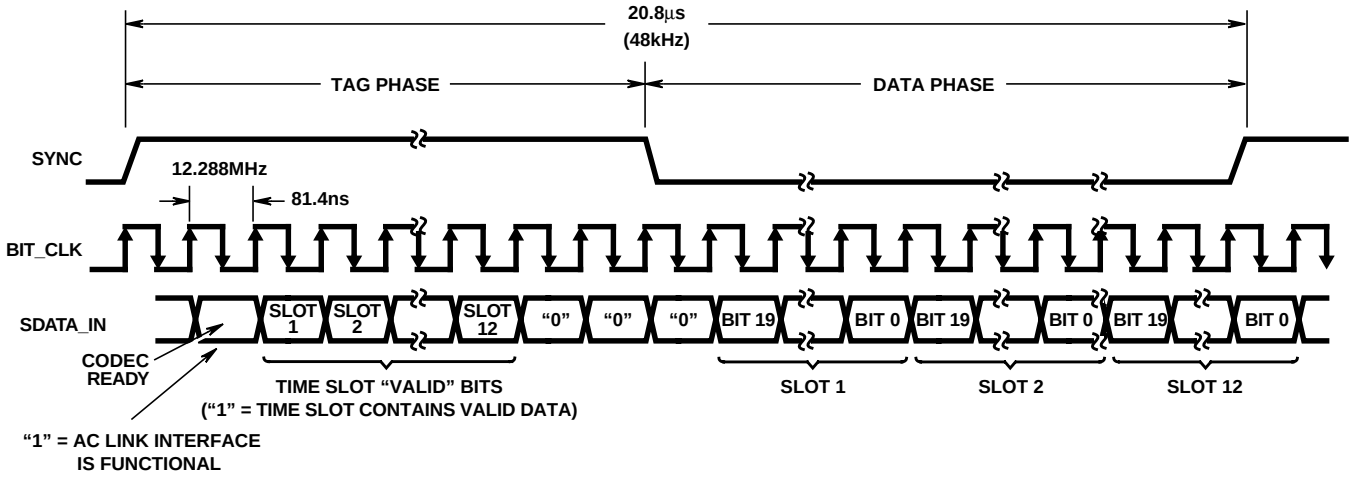
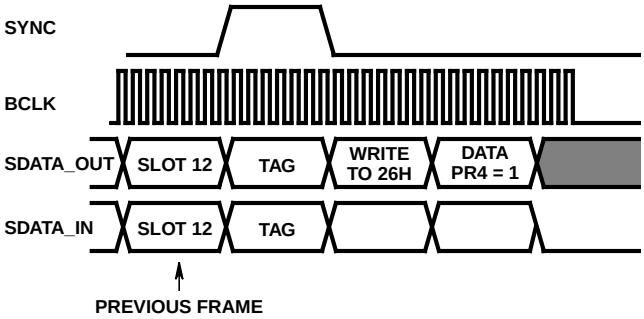


FIGURE 6. AC LINK AUDIO INPUT FRAME

AC Link Powerdown

The AC-link interface can be placed in a low power mode by setting PR4 = 1 in the Powerdown Register (see above). In this mode, both BIT_CLK and SDATA_IN are forced to a logic “low” voltage level.



NOTE: BCLK not to scale.

FIGURE 7. AC-LINK POWERDOWN TIMING

As shown in Figure 7 BIT_CLK and SDATA_IN are driven low immediately following the decode of the write to the Powerdown Control/Status Register (26h) with PR4 = 1. Once HMP9701A has been instructed to powerdown the AC Link, a special “wake up” sequence is required to return the AC-Link to active mode. Note: any valid slots of audio output samples in the frame containing the AC Link powerdown command will be dropped.

Waking up the AC-Link

There are 2 methods for bringing the HMP9701A’s AC-link out of powerdown mode. The first is a “warm reset” that preserves reactivates the AC Link while preserving the contents of the HMP9701A control registers. The second is a “Cold Reset” that reactivates the digital interface while resetting the control registers to their default values. Once the AC Link has been powered up, its operational readiness will be indicated via the Codec Ready bit in the audio input frame (slot 0, bit 15).

Warm AC Link Reset

A warm reset will reactivate the HMP9701A’s AC-link without altering the current control register values. A warm reset is generated by driving SYNC high for a minimum of 1µs in the absence of BIT_CLK. Within normal audio frames SYNC is a synchronous BIT_CLK. However, in the absence of BIT_CLK, SYNC functions as an asynchronous input that is used to generate a warm reset. The activation of BIT_CLK will not occur until after the falling edge (high to low transition) of the “wake up” SYNC. Note: the HMP9701A will not respond to a “warm reset” via the SYNC input for 4 audio frame times following the frame that triggered the powerdown.

Cold AC Link Reset

A cold reset is achieved by asserting $\overline{\text{RESET}}$ for a minimum of 1µs. By driving $\overline{\text{RESET}}$ low, BIT_CLK will be activated, the AC-Link will return to normal operation, and all HMP9701A control registers will be initialized to their default values. $\overline{\text{RESET}}$ is an asynchronous HMP9701A input. Note: the HMP9701A will remain in the reset state as long as $\overline{\text{RESET}}$ is asserted “low”.

Suggested Powerdown Sequences

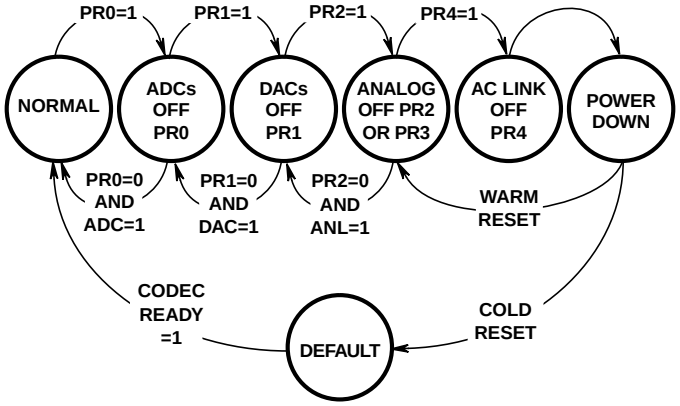


FIGURE 8. EXAMPLE OF SEQUENTIAL POWERDOWN

Figure 8 illustrates the complete powerdown of the HMP9701A. Starting from normal operation, sequential writes to the Powerdown Register are performed to powerdown one codec section at a time. After powering down the converters and the analog front end, a final write to PR4 is executed to shut down the HMP9701A’s digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values.

A warm reset can be used to wake up the AC link which can then be used to sequentially power up each codec section. Each section should be powered up sequentially, and the Powerdown Control/Status register (26h) should be read to verify that a powered up section is stable/ready before preceding to power up the next section as shown in Figures 8 and 9. Note: after a complete powerdown, care must be taken to make sure the Analog Mixer (PR2, PR3) is powered up and stable before preceding to power up the ADCs and DACs.

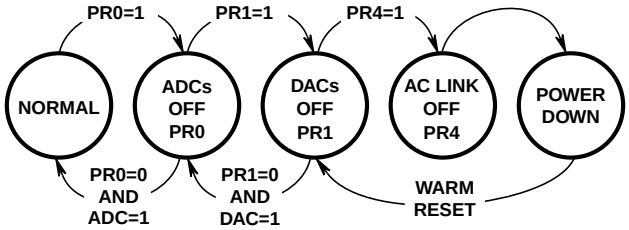


FIGURE 9. HMP9701A POWERDOWN/UP WITH ANALOG ALIVE

The Figure 9 illustrates an HMP9701A powerdown sequence that will keep all the mixers operational with the static volume settings contained in their associated registers. This powerdown scenario could be used to place the HMP9701A in low power mode while preserving the capability to play a CD (or external LINE_IN source) through the HMP9701A to the speakers.

Testability

The HMP9701A provides a test mode to support the in circuit test capabilities provided by automatic test equipment (ATE). In this mode, the HMP9701A drives its digital AC-Link outputs (BIT_CLK and SDATA_IN) to a high impedance state. This allows for in circuit testing of the digital controller component of the sound subsystem.

The HMP9701A enters ATE test mode when SDATA_OUT is sampled high by the trailing edge of $\overline{\text{RESET}}$ (see AC Timing Diagrams). The HMP9701A will remain in test mode until a "cold" reset returns the part to normal operation.

Control/Status Registers

The HMP9701A contains a bank of 16-bit control/status registers to control and monitor part operation. The control registers are accessed via the even addresses within the 6-bit address space provided in Slot 1 of the Audio Output Frame. The control/status register address map is given in Table 20.

Reset Register (Index 00h)

Writing any value to this register performs a register reset that causes all registers to revert to their default values. Reading this register returns the AC'97 ID code that specifies the optional AC'97 features supported by the HMP9701A. This register will read back 0001h to indicate that the HMP9701A provides the optional ADC for a dedicated MIC channel.

Master Volume Control Registers (Index 02h, 06h)

These registers manage the output audio volumes. Register 02h sets the master stereo volume (LINE_OUT_L, LINE_OUT_R) and Register 06h controls the mono volume (MONO_OUT). Each volume step corresponds to 1.5dB. The MSB of both registers is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

TABLE 11. MASTER VOLUME SETTINGS

MUTE	MX5...MX0	FUNCTION
0	00 0000	0dB Attenuation
0	01 1111	46.5dB Attenuation
0	1x xxxx	46.5dB Attenuation
1	xx xxxx	-∞dB Attenuation
Default Value: 8000h (0dB Gain with Mute On)		

The HMP9701A supports 5 bits of gain control for the stereo line out and mono out. The right and left stereo channels are controlled via MR4:0 and ML4:0 respectively. The mono output is controlled by MM4:0. Writing a "1" to MR5, ML5, or MM5 will force the volume level to max attenuation, Mx4:0 = 11111 (46.5dB attenuation). Note: if these registers are written with Mx5:0 = 1xxxx, they will read back Mx5:0 = 01111.

PC Beep Register (Index 0Ah)

This register controls the level of the PC Beep input. The PC Beep is attenuated as specified by the contents of this register and mixed equally into both the right and left output channels. The PC_BEEP input is attenuated in 3dB steps from 0dB to 45dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at - ∞dB.

TABLE 12. PC_BEEP ATTENUATION SETTINGS

MUTE	PV3:0	FUNCTION
0	0000	0dB Attenuation
0	1111	45dB Attenuation
1	xxxx	-∞dB Attenuation
Default Value: 8000h (0dB Gain w/ Mute on)		

Input Volume Control (Index 0Ch- 18h)

These registers control the input gain/attenuate/mute (GAM) blocks through which each of the analog mixer's inputs pass. Each GAM block has a 5-bit control that supports setting the gain in increments of 1.5dB. A total gain range from +12dB to -34.5dB is supported. The MSB of each register is a Mute bit that will set the gain to -∞dB when programmed to 1. Note: register 0Eh (Mic Volume Register) has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on.

TABLE 13. ANALOG MIXER INPUT GAIN SETTINGS

MUTE	PV3:0	FUNCTION
0	00000	+12dB Gain
0	01000	0dB Gain
0	11111	-34.5dB Gain
1	xxxx	-∞dB Gain
Default: All GAM blocks set to Mute with 0dB Gain (see Table 20)		

Record Select (Index 1Ah)

This register is used to select the record source for the left and right record ADC's. The selections are summarized below in Table 14 and 15.

TABLE 14. RECORD SELECT RIGHT CHANNEL

SR2:0	RIGHT RECORD SOURCE
0	MIC
1	CD_R
2	VIDEO_R
3	AUX_R
4	LINE_IN_R
5	Stereo Mix Right
6	Mono Mix
7	PHONE
Default: 000 (MIC in)	

TABLE 15. RECORD SELECT LEFT CHANNEL

SL2:0	RIGHT RECORD SOURCE
0	MIC
1	CD_L
2	VIDEO_L
3	AUX_L
4	LINE_IN_L
5	Stereo Mix Right
6	Mono Mix
7	PHONE
Default: 000 (MIC in)	

Record Gain Registers (Index 1Ch and 1Eh)

These registers control the record gain for both the MIC input and the selected stereo inputs (see Record Select Register). The gain is programmed in steps of 1.5dB and ranges from 0dB to +22.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel(s) is set at -∞dB.

TABLE 16. RECORD GAIN SETTINGS

MUTE	PV3:0	FUNCTION
0	0 1111	+22.5dB Gain
0	0 0000	0dB Gain
1	x xxxx	-∞dB Gain
Default: 8000h (0dB Gain with Mute on)		

General Purpose Register (Index 20h)

This register is used to control several miscellaneous functions within the HMP9701A. These include the selection of Mic input source, the selection of MONO_OUT source, and activation of ADC/DAC loopback mode. When loopback mode is enabled, the ADC output is looped back to the DAC input bypassing the AC-link, thus allowing for full system performance measurements.

TABLE 17. GENERAL PURPOSE CONTROL

BIT	FUNCTION
MIX	Mono Output Select (0 = Mix, 1 = MIC)
MS	Mic Select (1 = Mic2, 0 = Mic1)
LPBK	ADC/DAC Loopback Mode
Default: 0000h	

Powerdown Control/Status Register (Index 26h)

This register is used to program the HMP9701A's powerdown states and monitor subsystem status. The upper bits of this register are used to power up/down individual sections within the codec as summarized in Table 18.

TABLE 18. POWERDOWN CONTROL

BIT	FUNCTION
PR0	Input Mux and ADC's (1 = PWR Down, 0 = PWR Up)
PR1	DACs (1 = PWR Down, 0 = PWR Up)
PR2	Analog Mixer Powerdown with V_{REF} Left On (1 = PWR Down, 0 = PWR Up)
PR3	Analog Mixer Powerdown with V_{REF} Turned Off (1 = PWR Down, 0 = PWR Up)
PR4	Digital Interface (AC Link) powerdown (BCLK off) (1 = PWR Down, 0 = PWR Up)
PR5	Internal Clock Disable (1 = CLK Off, 0 = CLK On)
Default: na	

The lower byte of this register is used to monitor the status of individual sections with in the HMP9701A. The status bits, as summarized in Table 19, indicate whether a subsection is in it's normal operational state (Ready). Note: the status bits are read only, and writes to this register will have no effect on the state of these bits.

TABLE 19. POWERDOWN STATUS

BIT	FUNCTION
REF	V_{REFs} at Nominal Level ($1 = V_{REF}$ Ready, $0 = V_{REF}$ Down)
ANL	Analog Mixer Powerdown (1 = Mixer Up, 0 = Mixer Down)
DAC	DAC Ready for Audio Samples (1 = Ready, 0 = Not Ready)
ADC	ADC Section Ready to Record (1 = Ready, 0 = Not Ready)
Default: na	

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-link and AC'97 control and status registers are in a fully operational state. It is the responsibility of the digital controller to further probe the Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Reserved Registers (Index 28h - 7ah)

These are reserved. Do not write to these registers.

Vendor ID Registers (Index 7Ch - 7Eh)

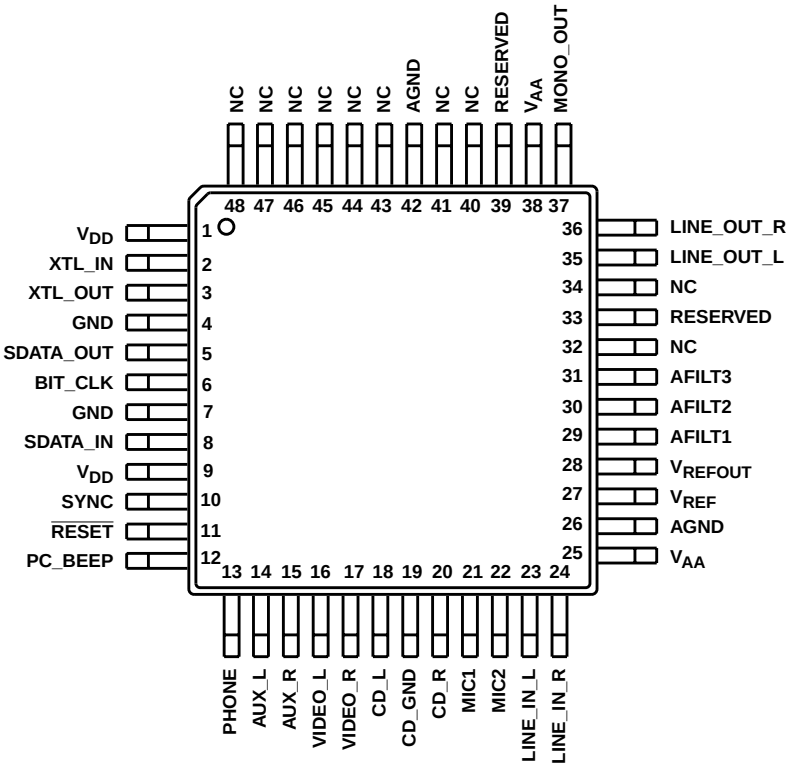
This register contains the Harris Semiconductor vendor ID. The ID method is a Microsoft's Plug and Play Vendor ID code with F7:0 the first character of that ID, S7:0 the second character and T7:0 the third character. These three characters are ASCII encoded, and they will read back as 'HRS'. The REV7:0 field is for the Revision number.

TABLE 20. CONTROL/STATUS REGISTER ADDRESS MAP

REG	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	na
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	MM5	MM4	MM3	MM2	MM1	MM0	8000h
08h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	8000h
0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	GN5	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	GN5	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Vol	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	Record Gain Mic	Mute	X	X	X	X	X	X	X	X	X	X	X	GM3	GM2	GM1	GM0	8000h
20h	General Purpose	X	X	X	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
24h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
26h	Powerdown Ctrl/Stat	X	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na
28h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
7Ah	Vendor Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4852
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5300

Pinout

HMP9701A (TQFP)
TOP VIEW



Pin Descriptions

NAME	TQFP PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
DIGITAL I/O			
$\overline{\text{RESET}}$	11	I	RESET - This active low signal causes a HMP9701A hardware reset that will return the control/status registers to their default conditions.
SYNC	10	I	SYNC - 48kHz sync pulse which defines the beginning of serial audio I/O frames. Note: must be synchronous to BIT_CLK.
BIT_CLK	6	O	BIT Clock - 12.288MHz serial data clock derived by dividing down 24.576MHz crystal input.
SDATA_OUT	5	I	Serial Data Out - Output bit stream that contains audio playback samples as well as control data. This input is sampled on the falling edge of BIT_CLK.
SDATA_IN	8	O	Serial Data In - Input bit stream that contains recorded audio samples as well as codec status information. Data output on the rising edge of BIT_CLK.
ANALOG I/O			
PC_BEEP	12	I	PC Beep. Mono Input for PC Beep pass through to LINE_OUT. This input is attenuated from 0dB to 45dB in 3dB steps and then summed with left and right line outputs (LINE_OUT_L, LINE_OUT_R)
PHONE	13	I	Phone. Mono Input from telephony subsystem speaker phone (or DLP - Down Line Phone)
MIC1	21	I	Microphone Input 1. The MIC input may be either line-level or -20dB from line-level. In the latter case, a software controlled 20dB gain block may be activated.
MIC2	22	I	Microphone Input 2. The MIC input may be either line-level or -20dB from line-level. In the latter case, a software controlled 20dB gain block may be activated.
LINE_IN_L	23	I	Left Line Input. The left line-level may be selected for recording via one of the stereo ADC's via the Input Mux. In addition, this input can be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with left line output (LINE_OUT_L).

Pin Descriptions (Continued)

NAME	TQFP PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
LINE_IN_R	24	I	Right Line Input. The right line-level may be selected for recording via one of the stereo ADC's via the Input Mux. In addition, this input can be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with right line output (LINE_OUT_R).
CD_L	18	I	Left CD Audio Channel. This line-level input may be input to one of the stereo ADC's via the Input Mux. It can also be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with the Left Line Output (LINE_OUT_L).
CD_GND	19	I	CD Audio Analog Ground.
CD_R	20	I	Right CD Audio Channel. This line-level input is selected for input to one of the stereo ADCs via the Input Mux. It can also be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with the Right Line Output (LINE_OUT_R).
VIDEO_L	16	I	Left Video Input. This line-level input is driven with the left channel audio track from a video source. The signal is selected for input to one of the stereo ADCs via the Input Mux, and it can be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with Left Line Output (LINE_OUT_L).
VIDEO_R	17	I	Right Video Input. This line-level input is driven with the right channel audio track from a video source. The signal is selected for input to one of the stereo ADCs via the Input Mux, and it can be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with Right Line Output (LINE_OUT_R).
AUX_L	14	I	Left Auxiliary Input. This line-level input is input to one of the stereo ADCs via the Input Mux. It can also be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with the Left Line Output (LINE_OUT_L).
AUX_R	15	I	Right Auxiliary Input. This line-level input is input to one of the stereo ADCs via the Input Mux. It can also be gained/attenuated from +12dB to -34.5dB in 1.5dB steps and then summed with the Right Line Output (LINE_OUT_R).
LINE_OUT_L	35	O	Left Line Output. This line level output is the post-mixed output for the left audio channel. The audio output passes through a Master Volume block that provides attenuation from 0dB to 45dB in 1.5dB steps.
LINE_OUT_R	36	O	Right Line Output. This line level output is the post-mixed output for the right audio channel. The audio output passes through a Master Volume block that provides attenuation from 0dB to 45dB in 1.5dB steps.
MONO_OUT	37	O	Mono Output. This user selectable line level output is either the post-mixed output or the microphone input. The mono output passes through a Mono Volume block that provides attenuation from 0dB to 45dB in 1.5dB steps.
MISCELLANEOUS			
V_{REF}	27	O	Voltage Reference. Nominal 2.25V reference output. Should not be used to sink or source current.
V_{REFOUT}	28	O	Voltage Reference Out. Nominal 2.25V reference output with 5mA drive capability. Intended a microphone bias.
AFILT1	29	O	Anti-Alias Filter 1 (Left Record Channel). This pin requires a 1nF capacitor to analog ground for proper operation.
AFILT2	30	O	Anti-Alias Filter 2 (Right Record Channel). This pin requires a 1nF capacitor to analog ground for proper operation.
AFILT3	31	O	Anti-Alias Filter 3 (MIC Record Channel). This pin requires a 1nF capacitor to analog ground for proper operation.
XTL_IN	2	I	24.576MHz Crystal Input. This pin may also be used to input an external 24.576MHz clock source.
XTL_OUT	3	O	24.576MHz Crystal Output. Leave this pin unconnected when using an external clock source.
V_{AA}	25, 38	I	Analog Supply Voltage (5.0V).
AGND	26, 42	I	Analog Ground.
V_{DD}	1, 9	I	Digital Supply Voltage (5.0V).
GND	4, 7	I	Digital Ground.
Reserved	33,39		These pins should NOT be connected externally to any device. They must be left floating!

Absolute Maximum Ratings

Supply Voltage 7.0V
Input Voltages . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Temperature Range
HMP9701ACN . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
TQFP Package 76
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Electrical Specifications

V_{CC} = 5.0V, T_A = 25^oC, Note 1

PARAMETER	SYMBOL	TEST CONDITION	HMP9701ACN MIN	HMP9701ACN TYP	HMP9701ACN MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Current	Digital I_{CCOP}	f_{CLK} = 24.576MHz, V_{DD} = 5.0V, Outputs Not Loaded	-	-	35	mA
	Analog I_{CCOP}	f_{CLK} = 24.576MHz, V_{AA} = 5.0V, Outputs Not Loaded	-	-	80	mA
Power Supply Rejection (1kHz, 10mV_{RMS})			-	50	-	dB
DIGITAL I/O						
Input Logic High Voltage, Digital Inputs	V_{IH}	V_{DD} = Max	2.0	-	-	V
Input Logic High Voltage, XTL_IN	V_{IH}	V_{DD} = Max	0.7*V_{DD}	-	-	V
Input Logic Low Voltage, Digital Inputs	V_{IL}	V_{DD} = Min	-	-	0.8	V
Input Logic Low Voltage, XTL_IN	V_{IL}	V_{DD} = Min	-	-	0.3*V_{DD}	V
Input Logic Current	I_{IH}, I_{IL}	V_{DD} = Max, Input = 0V or 5.25V	-10	-	+10	µA
Output Logic High Voltage	V_{OH}	I_{OH} = -4mA, V_{DD} = Max	2.4	-	-	V
Output Logic Low Voltage	V_{OL}	I_{OL} = 4mA, V_{DD} = Min	-	-	0.4	V
Three-State Output Current Leakage	I_{OZ}		-10	-	+10	µA
Rise/Fall Time (SDATA_IN, BIT_CLK)	t_r, t_f	Note 1	-	-	6.0	ns
Input/Output Capacitance	C_{IN}	CLK Frequency = 1MHz, Note 2, All Measurements Referenced to Ground T_A = 25^oC	-	-	8	pF

Timing Specifications (Notes 1, 5)

PARAMETER	SYMBOL	TEST CONDITION	HMP9701ACN MIN	HMP9701ACN TYP	HMP9701ACN MAX	UNITS
BIT_CLK Frequency		24.576MHz Xtal, Note 2	-	12.288	-	MHz
BIT_CLK Period	t_{BCP}	24.576MHz Xtal, Note 2	-	81.4	-	ns
BIT_CLK High	t_{BCH}	Note 2	32.56	-	48.84	ns
BIT_CLK Low	t_{BCL}	Note 2	32.56	-	48.84	ns

Timing Specifications (Notes 1, 5) (Continued)

PARAMETER	SYMBOL	TEST CONDITION	HMP9701ACN			UNITS
			MIN	TYP	MAX	
Sync Pulse Frequency			-	48	-	kHz
Sync Period	t_{SP}		-	20.8	-	µs
Sync High	t_{SH}		-	$16*t_{BCP}$	-	µs
Sync Low	t_{SL}		-	$240*t_{BCP}$	-	µs
Setup Time SDATA_OUT, SDATA_IN, SYNC to BIT_CLK	t_{SU}	Note 2	15	-	-	ns
Hold Time SDATA_OUT, SDATA_IN, SYNC to BIT_CLK	t_{HD}		5	-	-	ns
$\overline{\text{RESET}}$ Low Pulse Width (for Cold Reset)	t_{CRL}		1.0	-	-	µs
$\overline{\text{RESET}}$ Inactive to BIT_CLK Start Up (for Cold Reset)	t_{R2BC}		$2*t_{BCP}$	-	-	ns
SYNC Active High Pulse Width (for Warm Reset)	t_{SRH}		-	1.3	-	µs
SYNC Inactive Low to BIT_CLK Start Up (for Warm Reset)	t_{S2BC}		$2*t_{BCP}$	-	-	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low (for AC Link Powerdown)	t_{PDWN}		-	-	1	µs
SDATA_OUT to $\overline{\text{RESET}}$ High (for ATE Test Mode)	t_{SU2RST}		15	-	-	ns
$\overline{\text{RESET}}$ High to Hi-Z (for ATE Test Mode)	t_{HZ}	Note 2	-	-	25	ns

Digital Filter Characteristics (Note 2)

PARAMETER	MIN	TYP	MAX	UNITS
Passband	0	-	0.4xFs	Hz
Transition Band	0.4xFs	-	0.6xFs	Hz
Passband Ripple (0 - 0.4Fs)	-	-	±0.03	dB
Stopband	0.6xFs	-	-	Hz
Stopband Rejection	76	-	-	dB
Group Delay	-	-	18/Fs	s

Analog-to-Digital Converters (Notes 1, 3)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENT
Resolution	-	16	-	Bits	Note 2
Signal-to-Noise					
Line Inputs	-	85	-	dB	
Mic Inputs (Mic Gain = 0dB)	-	85	-	dB	
Total Harmonic Distortion					
Line	-	0.02	-	%	
Mic	-	0.02	-	%	

Analog-to-Digital Converters (Notes 1, 3) **(Continued)**

PARAMETER	MIN	TYP	MAX	UNITS	COMMENT
Interchannel Isolation					
Line/Line	-	80	-	dB	Note 2
Line/Mic	-	80	-	dB	Note 2
Line/Aux	-	80	-	dB	Note 2
Line/Video	-	80	-	dB	Note 2
Gain Error (Full Scale)	-	±5	-	%	
Inter-Channel Gain Mismatch	-	-	±0.5	dB	
Offset Error (0dB Gain)	-	20	200	LSB	
Gain Drift	-	100	-	ppm/^{o}C	Note 2

Digital-to-Analog Converters (Notes 1, 4)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENT
Resolution	16	17	-	Bits	Note 2
Signal-to-Noise	-	87	-	dB	
Total Harmonic Distortion	-	0.02	-	%	
Interchannel Isolation (Line Out)	-	75	-	dB	Note 2
Interchannel Gain Mismatch	-	±0.35	-	dB	
Gain Error	-	-	±5	%	Note 6
Gain Drift	-	100		ppm/^{o}C	Note 2
Total Out of Band Energy (28.8kHz - 100kHz)	-	-	-50	dB	Note 2
Mute Attenuation (0dB)	80	-	-	dB	
Audible Out of Band Energy (20kHz - 28.8kHz)	-	-	-65	dB	Note 2
Deviation from Linear Phase	-	-	1	Degree	Note 2

Programmable Attenuation/Gain (Note 1)

PARAMETER	MIN	TYP	MAX	UNITS
Record Gain (0dB to 22.5dB)	-	22.5	-	dB
Record Gain Step Size	-	1.5 ± 0.2	-	dB
PCM Output Volume Span (+12dB to -34.5dB)	-	46.5	-	dB
PCM Output Volume Span Step Size	-	1.5 ± 0.2	-	dB
Master Volume Span for LINE_OUT, MONO_OUT (0dB to -46.5dB)	-	46.5	-	dB
Master Volume Step Size	-	1.5 ± 0.2	-	dB
Mixer Input Gain Span for LINE_IN, CD, VIDEO, AUX, PHONE, MIC (+12dB to -34.5dB)	-	46.5	-	dB
Mixer Input Gain Step SIze	-	1.5 ± 0.2	-	dB
PC_BEEP Attenuation Span (0dB to 45dB)	-	45	-	dB
PC_BEEP Attenuation Step Size	-	3 ± 0.2	-	dB

Analog Inputs (Note 1)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENT
Full Scale Input Voltages					
MIC Inputs with 0dB Gain	-	2.83 ± 10%	-	V_{PP}	
MIC Inputs with 0dB Gain	-	1.0	-	V_{RMS}	
MIC Inputs with 20dB Gain Enabled	-	0.283 ± 10%	-	V_{PP}	
MIC Inputs with 20dB Gain Enabled	-	0.1	-	V_{RMS}	
LINE_IN, CD, VIDEO, AUX, and PHONE Inputs	-	2.83 ± 10%	-	V_{PP}	
LINE_IN, CD, VIDEO, AUX, and PHONE Inputs	-	1.0	-	V_{RMS}	
Input Impedance	10	-	-	kΩ	Note 2
Input Capacitance	-	15	-	pF	Note 2

Analog Outputs (Note 1)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENT
Full Scale Output Voltages					
LINE_OUT and MONO_OUT	-	2.83 ± 10%	-	V_{PP}	
LINE_OUT and MONO_OUT	-	1.0	-	V_{RMS}	
External Load Impedance	10	-	-	kΩ	
External Load Capacitance	-	-	50	pF	Note 2
V_{REF} Output Voltage	-	2.25 ± 10%	-	V	
V_{REF} Drive Current	-	5	-	mA	
V_{REF} Output Impedance	-	4	-	kΩ	Note 2

NOTES:

1. $T_A = 25^0C$, $V_{AA} = V_{DD} = 5.0V$
2. Guaranteed but not production tested.
3. Based on 1kHz, Full scale analog tone input; Measurement Bandwidth is 20 to 20kHz, A-weighted.
4. DAC's driven with 1kHz, Full Scale PCM Sine Wave, output measurement bandwidth is 20 to 20kHz, A-weighted.
5. Test performed with $C_L = 40pF$, $I_{OL} = 4mA$, $I_{OH} = -4mA$. Input reference level is 1.5V for all inputs. $V_{IH} = 3.0V$, $V_{IL} = 0V$.
6. This is measured relative to a nominal output level.

ADC/DAC Filter Response Curves

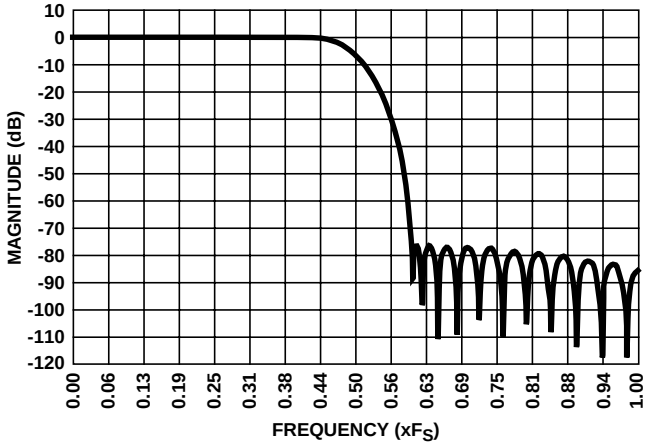


FIGURE 10. ANALOG-TO-DIGITAL FREQUENCY RESPONSE (FULL SCALE LINE INPUTS, 0dB)

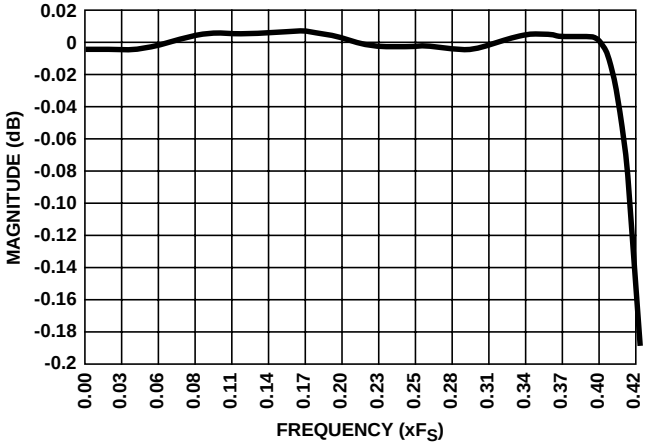


FIGURE 11. ANALOG-TO-DIGITAL PASSBAND FREQUENCY RESPONSE (FULL SCALE LINE INPUTS, 0dB)

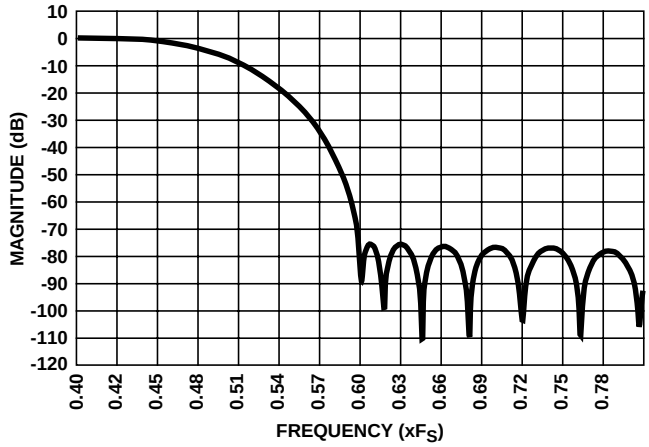


FIGURE 12. ANALOG-TO-DIGITAL TRANSITION BAND FREQUENCY RESPONSE (FULL SCALE LINE INPUTS, 0dB)

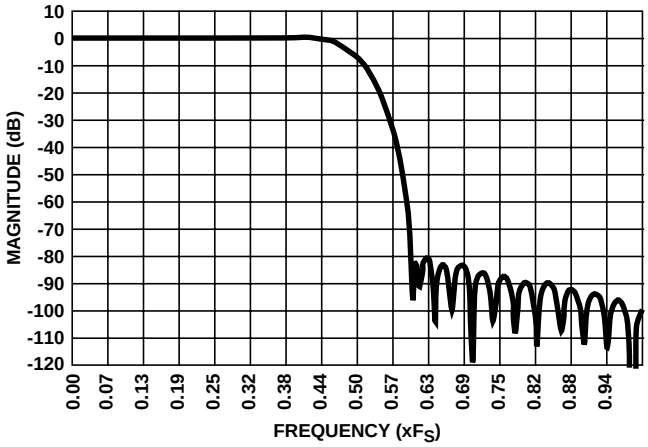


FIGURE 13. DIGITAL-TO-ANALOG FREQUENCY RESPONSE (FULL SCALE INPUTS, 0dB)

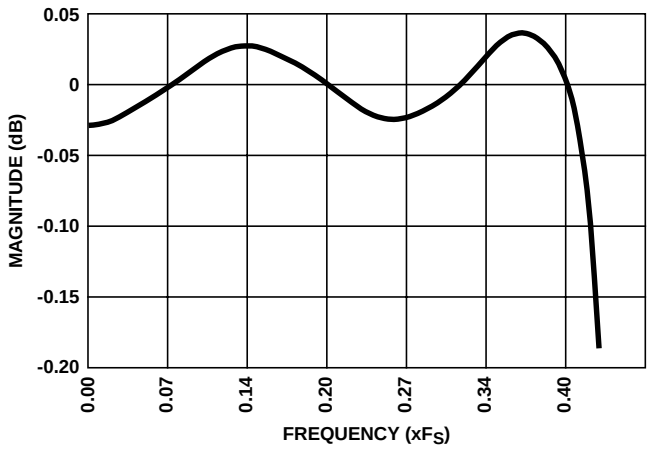


FIGURE 14. DIGITAL-TO-ANALOG PASSBAND FREQUENCY RESPONSE (FULL SCALE INPUTS, 0dB)

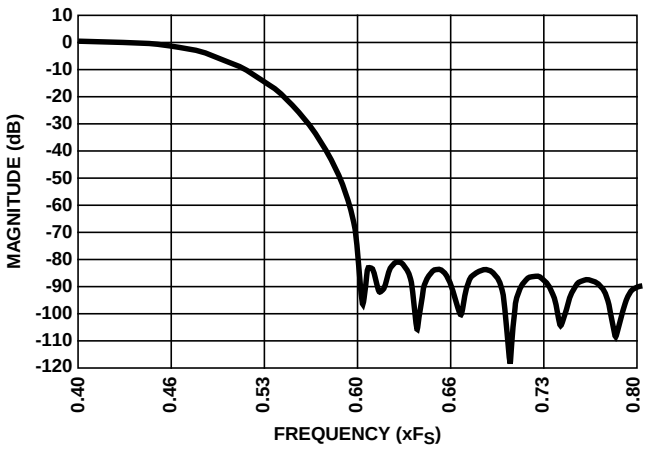


FIGURE 15. DIGITAL-TO-ANALOG TRANSITION BAND FREQUENCY RESPONSE (FULL SCALE INPUTS, 0dB)

AC Timing Waveforms

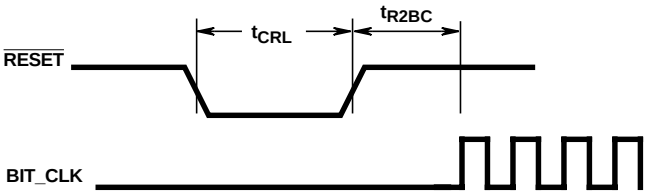


FIGURE 16. COLD RESET TIMING

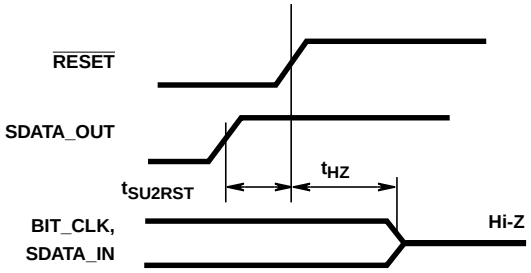


FIGURE 17. ATE TEST MODE

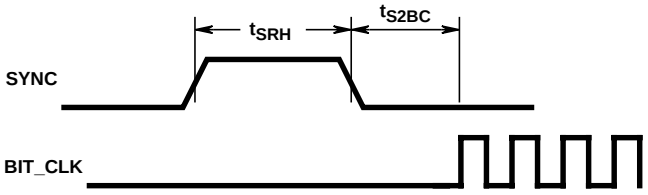


FIGURE 18. WARM RESET TIMING

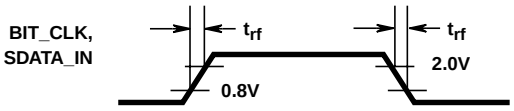


FIGURE 19. RISE AND FALL TIMES

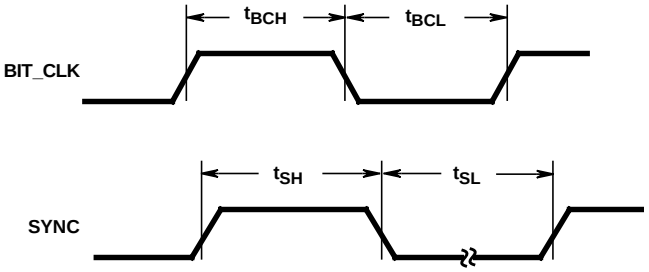
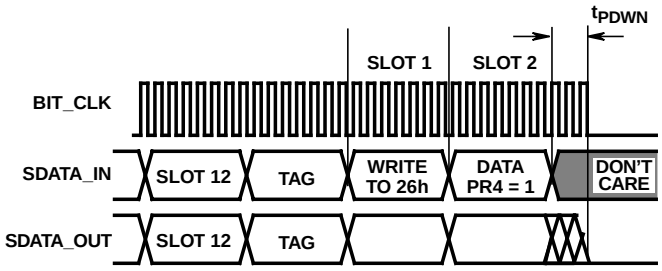


FIGURE 20. CLOCKS



NOTE: BCLK not to scale.

FIGURE 21. POWERDOWN

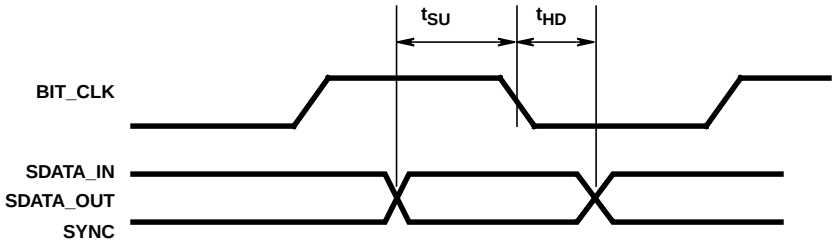
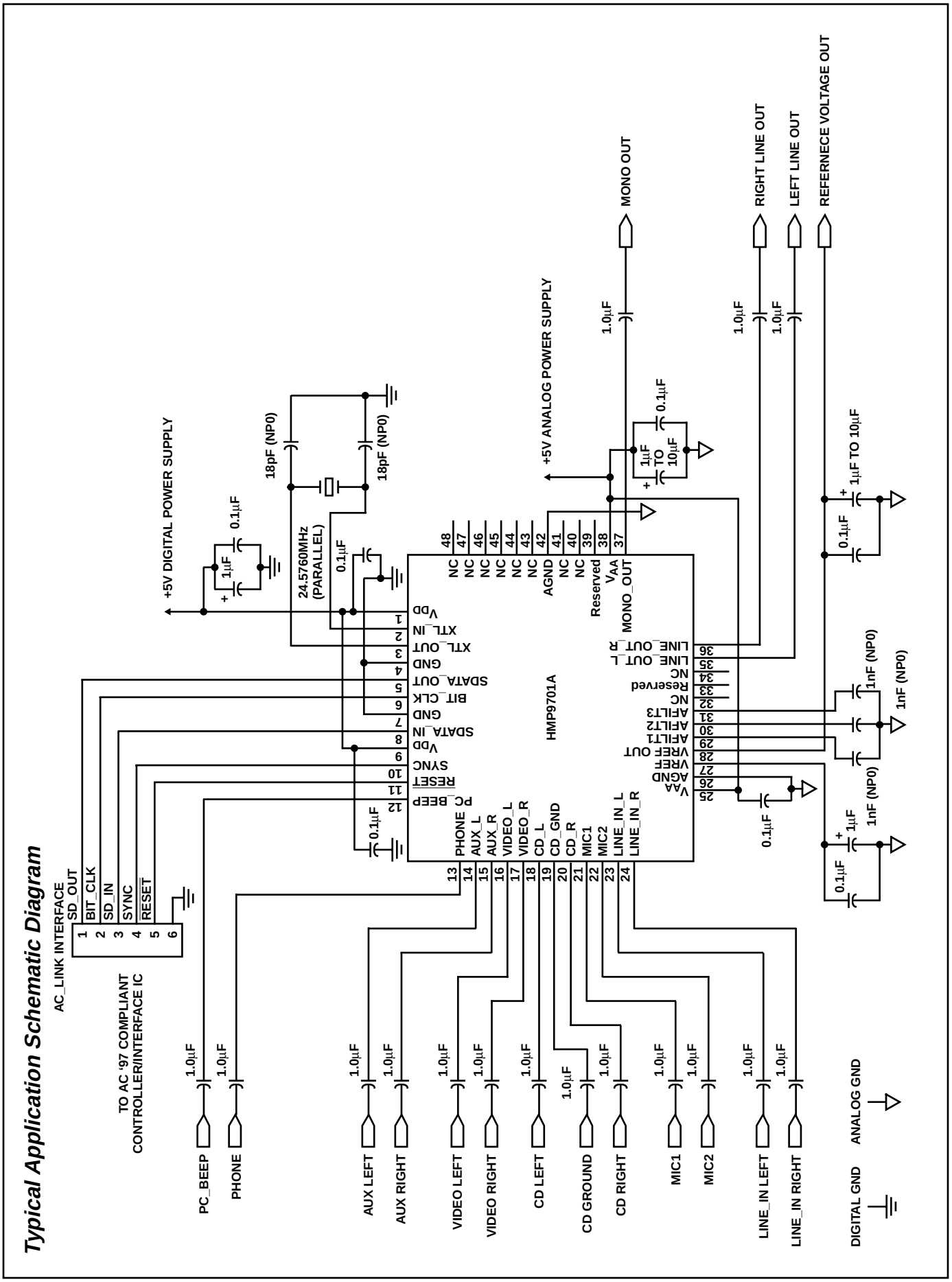


FIGURE 22. DIGITAL SETUP AND HOLD

Typical Application Schematic Diagram



Typical Application Schematic Notes

1. A note about the capacitors used for coupling externally input audio or for outputting audio externally:
   The capacitance value and the associated circuit impedances will determine the lower frequency cutoff of the audio signal. The designer must determine what the circuit impedances are and select the coupling capacitor value accordingly. Ceramic types (over electrolytic) are highly recommended.
2. The crystal should be a parallel resonant type, frequency is 24.756MHz, initial room temperature tolerance of 50ppm, and a load cap of about 16-20pF.
3. It is recommended to decouple each analog and digital power supply pin with a combination of a small value and large value bypass capacitor. The large value capacitor should be either a tantalum or aluminum electrolytic type.
4. Locate all decoupling capacitors CLOSE to their associated pins on the codec.
5. Please note that all analog inputs and outputs of the HMP9701A codec are at the DC level of V_{REF} and require AC coupling to zero biased signal sources and destinations.
6. Keep all analog input and output traces as short as possible, prevent any coupling from adjacent digital lines.
7. For optimum performance, it is preferred to layout separate analog and digital ground planes, joining them together at a point directly adjacent to the codec (i.e., directly under it). This case is true even if the designer is using a single supply for the codec; the single supply should have adequate decoupling/isolation between the digital and analog sections.
8. When using an external clock source, please feed that signal into the XTL_IN pin and leave the XTL_OUT pin unconnected. Also, do not use any capacitors between XTL_IN and GND or XTL_OUT and GND in that mode.