

Linear Systems Ultra Low Leakage Low Drift Monolithic Dual JFET

The LS842 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LS842 features a 25-mV offset and 40- $\mu\text{V}/^\circ\text{C}$ drift.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS842 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

| FEATURES | | |
|--|---|----------------|
| LOW DRIFT | $ V_{GS1-2}/T \leq 40\mu\text{V}/^\circ\text{C}$ | |
| LOW LEAKAGE | $I_G = 10\text{pA TYP.}$ | |
| LOW NOISE | $e_n = 8\text{nV}/\sqrt{\text{Hz}}$ TYP. | |
| LOW OFFSET VOLTAGE | $ V_{GS1-2} \leq 25\text{mV}$ | |
| ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted) | | |
| Maximum Temperatures | | |
| Storage Temperature | -65°C to +150°C | |
| Operating Junction Temperature | +150°C | |
| Maximum Voltage and Current for Each Transistor – Note 1 | | |
| -V _{GSS} | Gate Voltage to Drain or Source | 60V |
| -V _{DSO} | Drain to Source Voltage | 60V |
| -I _{G(f)} | Gate Forward Current | 50mA |
| Maximum Power Dissipation | | |
| Device Dissipation @ Free Air – Total | | 400mW @ +125°C |

| MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED | | | | |
|--|-----------------------|-------|------------------------------|--|
| SYMBOL | CHARACTERISTICS | VALUE | UNITS | CONDITIONS |
| $ V_{GS1-2}/T \text{ max.}$ | DRIFT VS. TEMPERATURE | 40 | $\mu\text{V}/^\circ\text{C}$ | $V_{DG}=20\text{V}, I_D=200\mu\text{A}$ $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$ |
| $ V_{GS1-2} \text{ max.}$ | OFFSET VOLTAGE | 25 | mV | $V_{DG}=20\text{V}, I_D=200\mu\text{A}$ |

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

| SYMBOL | CHARACTERISTICS | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|--|-------------------------------|------|------|------|------------------------|---|
| BV _{GSS} | Breakdown Voltage | 60 | 60 | -- | V | $V_{DS} = 0$ $I_D = 1\text{nA}$ |
| BV _{GGO} | Gate-To-Gate Breakdown | 60 | -- | -- | V | $I_G = 1\text{nA}$ $I_D = 0$ $I_S = 0$ |
| TRANSCONDUCTANCE | | | | | | |
| Y _{FSS} | Full Conduction | 1000 | -- | 4000 | μmho | $V_{DG} = 20\text{V}$ $V_{GS} = 0\text{V}$ $f = 1\text{kHz}$ |
| Y _{FS} | Typical Operation | 500 | -- | 1000 | μmho | $V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$ |
| $ Y_{FS1-2}/Y_{FS} $ | Mismatch | -- | 0.6 | 3 | % | |
| DRAIN CURRENT | | | | | | |
| I _{DSS} | Full Conduction | 0.5 | 2 | 5 | mA | $V_{DG} = 20\text{V}$ $V_{GS} = 0\text{V}$ |
| $ I_{DSS1-2}/I_{DSS} $ | Mismatch at Full Conduction | -- | 1 | 5 | % | |
| GATE VOLTAGE | | | | | | |
| V _{GS(off)} or V _p | Pinchoff voltage | 1 | 2 | 4.5 | V | $V_{DS} = 20\text{V}$ $I_D = 1\text{nA}$ |
| V _{GS(on)} | Operating Range | 0.5 | -- | 4 | V | $V_{DS} = 20\text{V}$ $I_D = 200\mu\text{A}$ |
| GATE CURRENT | | | | | | |
| -I _G max. | Operating | -- | 10 | 50 | pA | $V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$ |
| -I _G max. | High Temperature | -- | -- | 50 | nA | $T_A = +125^\circ\text{C}$ |
| -I _G max. | Reduced V _{DG} | -- | 5 | -- | pA | $V_{DG} = 10\text{V}$ $I_D = 200\mu\text{A}$ |
| -I _{GSS} max. | At Full Conduction | -- | -- | 100 | pA | $V_{DG} = 20\text{V}, V_{DS} = 0$ |
| OUTPUT CONDUCTANCE | | | | | | |
| Y _{OSS} | Full Conduction | -- | -- | 10 | μmho | $V_{DG} = 20\text{V}$ $V_{GS} = 0\text{V}$ |
| Y _{OS} | Operating | -- | 0.1 | 1 | μmho | $V_{DG} = 20\text{V}$ $I_D = 200\mu\text{A}$ |
| $ Y_{OS1-2} $ | Differential | -- | 0.01 | 0.1 | μmho | |
| COMMON MODE REJECTION | | | | | | |
| CMR | $-20 \log V_{GS1-2}/V_{DS} $ | -- | 100 | -- | dB | $\Delta V_{DS} = 10$ to 20V $I_D = 200\mu\text{A}$ |
| | $-20 \log V_{GS1-2}/V_{DS} $ | -- | 75 | -- | dB | $\Delta V_{DS} = 5$ to 10V $I_D = 200\mu\text{A}$ |
| NOISE | | | | | | |
| NF | Figure | -- | -- | 0.5 | dB | $V_{DS} = 20\text{V}$ $V_{GS} = 0\text{V}$ $R_G = 10\text{M}\Omega$ $f = 100\text{Hz}$ $\text{NBW} = 6\text{Hz}$ |
| e _n | Voltage | -- | -- | 10 | nV/ $\sqrt{\text{Hz}}$ | $V_{DS} = 20\text{V}$ $I_D = 200\mu\text{A}$ $f = 1\text{kHz}$ $\text{NBW} = 1\text{Hz}$ |
| | | -- | -- | 15 | | $V_{DS} = 20\text{V}$ $I_D = 200\mu\text{A}$ $f = 10\text{Hz}$ $\text{NBW} = 1\text{Hz}$ |
| CAPACITANCE | | | | | | |
| C _{ISS} | Input | -- | 4 | -- | pF | $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$ |
| C _{RSS} | Reverse Transfer | -- | 1.2 | 5 | | |
| C _{DD} | Drain-to-Drain | -- | 0.1 | -- | | |

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS842 / LS842 in PDIP & SOIC
LS842 / LS842 available as bare die
Please contact [Micross](http://www.micross.com) for full package and die dimensions

PDIP & SOIC (Top View)

