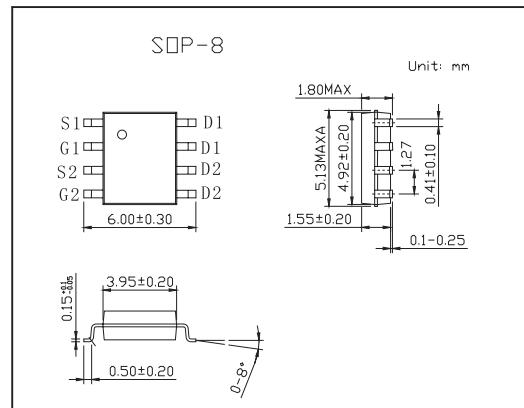
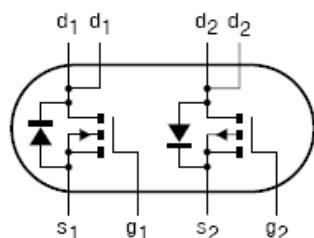


KHC21025

■ Features

- High-speed switching
- No secondary breakdown
- Very low on-resistance.



■ Absolute Maximum Ratings Ta = 25°C

Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain to Source Voltage	V _{DSS}	30	-30	V	
Gate to Source Voltage	V _{GSS}	±20	±20	V	
Drain Current Ts ≤ 80°C	I _D	3.5	-2.3	A	
peak drain current *1	I _{DM}	14	-10	A	
total power dissipation Ts = 80°C; *2	P _{tot}	2	W		
T _{amb} = 25 °C; *3					
T _{amb} = 25°C; *4					
T _{amb} = 25 °C; *5					
storage temperature	T _{stg}	-65 to 150		°C	
operating junction temperature	T _j	150		°C	
source current (DC) Ts ≤ 80 °C	I _S	1.5	-1.25	A	
peak pulsed source current *1	I _{SM}	6	-5	A	
thermal resistance from junction to soldering point	R _{th j-s}	35		K/W	

*1 Pulse width and duty cycle limited by maximum junction temperature.

*2 Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.

*3 Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an R_{th a-tp} (ambient to tie-point) of 27.5 K/W.

*4 Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an R_{th a-tp} (ambient to tie-point) of 90 K/W.

*5 Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an R_{th a-tp} (ambient to tie-point) of 90 K/W.

KHC21025

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Type	Min	Typ	Max	Unit
drain-source breakdown voltage	V(BR)DSS	V _{GS} = 0; Id = 10 mA	N-Ch	30			V
		V _{GS} = 0; Id = -10 mA	P-Ch	-30			V
gate-source threshold voltage	V _{Gsth}	V _{GS} = V _{DS} ; Id = 1 mA	N-Ch	1		2.8	V
		V _{GS} = V _{DS} ; Id = -1 mA	P-Ch	-1		-2.8	V
drain-source leakage current	I _{DSS}	V _{GS} = 0; V _{DS} = 24 V	N-Ch			100	nA
		V _{GS} = 0; V _{DS} = -24 V	P-Ch			-100	nA
gate leakage current	I _{GSS}	V _{GS} = ±20 V; V _{DS} = 0	N-Ch			±100	nA
			P-Ch			±100	nA
on-state drain current	I _{DOn}	V _{GS} = 10 V; V _{DS} = 1 V	N-Ch	3.5			A
		V _{GS} = 4.5 V; V _{DS} = 5 V		2			A
		V _{GS} = -10 V; V _{DS} = -1 V	P-Ch	-2.3			A
		V _{GS} = -4.5 V; V _{DS} = -5 V		-1			A
drain-source on-state resistance	R _{Dson}	V _{GS} = 4.5 V; Id = 1 A	N-Ch		0.11	0.2	Ω
		V _{GS} = 10 V; Id = 2.2 A			0.08	0.1	Ω
		V _{GS} = -4.5 V; Id = -0.5 A	P-Ch		0.33	0.4	Ω
		V _{GS} = -10 V; Id = -1 A			0.22	0.25	Ω
forward transfer admittance	Y _{fs}	V _{DS} = 20 V; Id = 2.2 A	N-Ch	2	4.5		S
		V _{DS} = -20 V; Id = -1 A	P-Ch	1	2		S
input capacitance	C _{iss}	V _{GS} = 0; V _{DS} = 20 V; f = 1 MHz	N-Ch		250		pF
		V _{GS} = 0; V _{DS} = -20 V; f = 1 MHz	P-Ch		250		pF
output capacitance	C _{oss}	V _{GS} = 0; V _{DS} = 20 V; f = 1 MHz	N-Ch		140		pF
		V _{GS} = 0; V _{DS} = -20 V; f = 1 MHz	P-Ch		140		pF
reverse transfer capacitance	C _{rss}	V _{GS} = 0; V _{DS} = 20 V; f = 1 MHz	N-Ch		50		pF
		V _{GS} = 0; V _{DS} = -20 V; f = 1 MHz	P-Ch		50		pF
total gate charge	Q _G	V _{GS} = 10 V; V _{DS} = 15 V; Id = 2.3 A	N-Ch		10	30	nC
		V _{GS} = -10 V; V _{DS} = -15 V; Id = -2.3 A	P-Ch		10	25	nC
gate-source charge	Q _{GS}	V _{GS} = 10 V; V _{DS} = 15 V; Id = 2.3 A	N-Ch		1		nC
		V _{GS} = -10 V; V _{DS} = -15 V; Id = -2.3 A	P-Ch		1		nC
gate-drain charge	Q _{GD}	V _{GS} = 10 V; V _{DS} = 15 V; Id = 2.3 A	N-Ch		2.5		nC
		V _{GS} = -10 V; V _{DS} = -15 V; Id = -2.3 A	P-Ch		3		nC
turn-on time	t _{on}	V _{GS} = 0 to 10 V; V _{DD} = 20 V; Id = 1 A; R _L = 20 Ω	N-Ch		15	40	ns
		V _{GS} = 0 to -10 V; V _{DD} = -20 V; Id = -1 A; R _L = 20 Ω	P-Ch		20	80	ns
turn-off time	t _{off}	V _{GS} = 10 to 0 V; V _{DD} = 20 V; Id = 1 A; R _L = 20 Ω	N-Ch		25	140	ns
		V _{GS} = -10 to 0 V; V _{DD} = -20 V; Id = -1 A; R _L = 20 Ω	P-Ch		50	140	ns
source-drain diode forward voltage	V _{SD}	V _{GD} = 0; Is = 1.25 A	N-Ch			1.2	V
		V _{GD} = 0; Is = -1.25 A	P-Ch			-1.6	V
reverse recovery time	t _{rr}	I _s = 1.25 A; dI/dt = 100 A/μs	N-Ch		35	100	ns
		I _s = -1.25 A; dI/dt = 100 A/μs	P-Ch		150	200	ns