I^{2}C Clock Generator for Pentium® Notebook Designs.

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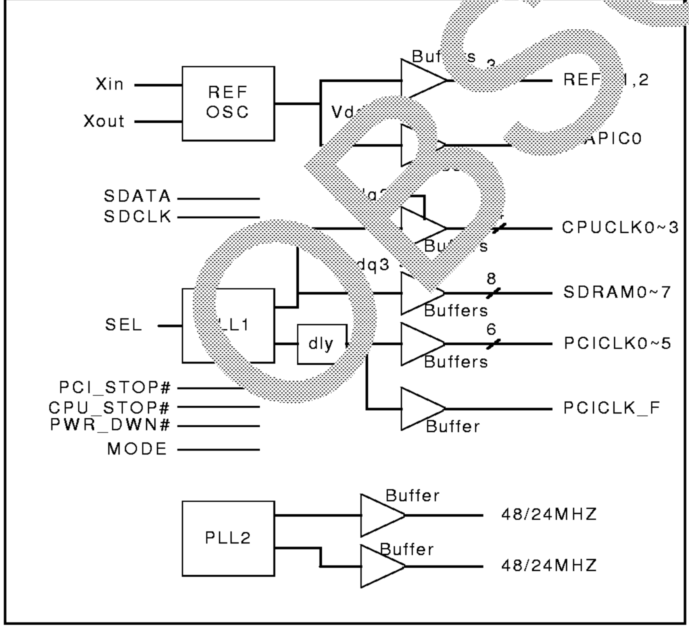
PRODUCT FEATURES

- Supports Pentium® & Pro CPUs.
- 4 CPU clocks up to 8 loads.
- Up to 8 SDRAM clocks for 2 DIMs.
- Supports Power Savings Frequencies.
- 7 PCI synchronous clocks.
- Optional common or mixed supply mode:
- (Vdd = Vddq3 = Vddq2 = 3.3V) or
- (Vdd = Vddq3 = 3.3V, Vddq2 = 2.5V)
- < 250ps skew CPU and SDRAM clocks.
- < 250ps skew among PCI clocks.
- I^{2}C 2-Wire serial interface
- Programmable registers featuring:
  - enable/disable each output pin
  - mode as tri-state, test, or normal
  - 24/48 MHz selections
- 1 IOAPIC clock for multiprocessor support.
- 48-pin SSOP package

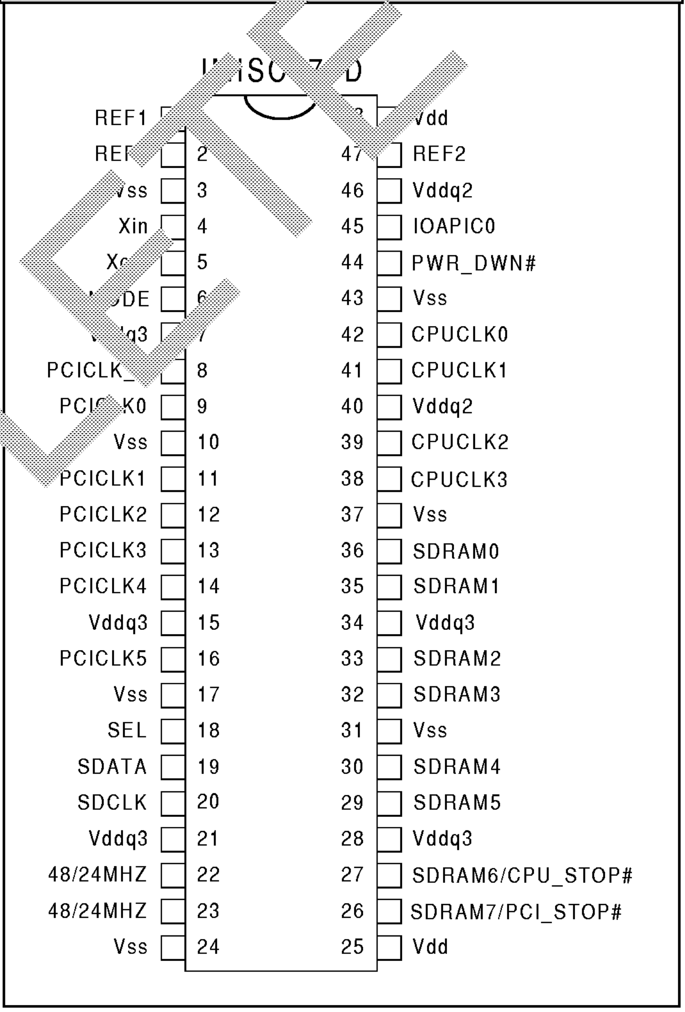
BLOCK DIAGRAM



FREQUENCY TABLE

SEL	CPU	PCI
0	60.0	30.0
1	66.6	33.3

CONNECTION DIAGRAM



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PIN DESCRIPTION

Xin, Xout - These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal (nominally 14.318 MHz). Xin may also serve as input for an externally generated reference signal.

SEL - Standard frequency select input. It has internal pull-up.

CPUCLK(0:3) - Low skew (<250 pS) clock outputs for host frequencies such as CPU, Chipset, Cache. Vddq2 is the supply voltage for these outputs.

SDRAM(0:5) - Synchronous DRAM DIMs clocks. They are powered by Vddq3.

SDRAM6/CPU_STOP# - If MODE=1, this pin is a Synchronous DRAM DIMs clock output powered by Vddq3. If MODE=0, this pin is a CPU_STOP# input signal, where a low level stops the CPU however, the SDRAM clocks will stay active. It has an internal pull-up.

SDRAM7/PCI_STOP# - If MODE=1, this pin is a Synchronous DRAM DIMs clock output powered by Vddq3. If MODE=0, this pin is a PCI_STOP# input signal, where a low level stops the PCI clocks except the PCI_F. It has an internal pull-up.

MODE - A low level on this pin causes pins 26, and 27 to be power management inputs PCI_STOP#, and CPU_STOP# respectly. A high level on this pin causes pins 26, and 27 to be clock output signals SDRAM7, and SDRAM6 respectively. It has an internal pull-up resistor.

PCICLK(0:5) - Low skew (<250pS) clock outputs for PCI frequencies. These buffers voltage level is controlled by Vddq3

PCICLK_F - A PCI clock output that does not stop until in power down mode. It is synchronous with other PCI clocks.

REF(0:2) - Buffered outputs of 14.3 MHz on-chip reference.

IOAPIC0 - Buffered output of 14.3MHZ for multiprocessor support. It is powered by Vddq2.

PWR_DWN# - Power down pin. When this pin is asserted low, the IC is in shutdown mode where all circuitry is turned off including VCO, crystal buffer and PCICLK_F. It has an internal pull-up. The I^2C interface is disabled with the PWR_DWN# pin is low.

48/24MHz(0:1) - Programmable 48 MHZ or 24 MHZ clock outputs.

SDATA - serial data of I^2C 2-wire control interface. Has internal pull-up resistor.

SDCLK - serial clock of I^2C 2-wire control interface. Has internal pull-up resistor.

Vss - Ground pins for the chip.

Vdd - 3.3 Volt power supply pins for analog circuit and core logic.

Vddq3 - Power supply pins for 3.3V IO pins.

Vddq2 - Power supply pins for 2.5V/3.3V IO pins.

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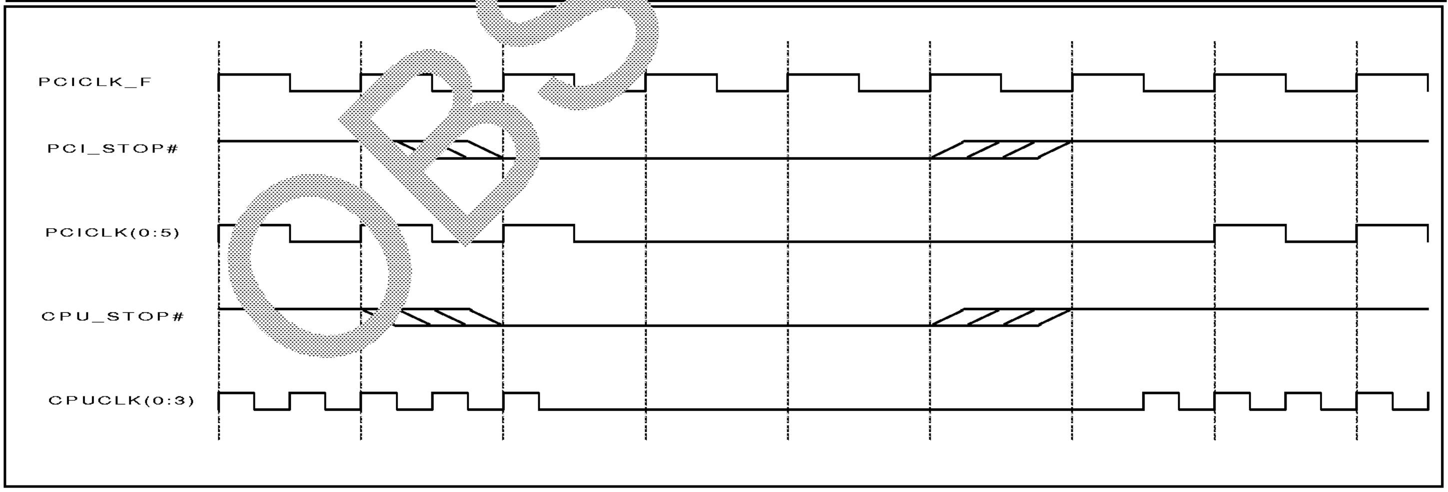
POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or stopped via the 2-wire control interface. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, the VCOs will stabilize to the correct pulse widths within about 0.2 mS. The CPU, SDRAM, and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

When MODE=0, pins 26 and 27 are inputs PCI_STOP# and CPU_STOP# respectively (when MODE=1, these functions are not available). A particular output is enabled only when both the serial interface and these pins indicate that it should be enabled. The IMISC671 clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped. On low to high transitions of PWR_DWN#, external circuitry should allow 0.2 mS for the VCOs to stabilize prior to assuming the clock periods are correct. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCICLK_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	OTHER CLKs	XTAL & VCOs
X	X	0	LOW	LOW	LOW	OFF
0	0	1	LOW	LOW	RUNNING	RUNNING
0	1	1	LOW	33/30 MHZ	RUNNING	RUNNING
1	0	1	66/60 MHZ	LOW	RUNNING	RUNNING
1	1	1	66/60 MHZ	33/30 MHZ	RUNNING	RUNNING

POWER MANAGEMENT TIMING



2-WIRE I^2C CONTROL INTERFACE

The 2-wire control interface implements a write only slave interface. The IMISC671D cannot be read back. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. It also allows 24/48 MHZ frequency selection and test mode enable.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit as the LSB. Data is transferred MSB first.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions. The I^2C interface is disabled when the PWR_DWN# pin is low. Previously set control registers are retained.

SERIAL CONTROL REGISTERS

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (D2), two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

Byte 0: Function Select Register

Bit	@Pup	Pin#	Description
7	0	*	Reserved, Don't set
6	0	*	Reserved, Don't set
5	0	*	Reserved, Don't set
4	0	*	Reserved, Don't set
3	1	23	48/24 Mhz (See note 1)
2	1	22	48/24 Mhz (See note 1)
1 0	0 0		Bit1 Bit0 1 1 Tri-State 1 0 Reserved 0 1 Test Mode 0 0 Normal

Note 1: Bits 3 and 2 are for selecting the function of pins 23 and 22 respectively. If these bits are set to "1" (default), the outputs will be 48 Mhz. If they are set to "0" the outputs are 24 MHz.

IMPORTANT NOTE

Reserved bits are intended for possible future functions. It is important that they be left at thie Power Up logic levels at all times. Otherwise data sheet specifications cannot be guaranteed.

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SERIAL CONTROL REGISTERS (Cont.)

Function Table

Function Description	Outputs						
	CPU	PCI	SDRAM	Ref	IOAPIC	24MHZ	48MHZ
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	Tclk/2	Tclk/4	Tclk/2	Tclk	Tclk	Tclk/4	Tclk/2
Normal SEL=1	66	CPU/2	CPU	14.318	14.318	24	48
Normal SEL=0	60	CPU/2	CPU	14.318	14.318	24	48

Notes:

1. Tclk is a test clock over driven on the Xin input during test mode.
2. The frequency ratio Fout/Fin for the USB output is 3.35294.

<u>Byte 1</u>: CPU, 48/24 MHz Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	23	48/24 MHz enable/Stopped
6	1	22	48/24 MHz enable/Stopped
5	x	-	Reserved
4	x	-	Reserved
3	1	38	CPUCLK3 enable/Stopped
2	1	39	CPUCLK2 enable/Stopped
1	1	41	CPUCLK1 enable/Stopped
0	1	42	CPUCLK0 enable/Stopped

<u>Byte 2</u>: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	1	8	PCICLK_F enable/Stopped
5	1	16	PCICLK5 enable/Stopped
4	1	14	PCICLK4 enable/Stopped
3	1	13	PCICLK3 enable/Stopped
2	1	12	PCICLK2 enable/Stopped
1	1	11	PCICLK1 enable/Stopped
0	1	9	PCICLK0 enable/Stopped

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SERIAL CONTROL REGISTERS(Continued)

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	SDRAM7 enable/Stopped
6	1	27	SDRAM6 enable/Stopped
5	1	29	SDRAM5 enable/Stopped
4	1	30	SDRAM4 enable/Stopped
3	1	32	SDRAM3 enable/Stopped
2	1	33	SDRAM2 enable/Stopped
1	1	35	SDRAM1 enable/Stopped
0	1	36	SDRAM0 enable/Stopped

Byte 4: Additional SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	1	-	Reserved
4	1	45	IOAPIC0 enable/Stopped
3	x	-	Reserved
2	1	47	REF2 enable/Stopped
1	1	1	REF1 enable/Stopped
0	1	2	REF0 enable/Stopped

SERIAL CONTROL REGISTERS(Continued)

<u>Byte 6</u>: Reserved Register

Bit	@Pup	Pin#	Description
7	x	-	Reserved
6	x	-	Reserved
5	x	-	Reserved
4	x	-	Reserved
3	x	-	Reserved
2	x	-	Reserved
1	x	-	Reserved
0	x	-	Reserved

<u>Byte 7</u>: Frequency Control

If the three LSBs of this register are 111 (as at power up), the frequency is controlled by the SEL package pin. Note that if this pin is open, the internal pull-up will select [illegible] MHz. Otherwise, the CPU clock frequency is controlled by F_SEL(0:2).

Bit	@Pup	Description
7	x	Reserved
6	x	Reserved
5	x	Reserved
4	x	Reserved
3	x	Reserved
2	1	F_SEL2
1	1	F_SEL1
0	1	F_SEL0

FSEL2	FSEL1	FSEL0	FREQUENCY
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	33 MHz
1	0	0	50 MHz
1	0	1	55 MHz
1	1	0	60 MHz
1	1	1	From SEL pin

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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V
Voltage Relative to VDD:	0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL			-66	µA	
Input High Current	IIH			5	µA	
Output Low Voltage IOL = 4mA	VOL	-	-	0.4	Vdc	All Outputs (see buffer spec)
Output High Voltage IOH = 4mA	VOH	2.4	-	-	Vdc	All Outputs Using 3.3V Power (see buffer spec)
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd	-	-	100	mA	CPU = 66.6 MHz, PCI = 33.3 MHz
Static Supply Current	Isdd	-	-	750	µA	Powered Down = Active
Short Circuit Current	ISC	25	-	-	mA	1 output at a time - 30 seconds

VDD = VDDQ3 =3.3V ±5%, ***VDDQ2 = 2.5V***±5% , ***TA = 0ºC to +70ºC***

SWITCHING CHARACTERISTICS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V
CPU to PCI Offset	tOFF	1	-	4	ns	15 pf Load Measured at 1.5V
Buffer out Skew All CPU and PCI Buffer Outputs	tSKEW	-	-	250	ps	15 pf Load Measured at 1.5V
ΔPeriod Adjacent Cycles	ΔP	-	-	±250	ps	-
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Overshoot/Undershoot Beyond Power Rails	V_{over}	-	-	1.5	V	22 ohms @ source of 8 inch PCB run to 15 pf load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	note1
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5V±5% , TA = 0ºC to +70ºC						

note 1: Ring Back must not enter this range.

TB4LB TYPE BUFFER CHARACTERISTICS FOR CPUCLK(0:3), IOAPIC AND SDRAM (0:7)						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	22		[illegible]	mA	Vout = VDDQ2 -.5V
Pull-Up Current	IOH	[illegible]	-	56	mA	Vout = 1.25V
Pull-Down Current	IOL	30	-	41	mA	Vout = 0.4V
Pull-Down Current	IOL	75		102	mA	Vout = 1.2V
Rise/Fall Time Min Between 0.4 V and 2.0 V	TRF_{min}	[illegible]			nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	TRF_{max}			2.0	nS	20 pF Load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5V±5% , TA = 0ºC to +70ºC						

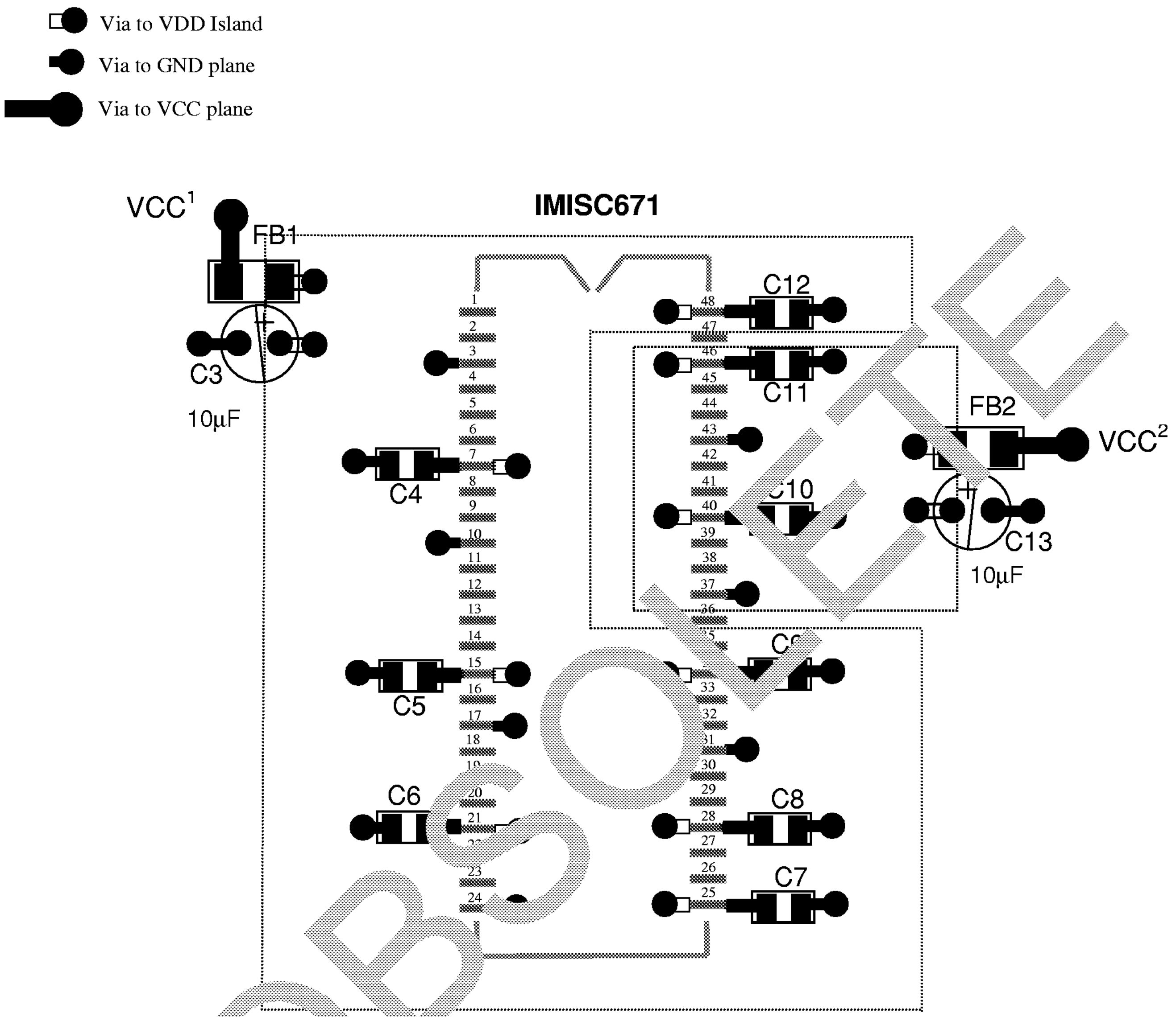
TB5L1 TYPE BUFFER CHARACTERISTICS FOR REF(1:2) and 48/24 MHz						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	13	-	17	mA	Vout = VDD-0.5V
Pull-Up Current	IOH	30	-	44	mA	Vout 1.5V
Pull-Down Current	IOL	13	-	19	mA	Vout = 0.4V
Pull-Down Current	IOL	32	-	44	mA	Vout = 1.5V
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	1.0	-	-	nS	10 pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	2.0	nS	20 pF Load
VDD = VDDQ3 =3.3V ±5%, VDDQ2 = 2.5V±5% , TA = 0ºC to +70ºC						

TB4L1 TYPE BUFFER CHARACTERISTICS FOR PCICLK (0:5, F), REF0						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Pull-Up Current	IOH	18	-	23	mA	Vout = VDD -.5V
Pull-Up Current	IOH	44	-	64	mA	Vout = 1.5
Pull-Down Current	IOL	18	-	25	mA	Vout = 0.4
Pull-Down Current	IOL	50	-	70	[illegible]	Vout = 1.5
Rise/Fall Time Min Between 0.4 V and 2.4 V	TRF_{min}	0.5	-	-	nS	[illegible] pF Load
Rise/Fall Time Max Between 0.4 V and 2.4 V	TRF_{max}	-	-	[illegible]	nS	30 pF Load
VDD = VDDQ3 =3.3V ±5%, VDD[illegible] = 2.5V±5% , TA = 0ºC to +70ºC						

CRYSTAL AND REFERENCE OSCILLATOR PARAMETERS						
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Frequency	F_o	12.00	14.31818	16.00	[illegible]	
Tolerence	TC	-	-	[illegible]100	PPM	Calibration note 1
	TS	-	-	+/-[illegible]	PPM	Stability (Ta -10 to +60C) note 1
	TA	-	[illegible]	[illegible]5	PPM	Aging (first year @ 25C) note 1
Mode	OM	-	[illegible]	-		Parallell Resonant
Pin Capacitance	CP		6		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	[illegible]	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	[illegible]0	-	pF	the crystals rated load. note 1
Effective Series resonant resistance	R[illegible]	-	-	40	Ohms	
Power Dissipation	DL	[illegible]	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	crystals internal package capacitance (total)
For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors. Budgeting Calculations Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore 2.0 pF Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore 3.0 pF External crystal loading capacitors (connect to ground) 15.0 pF the total parasitic capacitance would therefore be = 20.0.0 pF.						

Note 1: It is recommended but not manditory that a crystal meets these specifications.

PCB LAYOUT SUGGESTION



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C4, C5, C6, C7, C8, C9, C10, C11and C12 (all are 0.1µf) should always be used and placed close to their VDD pins.

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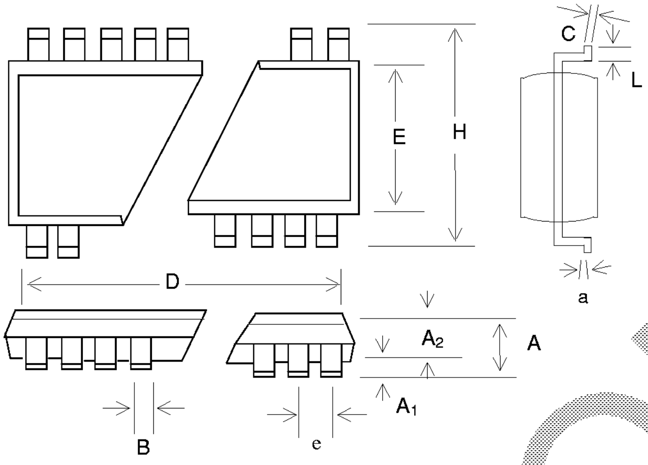
PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	[illegible]	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	0.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
[illegible]	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

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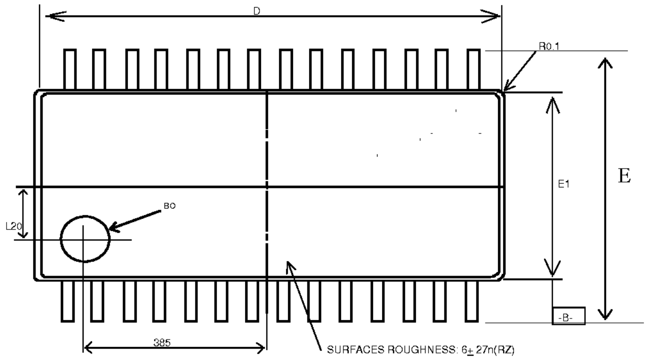
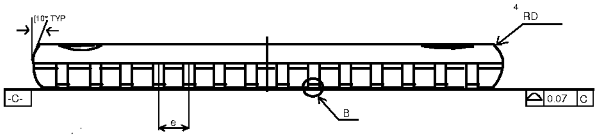
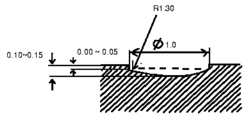
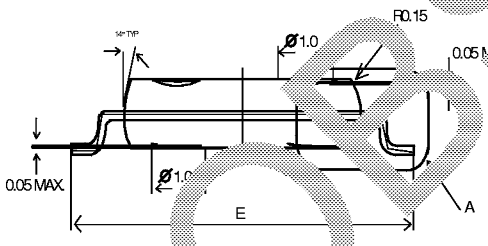
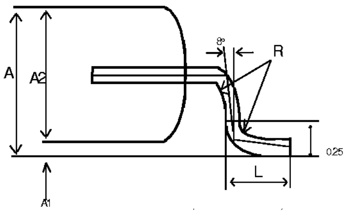




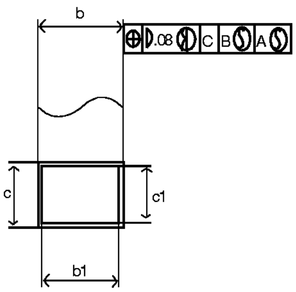


SECTION V-V





DETAIL A



DETAIL B

48 PIN TSSOP DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.0433	-	-	1.10
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.033	0.035	0.037	0.85	0.90	0.95
L	0.019	0.023	0.029	0.50	0.60	0.75
R	0.043	-	-	0.10	-	-
b	0.006	-	0.010	0.170	-	0.27
b1	0.006	0.008	0.009	0.170	0.20	0.225
c	0.004	-	0.007	0.105	-	0.175
c1	0.004	0.005	0.006	0.105	0.125	0.145
θ	0°	-	8°	0°	-	8°
e	0.020 BSC			0.50 BSC		
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.313	0.319	0.325	7.95	8.1	8.25
E1	0.236	0.240	0.244	6.00	6.1	6.20

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ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMISC671DYB	48 PIN SSOP	Commercial, 0ºC to +70ºC
IMISC671DTB	48 PIN TSSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
SC671DYB
Date Code, Lot #

IMISC671DYB

Flow
B = Commercial, 0ºC to + 70ºC

Package
Y = SSOP
T = TSSOP

Revision

IMI Device Number