
HM51W16165 Series

HM51W18165 Series

16 M EDO DRAM (1-Mword $\times$ 16-bit)
4 k Refresh/1 k Refresh

HITACHI

ADE-203-650D (Z)
Rev. 4.0
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Description

The Hitachi HM51W16165 Series, HM51W18165 Series are CMOS dynamic RAMs organized as 1,048,576-word $\times$ 16-bit. They employ the most advanced CMOS technology for high performance and low power. HM51W16165 Series, HM51W18165 Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They have package variations of standard 400-mil 42-pin plastic SOJ and 400-mil 50-pin plastic TSOP.

Features

- Single 3.3 V (± 0.3 V)
- Access time: 50 ns/60 ns/70 ns (max)
- Power dissipation
 - Active mode : 396 mW/360mW/324 mW (max) (HM51W16165 Series)
: 684 mW /612 mW /540 mW (max) (HM51W18165 Series)
 - Standby mode : 7.2 mW (max)
: 0.54 mW (max) (L-version)
- EDO page mode capability
- Refresh cycles
 - 4096 refresh cycles : 64 ms (HM51W16165 Series)
: 128 ms (L-version)
 - 1024 refresh cycles : 16 ms (HM51W18165 Series)
: 128 ms (L-version)
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)
- 2CAS-byte control
- Battery backup operation (L-version)

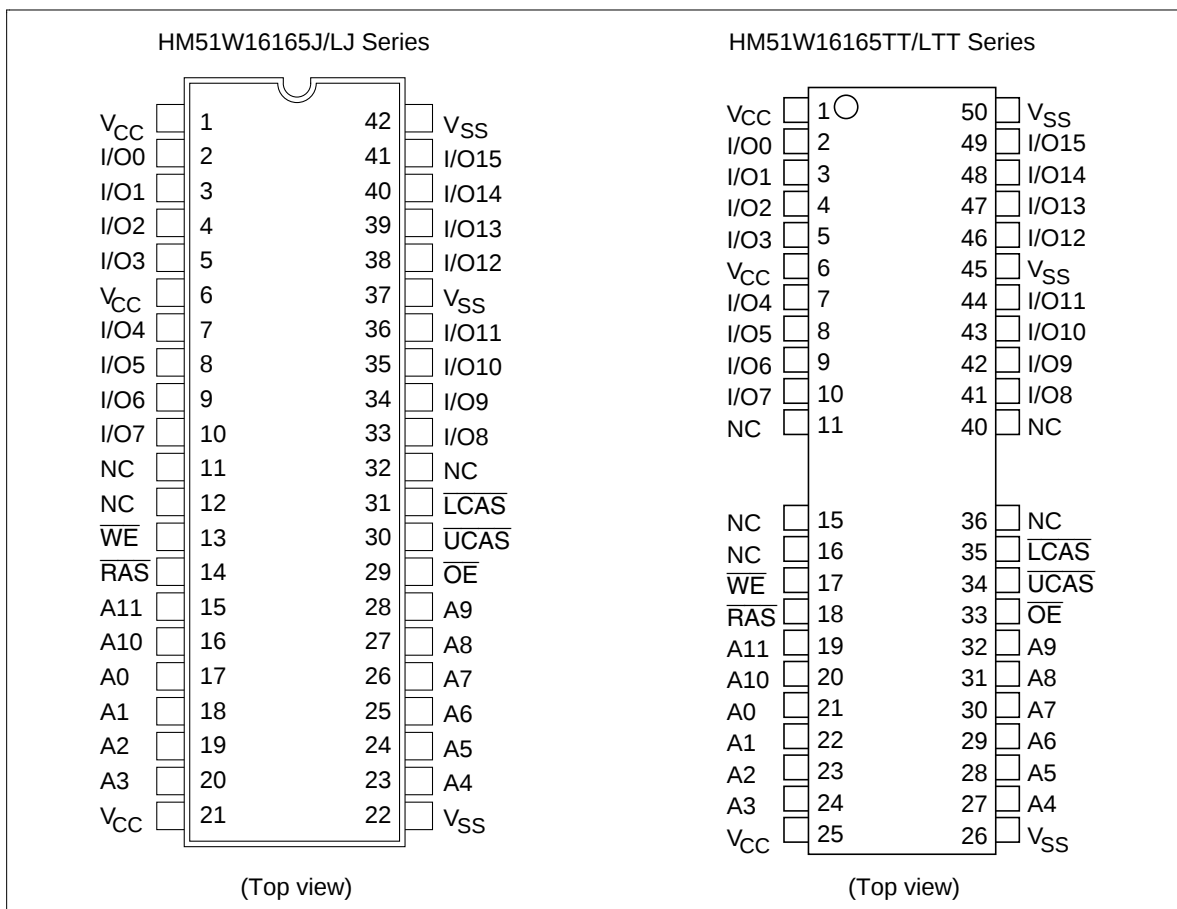
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Ordering Information

Type No.	Access time	Package
HM51W16165J-5	50 ns	400-mil 42-pin plastic SOJ (CP-42D)
HM51W16165J-6	60 ns	
HM51W16165J-7	70 ns	
HM51W16165LJ-5	50 ns	
HM51W16165LJ-6	60 ns	
HM51W16165LJ-7	70 ns	
HM51W18165J-5	50 ns	
HM51W18165J-6	60 ns	
HM51W18165J-7	70 ns	
HM51W18165LJ-5	50 ns	
HM51W18165LJ-6	60 ns	
HM51W18165LJ-7	70 ns	
HM51W16165TT-5	50 ns	400-mil 50-pin plastic TSOP II (TTP-50/44DC)
HM51W16165TT-6	60 ns	
HM51W16165TT-7	70 ns	
HM51W16165LTT-5	50 ns	
HM51W16165LTT-6	60 ns	
HM51W16165LTT-7	70 ns	
HM51W18165TT-5	50 ns	
HM51W18165TT-6	60 ns	
HM51W18165TT-7	70 ns	
HM51W18165LTT-5	50 ns	
HM51W18165LTT-6	60 ns	
HM51W18165LTT-7	70 ns	

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Pin Arrangement

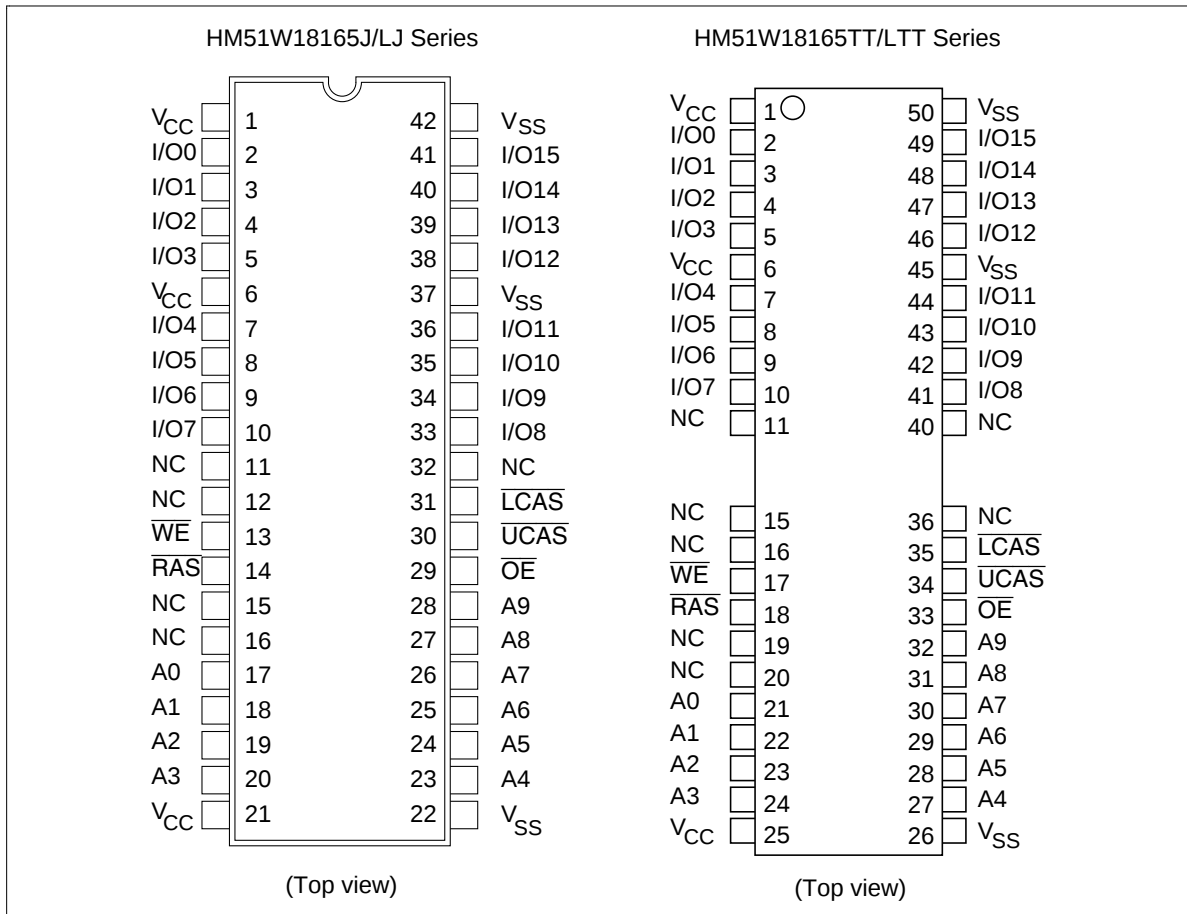


Pin Description

Pin name	Function
A0 to A11	Address input - Row/Refresh address A0 to A11 - Column address A0 to A7
I/O0 to I/O15	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

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Pin Arrangement

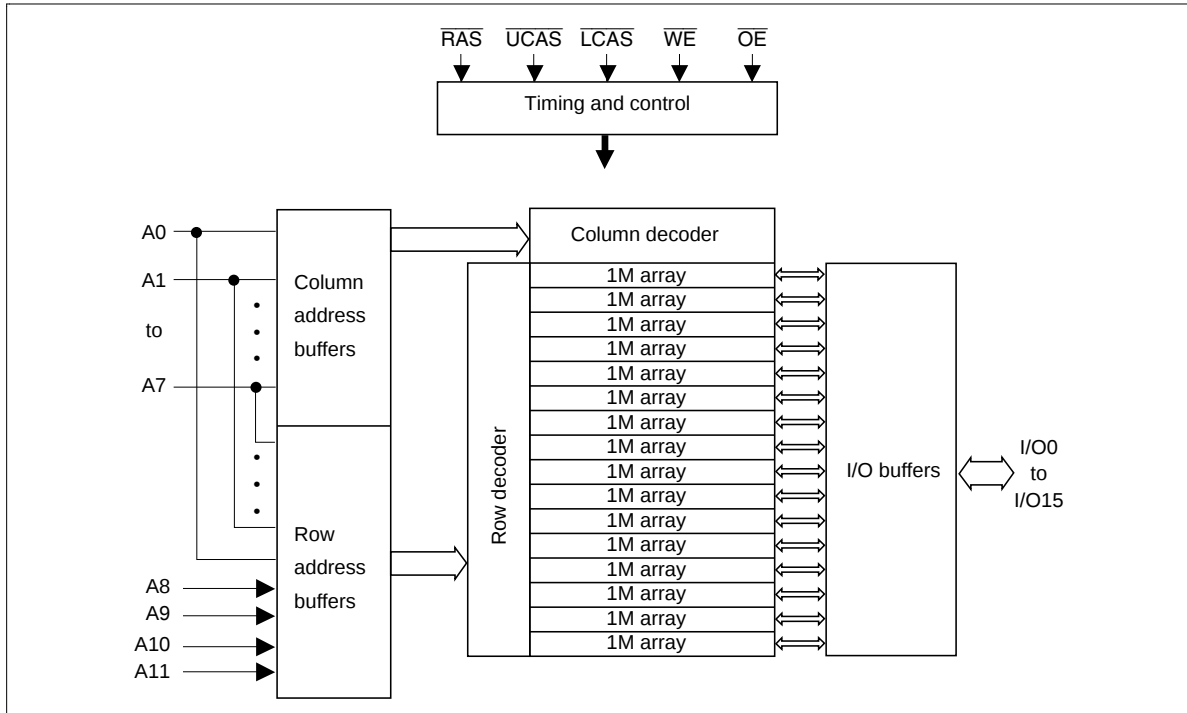


Pin Description

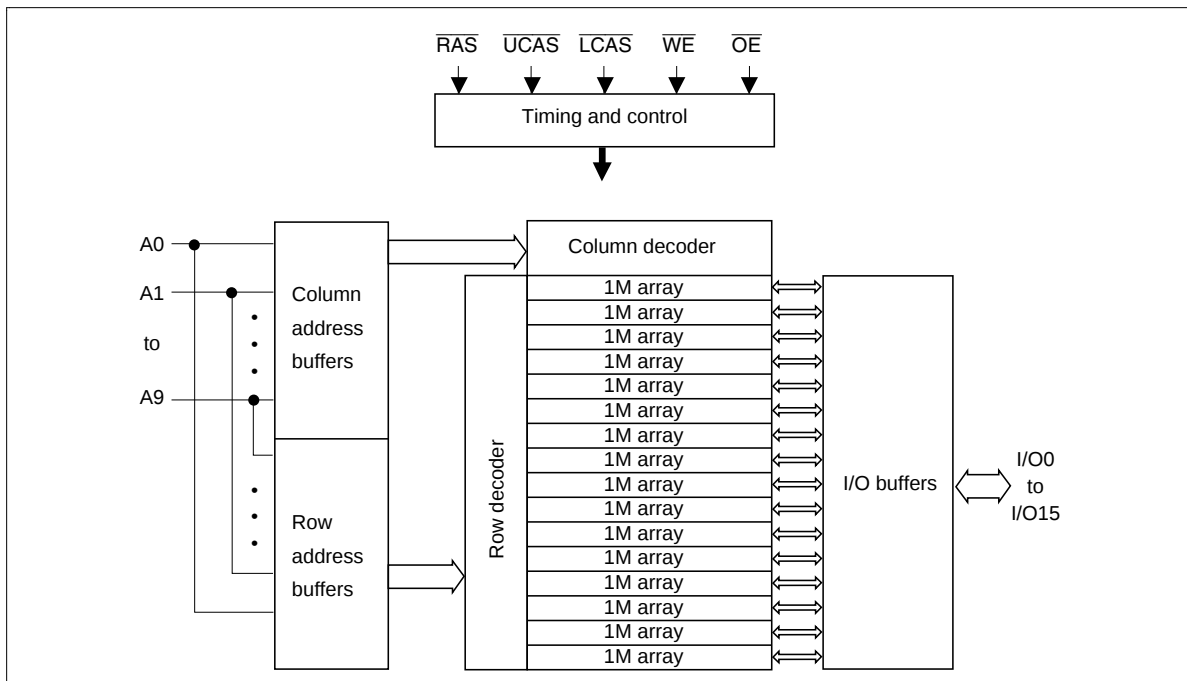
Pin name	Function
A0 to A9	Address input - Row/Refresh address A0 to A9 - Column address A0 to A9
I/O0 to I/O15	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

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Block Diagram (HM51W16165 Series)



Block Diagram(HM51W18165 Series)



Truth Table

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$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Output		Operation
H	D	D	D	D	Open		Standby
L	L	H	H	L	Valid	Lower byte	Read cycle
L	H	L	H	L	Valid	Upper byte	
L	L	L	H	L	Valid	Word	
L	L	H	L^{*2}	D	Open	Lower byte	Early write cycle
L	H	L	L^{*2}	D	Open	Upper byte	
L	L	L	L^{*2}	D	Open	Word	
L	L	H	L^{*2}	H	Undefined	Lower byte	Delayed write cycle
L	H	L	L^{*2}	H	Undefined	Upper byte	
L	L	L	L^{*2}	H	Undefined	Word	
L	L	H	H to L	L to H	Valid	Lower byte	Read-modify-write cycle
L	H	L	H to L	L to H	Valid	Upper byte	
L	L	L	H to L	L to H	Valid	Word	
L	H	H	D	D	Open	Word	$\overline{\text{RAS}}$ -only refresh cycle
H to L	H	L	D	D	Open	Word	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or
H to L	L	H	D	D	Open	Word	Self refresh cycle (L-version)
H to L	L	L	D	D	Open	Word	
L	L	L	H	H	Open		Read cycle (Output disabled)

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2. $t_{\text{WCS}} \geq 0 \text{ ns}$ Early write cycle

$t_{\text{WCS}} < 0 \text{ ns}$ Delayed write cycle

3. Mode is determined by the OR function of the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$. (Mode is set by the earliest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ active edge and reset by the latest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ inactive edge.) However write OPERATION and output HIZ control are done independently by each $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.

ex. if $\overline{\text{RAS}} = \text{H to L}$, $\overline{\text{UCAS}} = \text{H}$, $\overline{\text{LCAS}} = \text{L}$, then $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle is selected.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to $V_{CC} + 0.5$ ($\leq +4.6$ V (max))	V
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to $+4.6$	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to $+70$	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to $+125$	$^{\circ}\text{C}$

Recommended DC Operating Conditions ($T_a = 0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS} .

2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W16165 Series)

		HM51W16165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current* ¹ , * ²	I _{CC1}	—	110	—	100	—	90	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V _{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	—	150	μA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	110	—	100	—	90	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} UCAS, LCAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	110	—	100	—	90	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	105	—	95	—	85	mA	t _{HPC} = min
Battery backup current* ⁴ (Standby with CBR refresh) (L-version)	I _{CC10}	—	400	—	400	—	400	μA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	250	—	250	—	250	μA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

- Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while UCAS and LCAS = V_{IH}.
4. V_{IH} ≥ V_{CC} − 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

HM51W16165 Series, HM51W18165 Series

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (HM51W18165 Series)

		HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Operating current* ¹ , * ²	I _{CC1}	—	190	—	170	—	150	mA	t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V _{IH} Dout = High-Z
		—	1	—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
Standby current (L-version)	I _{CC2}	—	150	—	150	—	150	μA	CMOS interface RAS, UCAS, LCAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	190	—	170	—	150	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	5	—	5	—	5	mA	RAS = V _{IH} UCAS, LCAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	190	—	170	—	150	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	185	—	165	—	145	mA	t _{HPC} = min
Battery backup current* ⁴ (Standby with CBR refresh) (L-version)	I _{CC10}	—	400	—	400	—	400	μA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 125 μs t _{RAS} ≤ 0.3 μs
Self refresh mode current (L-version)	I _{CC11}	—	250	—	250	—	250	μA	CMOS interface RAS, UCAS, LCAS ≤ 0.2 V Dout = High-Z
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

- Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while UCAS and LCAS = V_{IH}.
4. V_{IH} ≥ V_{CC} − 0.2 V, 0 V ≤ V_{IL} ≤ 0.2 V.

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Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	5	pF	1
Input capacitance (Clocks)	C _{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C _{I/O}	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. RAS, UCAS and LCAS = V_{IH} to disable Dout.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$)*¹, *², *¹⁸, *¹⁹, *²⁰

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W16165/HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
RAS precharge time	t_{RP}	30	—	40	—	50	—	ns	
CAS precharge time	t_{CP}	8	—	10	—	13	—	ns	
RAS pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
CAS pulse width	t_{CAS}	8	10000	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	21
Column address hold time	t_{CAH}	8	—	10	—	13	—	ns	21
RAS to CAS delay time	t_{RCD}	12	37	14	45	14	52	ns	3
RAS to column address delay time	t_{RAD}	10	25	12	30	12	35	ns	4
RAS hold time	t_{RSH}	10	—	13	—	13	—	ns	
CAS hold time	t_{CSH}	35	—	40	—	45	—	ns	23
CAS to RAS precharge time	t_{CRP}	5	—	5	—	5	—	ns	22
OE to Din delay time	t_{OED}	13	—	15	—	18	—	ns	5
OE delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
CAS delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7

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Read Cycle

		HM51W16165/HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	—	35	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	—	18	ns	9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	21
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12, 22
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	27
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	13, 27
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	13	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	27
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	13	—	15	—	15	ns	27
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	13	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	t_{RNCD}	50	—	60	—	70	—	ns	

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Write Cycle

		HM51W16165/HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14, 21
Write command hold time	t_{WCH}	8	—	10	—	13	—	ns	21
Write command pulse width	t_{WP}	8	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8	—	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	—	10	—	13	—	ns	23
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15, 23
Data-in hold time	t_{DH}	8	—	10	—	13	—	ns	15, 23

Read-Modify-Write Cycle

		HM51W16165/HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	111	—	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	57	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	18	—	ns	

Refresh Cycle

		HM51W16165/HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	21
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	10	—	ns	22
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	21

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EDO Page Mode Cycle

		HM51W16165/HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t _{HPC}	20	—	25	—	30	—	ns	25
EDO page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	30	—	35	—	40	ns	9, 17, 22
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	30	—	35	—	40	—	ns	
Output data hold time from $\overline{\text{CAS}}$ low	t _{DOH}	3	—	3	—	3	—	ns	9
$\overline{\text{CAS}}$ hold time referred $\overline{\text{OE}}$	t _{COL}	8	—	10	—	13	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ setup time	t _{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{\text{CAS}}$ precharge	t _{RCHC}	30	—	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM51W16165/HM51W18165							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t _{HPRWC}	57	—	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t _{CPW}	45	—	54	—	62	—	ns	14, 22

Refresh (HM51W16165 Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	64	ms	4096 cycles
Refresh period (L-version)	t_{REF}	128	ms	4096 cycles

Refresh (HM51W18165 Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	16	ms	1024 cycles
Refresh period (L-version)	t_{REF}	128	ms	1024 cycles

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Self Refresh Mode (L-version)

		HM51W16165L/HM51W18165L							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
RAS pulse width (self refresh)	t _{RASS}	100	—	100	—	100	—	μs	28, 29, 30, 31
RAS precharge time (self refresh)	t _{RPS}	90	—	110	—	130	—	ns	
CAS hold time (self refresh)	t _{CHS}	−50	—	−50	—	−50	—	ns	

- Notes:
1. AC measurements assume $t_f = 2 \text{ ns}$.
 2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh).
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{\text{RCD}} \geq t_{\text{RAD}} (\text{max}) + t_{\text{AA}} (\text{max}) - t_{\text{CAC}} (\text{max})$, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. $t_{\text{OFF}} (\text{max})$ and $t_{\text{OEZ}} (\text{max})$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, and $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$, or $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}} (\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device
 19. When both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ go low at the same time, all 16-bit data are written into the device. $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ cannot be staggered within the same write/read cycles.
 20. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.

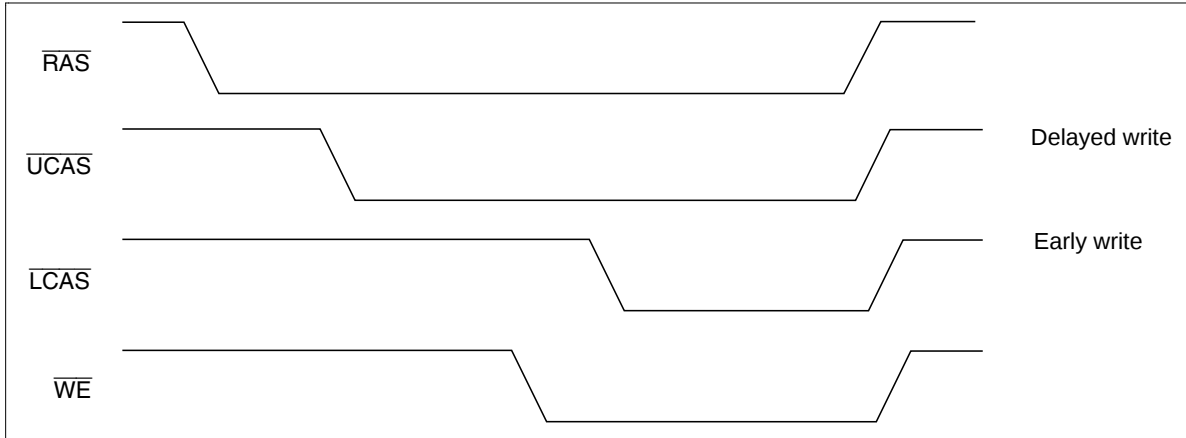
HM51W16165 Series, HM51W18165 Series

21. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
22. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
23. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
24. t_{CP} is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
25. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode RAS cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2 t_r$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/ V_{IL} max level.
27. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
28. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP} .
29. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
30. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 1024 cycles (4096 cycles: HM51W16165 Series, 1024 cycles: HM51W18165 Series) of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 64 or 16 ms (64 ms: HM51W16165, 16 ms: HM51W18165) immediately after exiting from and before entering into the self refresh mode.
31. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
32. XXX: H or L (H: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$)
/////: Invalid Dout
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

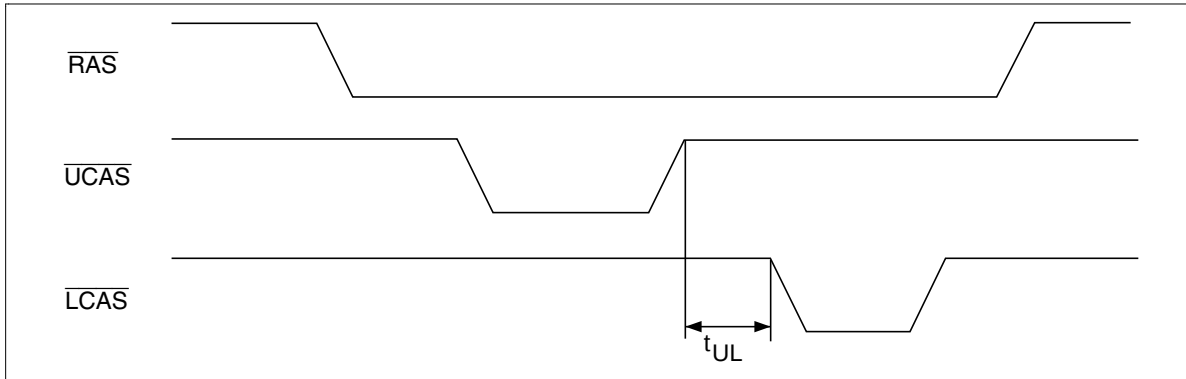
Notes concerning $\overline{2CAS}$ control

Please do not separate the $\overline{UCAS}/\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}/\overline{LCAS}$ are allowed under the following conditions.

1. Each of the $\overline{UCAS}/\overline{LCAS}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.



3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, EDO page mode can be performed.

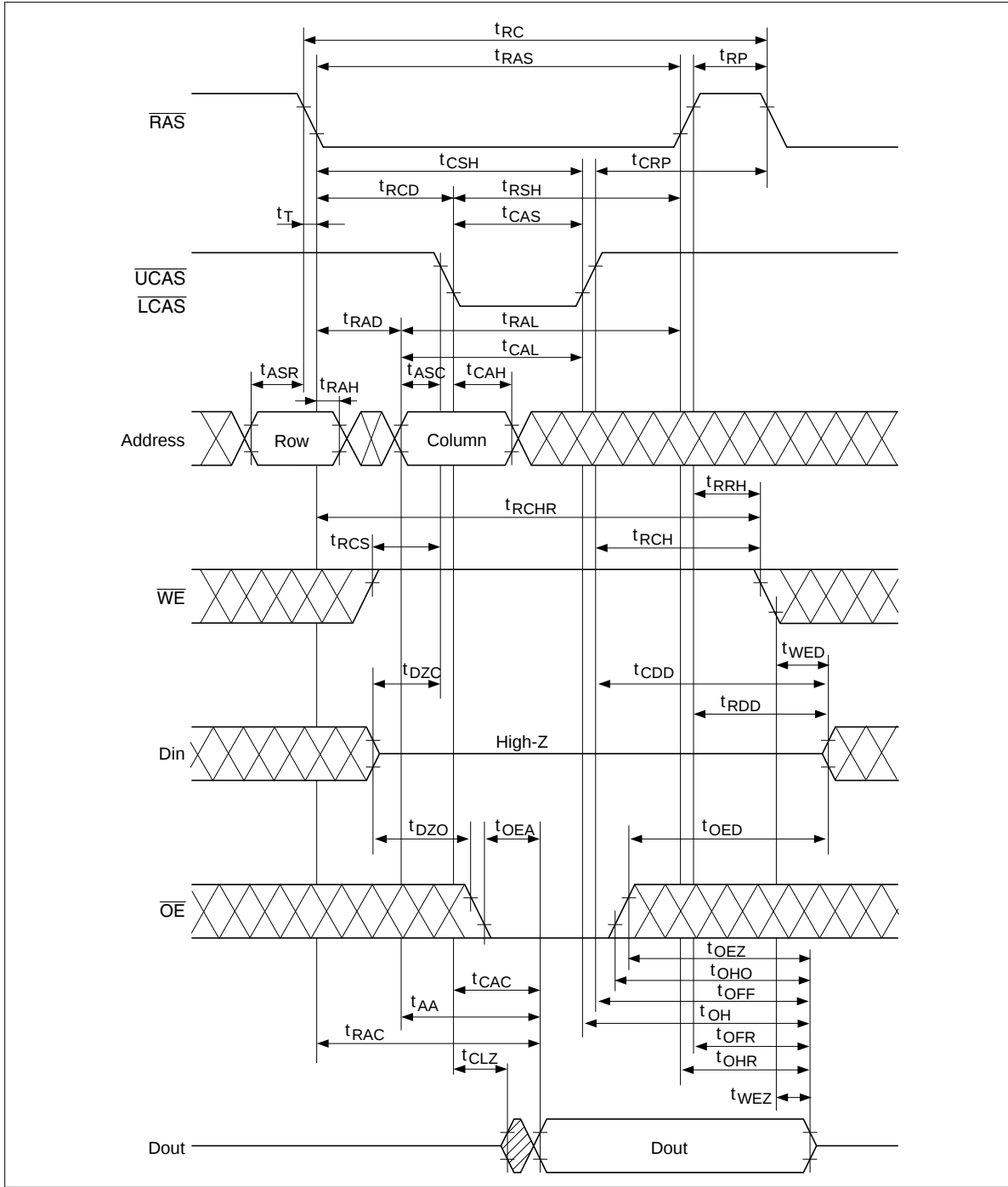


4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.

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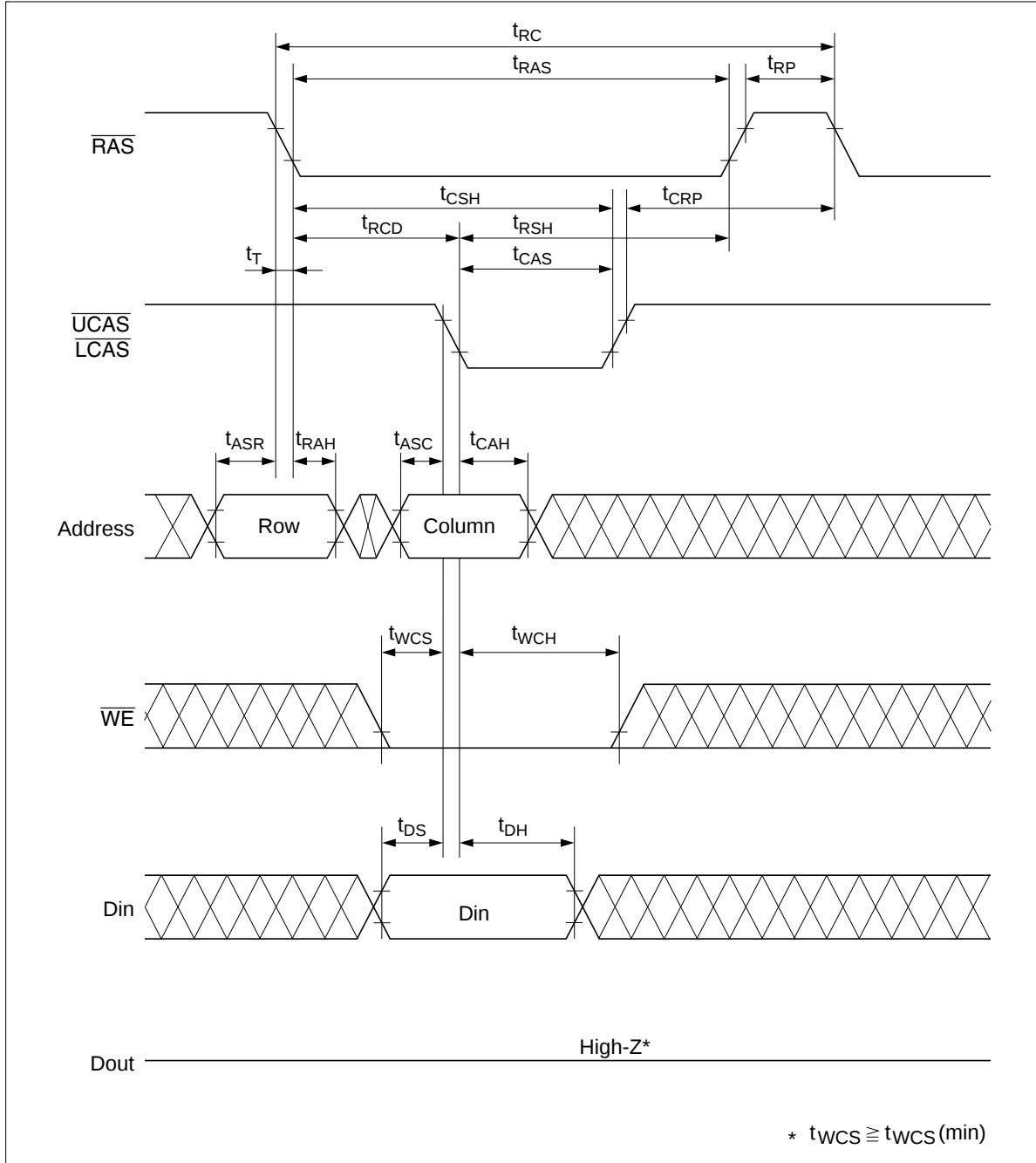
Timing Waveforms*32

Read Cycle



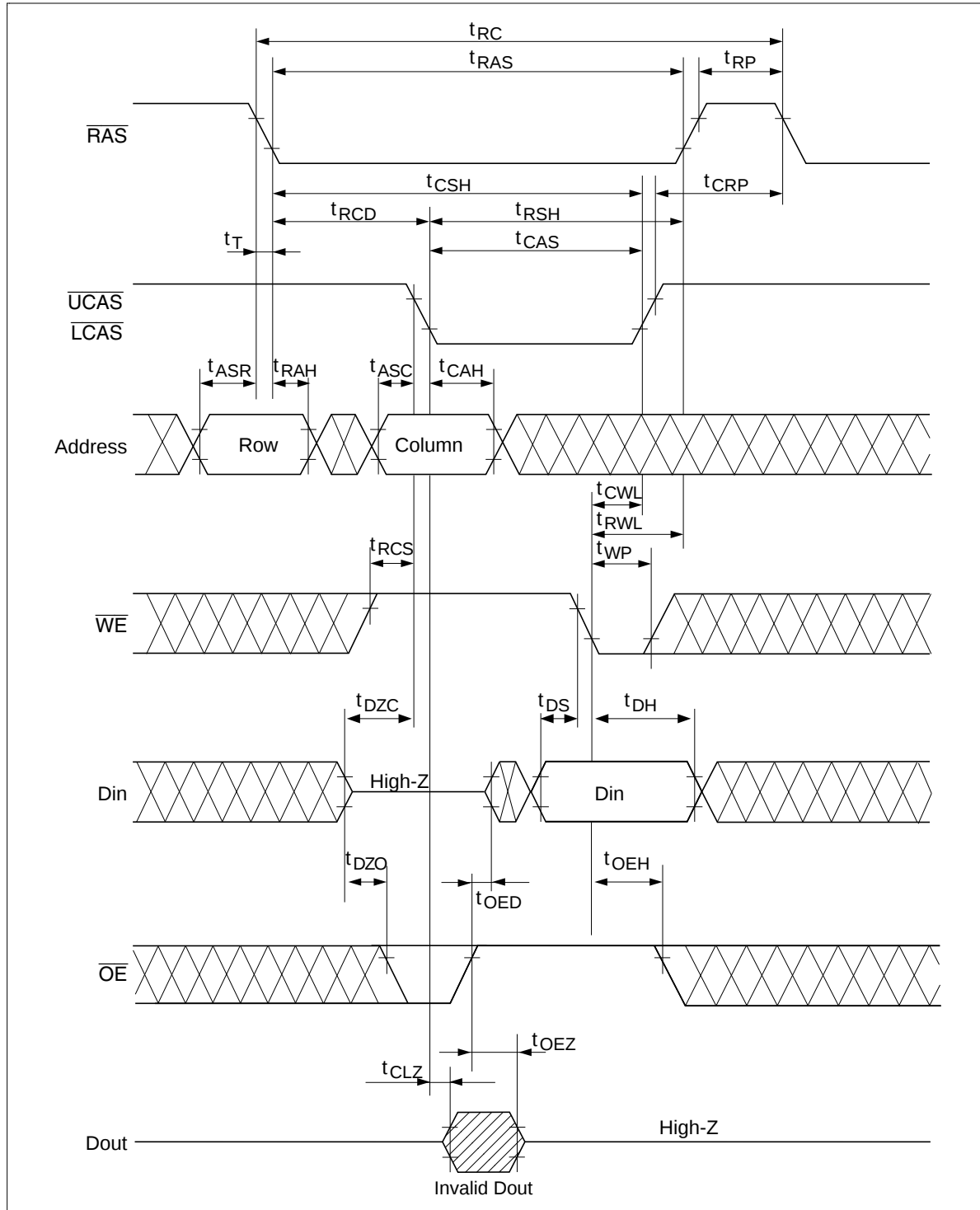
HM51W16165 Series, HM51W18165 Series

Early Write Cycle



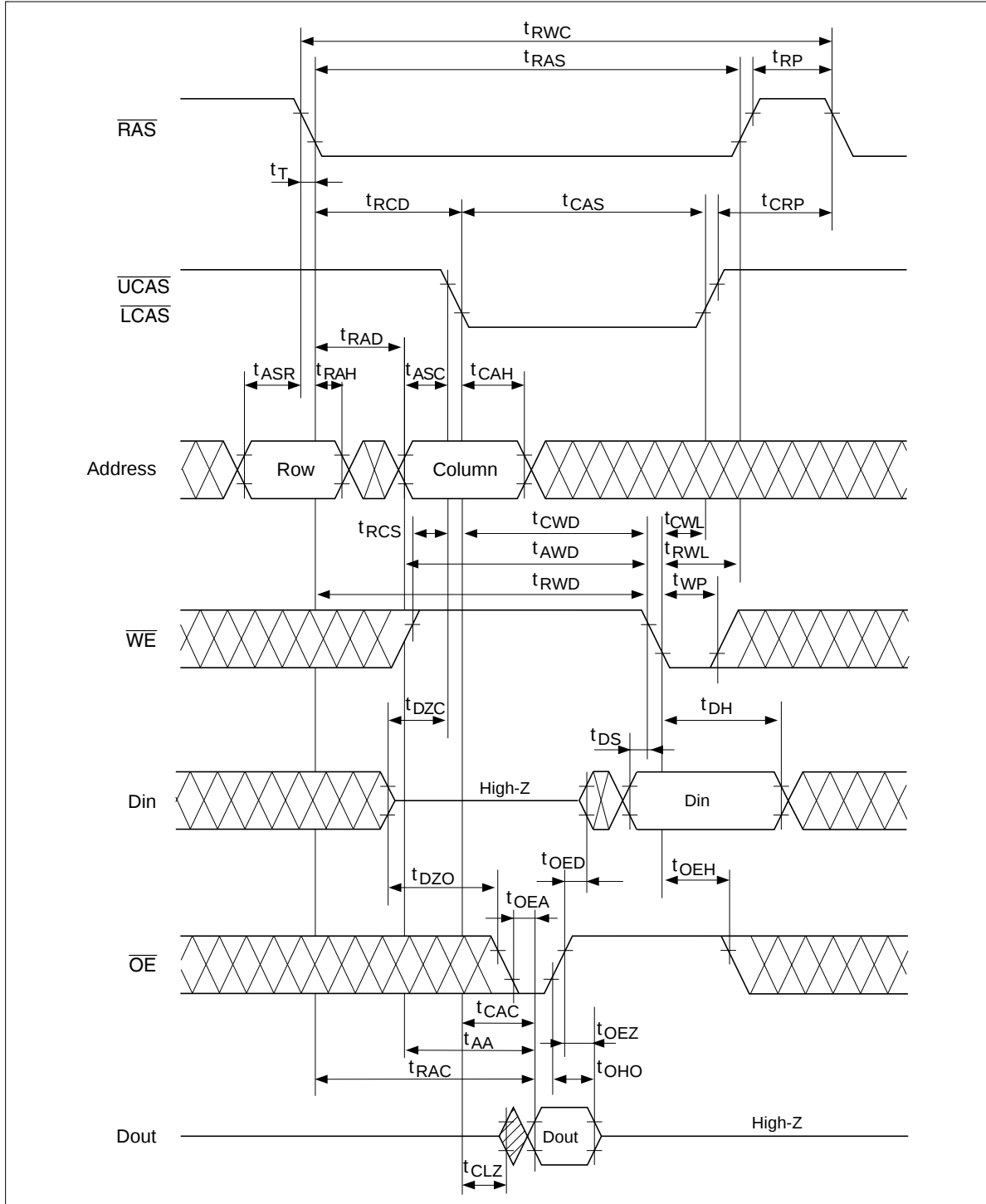
HM51W16165 Series, HM51W18165 Series

Delayed Write Cycle*¹⁸



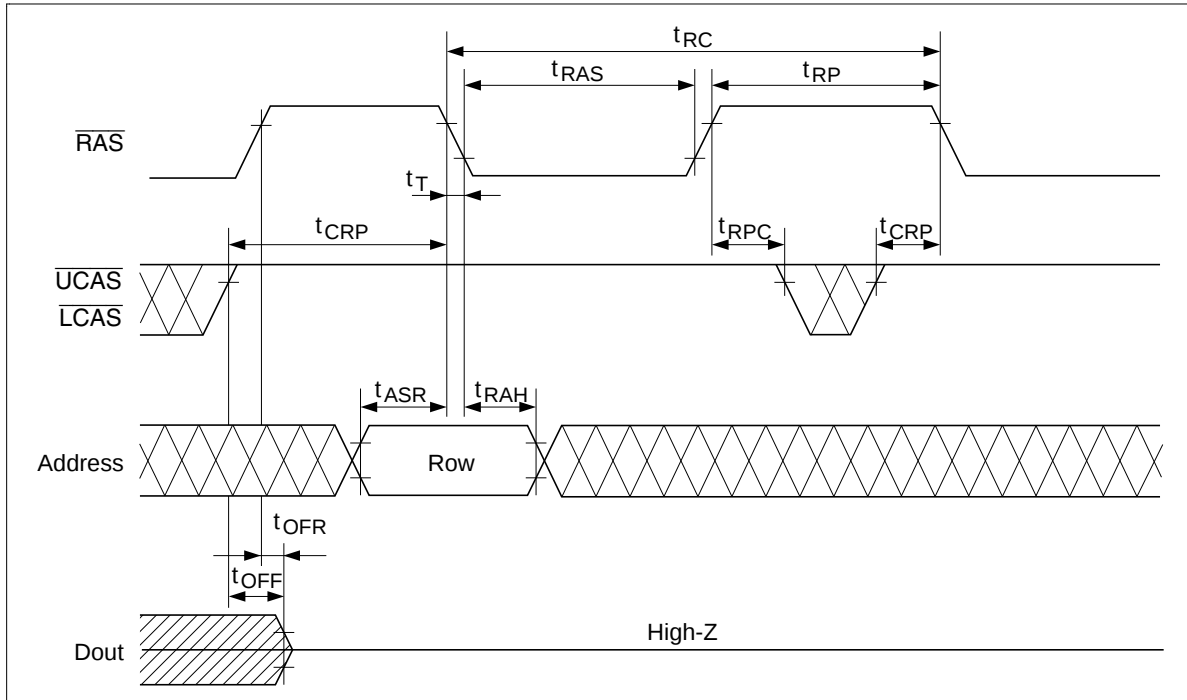
HM51W16165 Series, HM51W18165 Series

Read-Modify-Write Cycle*18



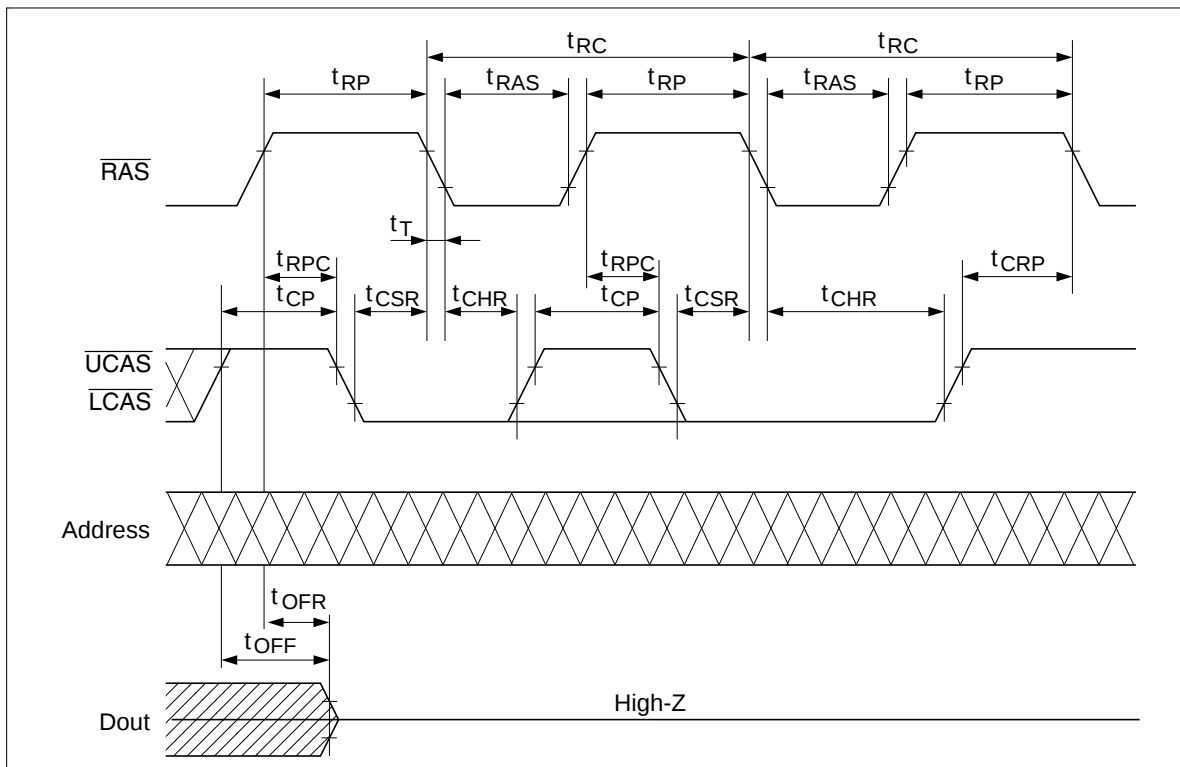
HM51W16165 Series, HM51W18165 Series

$\overline{\text{RAS}}$ -Only Refresh Cycle



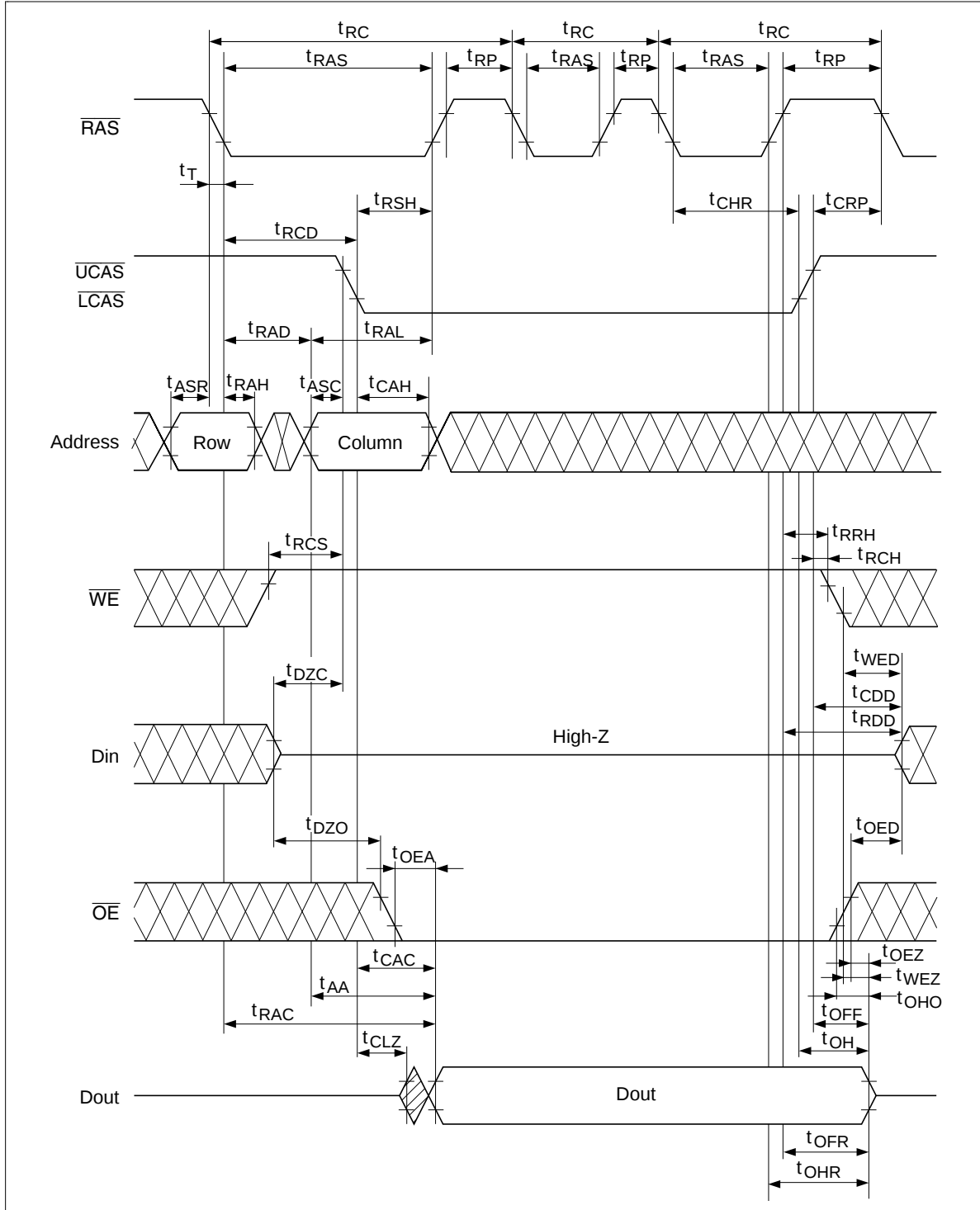
HM51W16165 Series, HM51W18165 Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

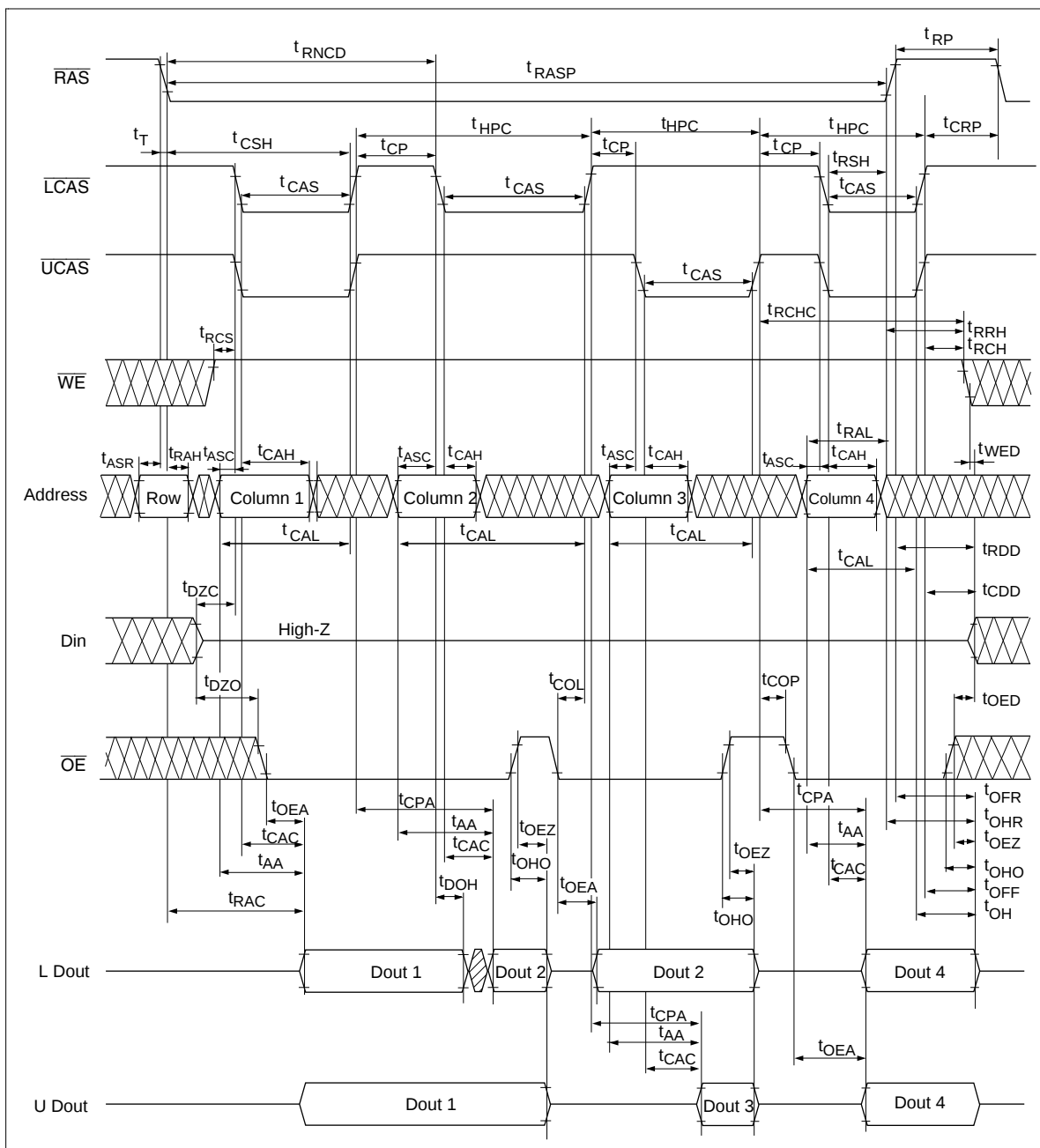


HM51W16165 Series, HM51W18165 Series

Hidden Refresh Cycle

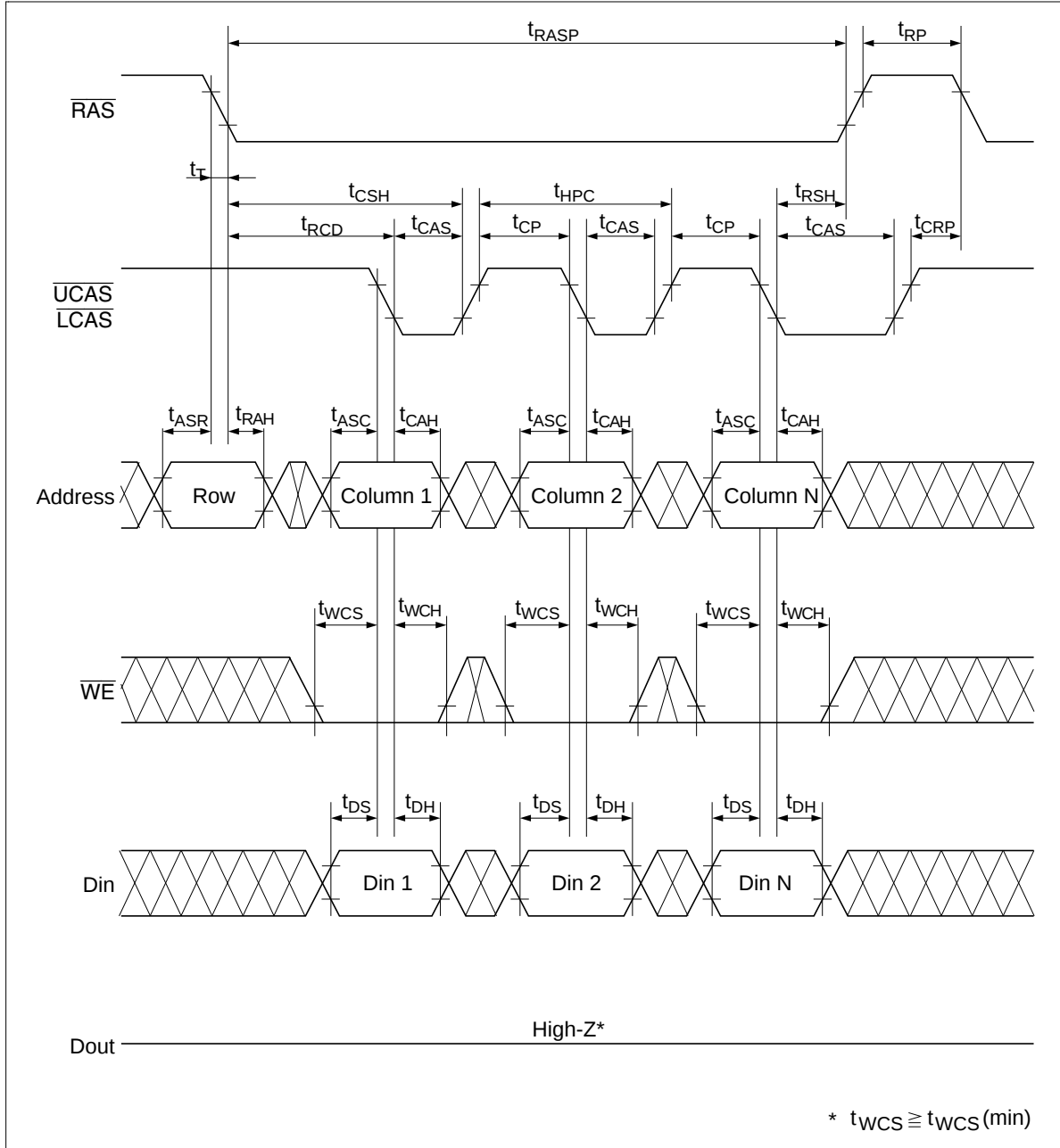


EDO Page Mode Read Cycle ($\overline{2\text{CAS}}$ control)



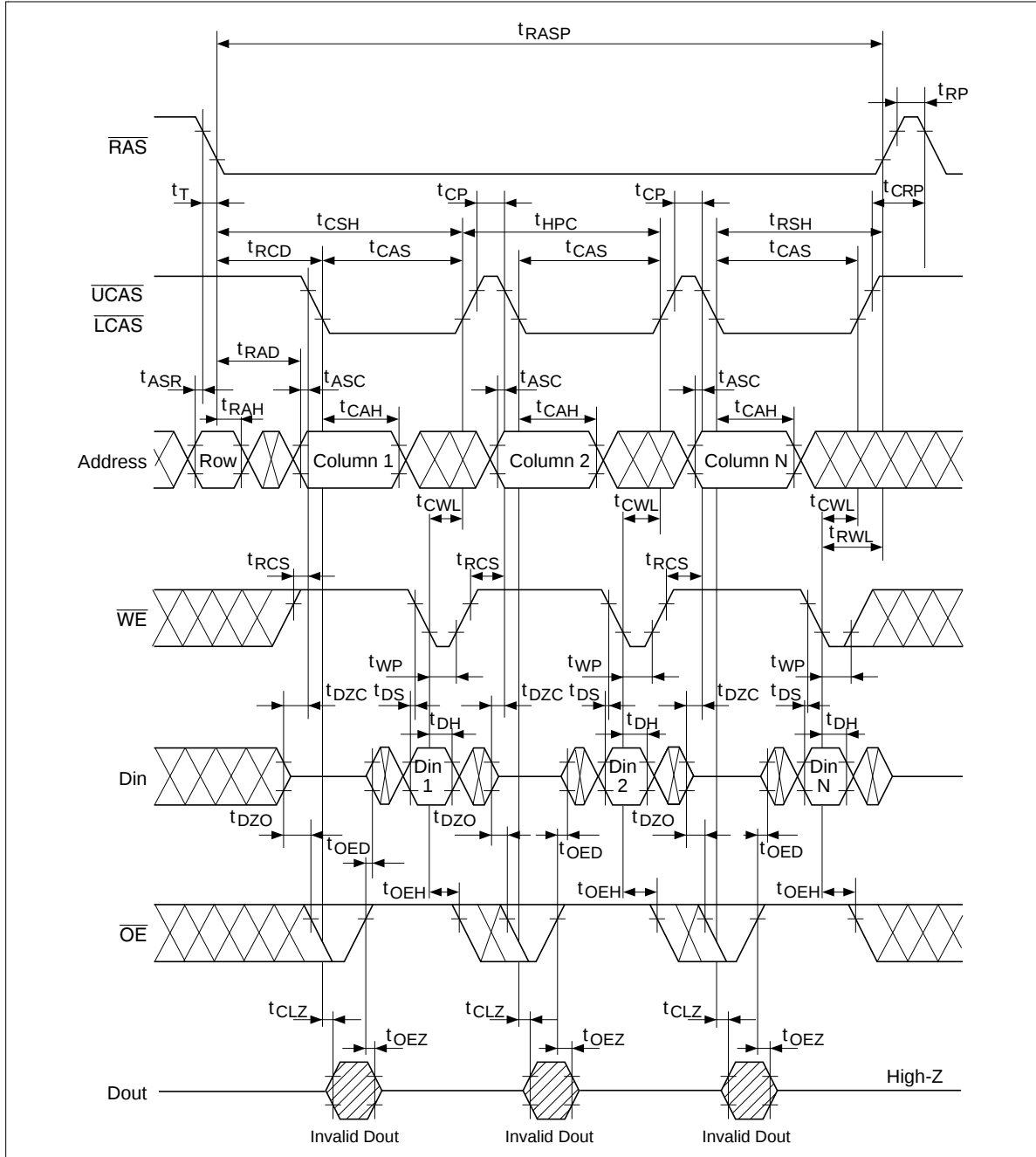
HM51W16165 Series, HM51W18165 Series

EDO Page Mode Early Write Cycle



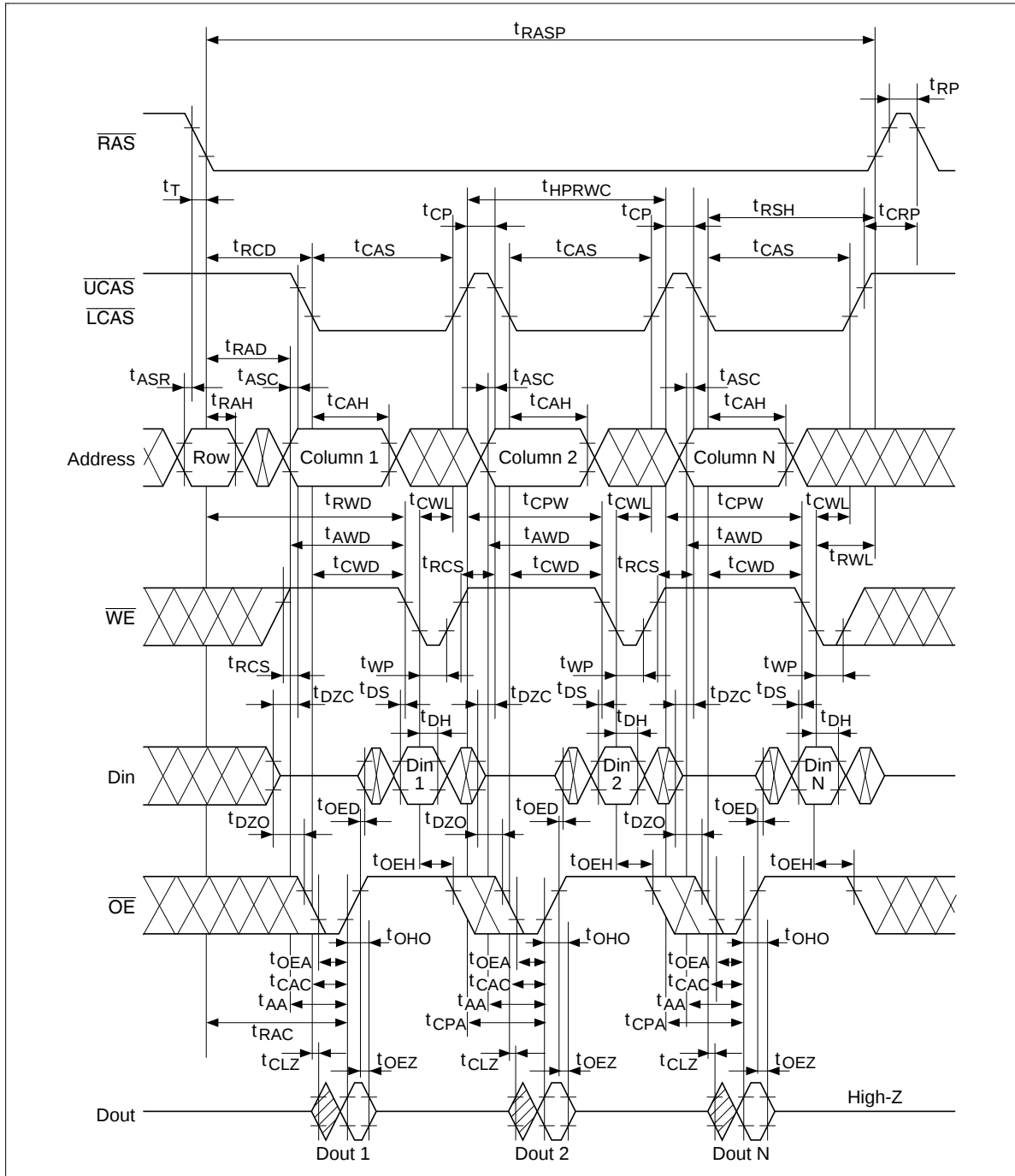
HM51W16165 Series, HM51W18165 Series

EDO Page Mode Delayed Write Cycle*18



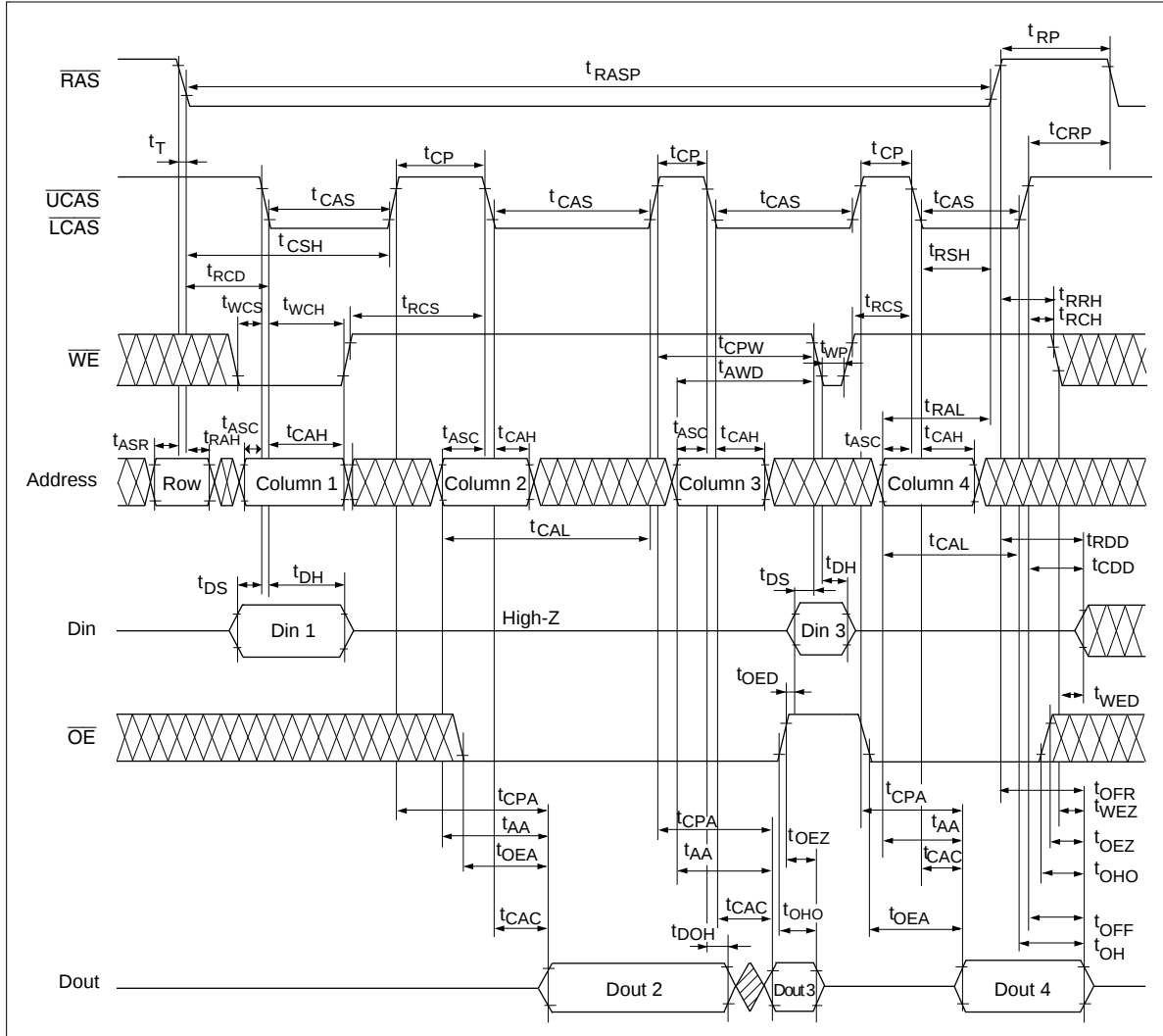
HM51W16165 Series, HM51W18165 Series

EDO Page Mode Read-Modify-Write Cycle*18

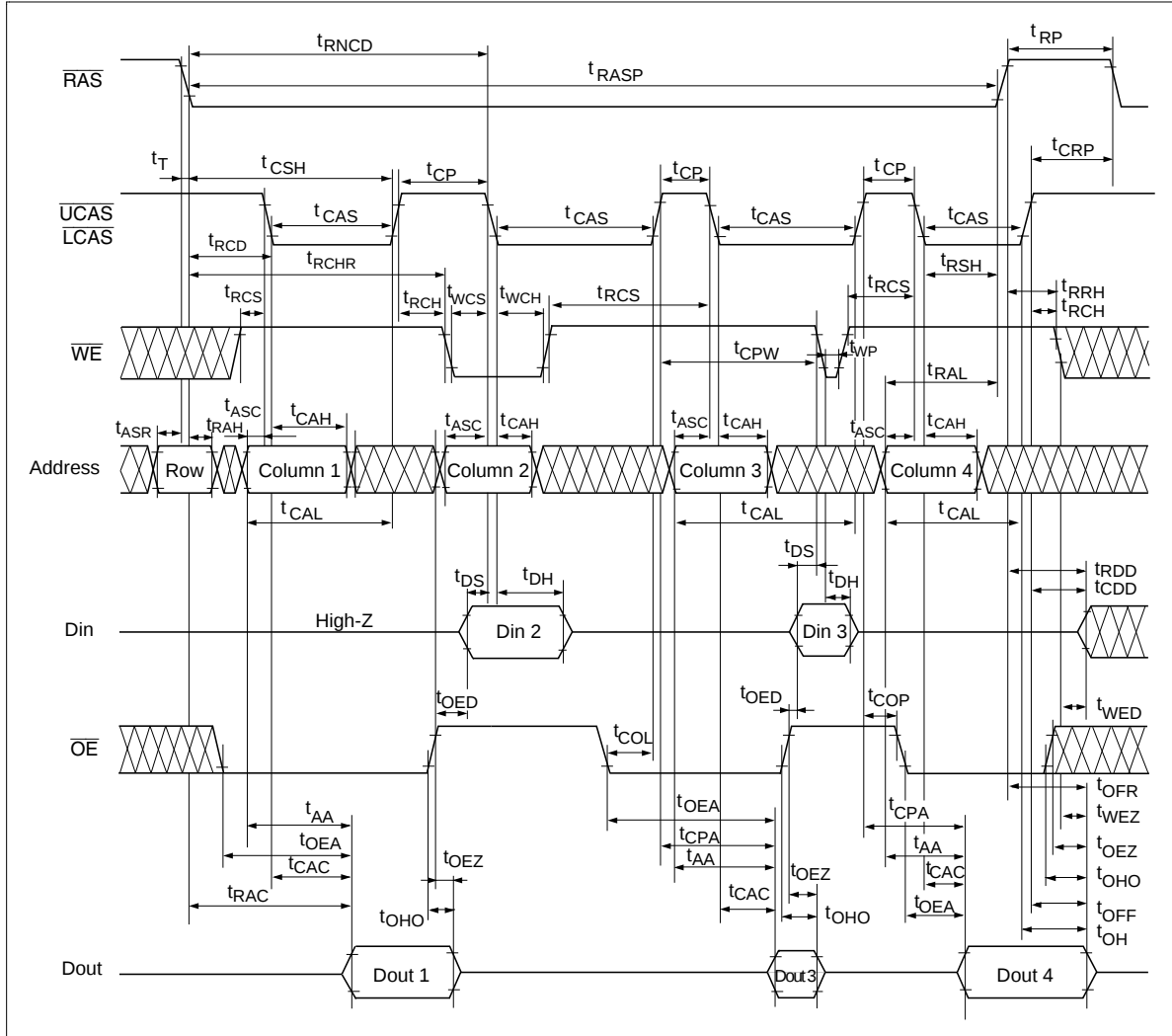


HM51W16165 Series, HM51W18165 Series

EDO Page Mode Mix Cycle (1)

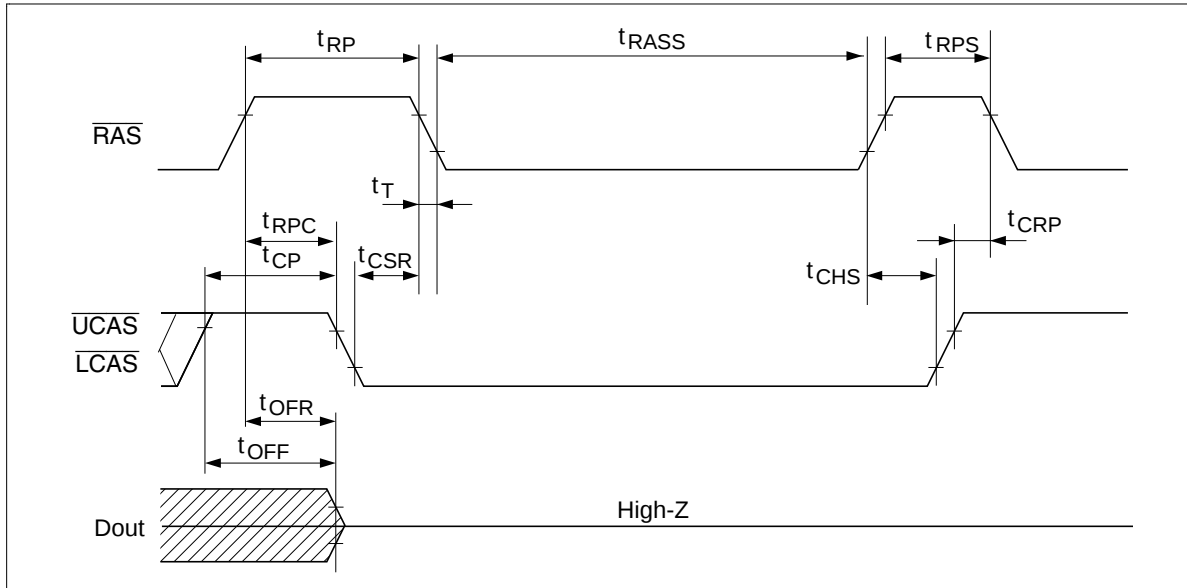


EDO Page Mode Mix Cycle (2)



HM51W16165 Series, HM51W18165 Series

Self Refresh Cycle (L-version)*28, *29, *30, *31



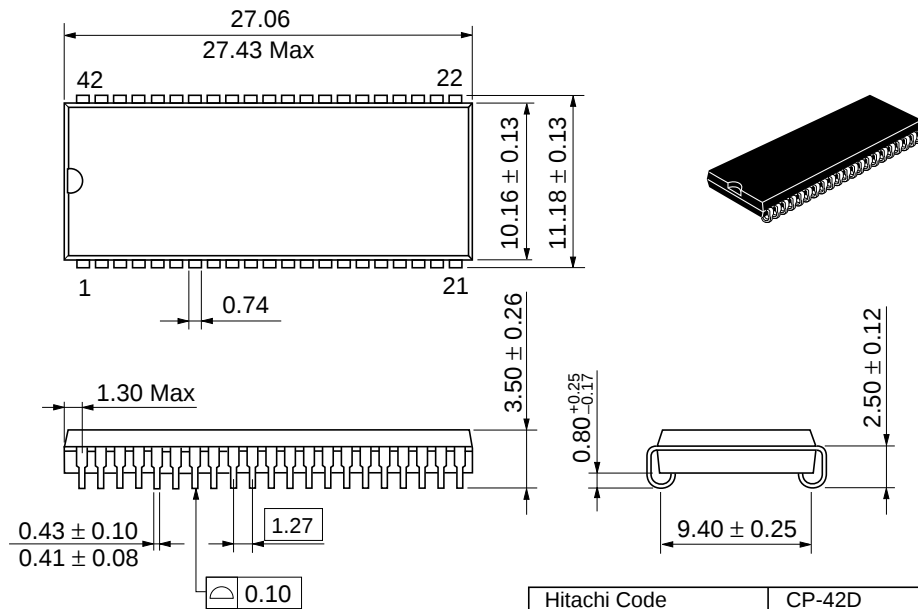
HM51W16165 Series, HM51W18165 Series

Package Dimensions

HM51W16165J/LJ Series

HM51W18165J/LJ Series (CP-42D)

Unit: mm



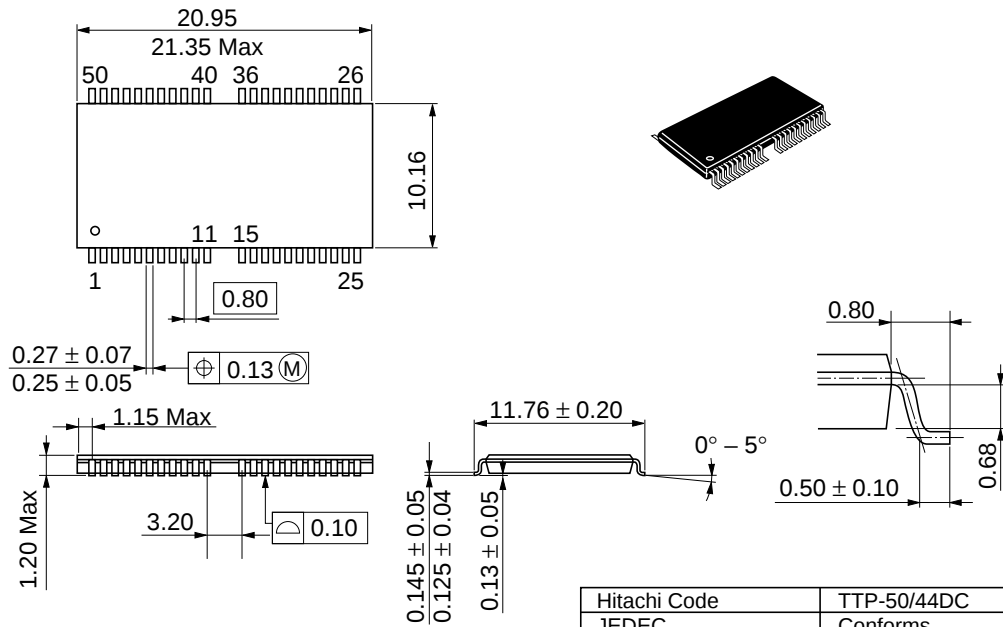
Hitachi Code	CP-42D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.75 g

HM51W16165 Series, HM51W18165 Series

HM51W16165TT/LTT Series

HM51W18165TT/LTT Series (TTP-50/44DC)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-50/44DC
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.50 g

HM51W16165 Series, HM51W18165 Series

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HM51W16165 Series, HM51W18165 Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Sep. 30, 1996	Initial issue	Y. Kasama	M. Mishima
2.0	Nov. 28, 1996	Addition of HM51W16165/HM51W18165-5 Series Power dissipation (active) 468/414 mW(max) to 396/360/324 mW (max) (HM51W16165 Series) 666/594 mW(max) to 684/612/540 mW (max) (HM51W18165 Series) DC Characteristics (HM51W16165 Series) I_{CC7} max: 135/115 mA to 105/95/85 mA DC Characteristics (HM51W18165 Series) I_{CC7} max: 185/165 mA to 185/165/145 mA AC Characteristics t_{RCD} min: 20/20 ns to 12/14/14 ns t_{RAD} min: 15/15 ns to 10/12/12 ns t_{RSH} min: 15/18 ns to 10/13/13 ns t_{RRH} min: 0/0 ns to 5/5/5 ns t_{RWC} min: 136/161 ns to 111/135/161 ns t_{RPC} min: 0/0 ns to 5/5/5 ns Timing Waveforms Addition of t_{RNCD} timing to EDO page mode mix cycle (2)	Y. Kasama	M. Mishima
3.0	Feb. 24, 1997	AC Characteristics t_{RRH} min: 5/5/5 ns to 0/0/0 ns	Y. Kasama	Y. Matsuno
4.0	Nov. 1997	Change of Subtitle		
