H 6060

Self Recovering Watchdog

Features

- Self recovering watchdog function: reset goes active after the 1st timeout period, reset goes inactive again after the 2nd timeout period, repeated active reset signal until the system recovers
- Standard timeout period and power-on reset time (100ms), externally programmable if required
- Unregulated DC monitoring (V_{IN}) with 3 standard or programmable trigger voltages for: power-on reset initialization, advanced power-fail warning ($\overline{SAVE}$), reset at power-down ($\overline{RES}$)
- Regulated DC monitoring (V_{DD}): power-on reset initialization enabled only if $V_{DD} \geq 3.5V$
- Internal voltage reference
- Works down to 1.6V supply voltage
- Push-pull or Open drain outputs
- Low current consumption
- Available for normal and extended temperature ranges
- DIP8 and SO8 package

Description

The H 6060 is a monolithic low-power CMOS device combining a programmable timer and a series of voltage comparators on the same chip. The device is specially suited for watchdog functions such as microprocessor and supply voltage monitoring. If the μP system malfunctions, the watchdog will recover it by issuing repeated active reset signals. The voltage monitoring part provides double security by combining both the unregulated voltage (V_{IN}) and the regulated voltage (V_{DD}) monitoring simultaneously. The H 6060 initializes the power-on reset after V_{IN} reaches V_{SH} (see table 4) and V_{DD} rises above 3.5V. If V_{IN} drops below V_{SL} (see table 4), the H 6060 gives an advanced warning signal for register saving and if the voltage drops further below V_{RL} (see table 4), $\overline{RES}$ and RES go active. The H 6060 functions at any supply voltage down to 1.6V and is therefore particularly suited for start-up and shut-down control of microprocessor systems.

Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems

Typical Operating Configuration

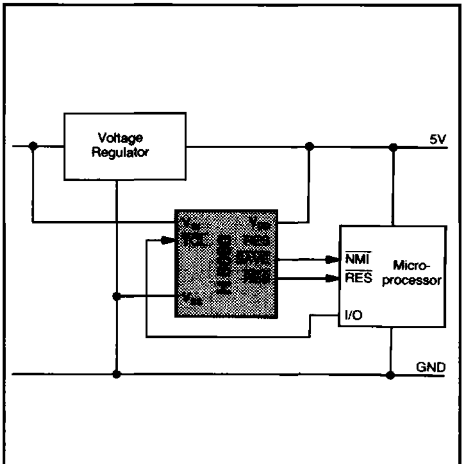


Fig. 1

Pin Assignment

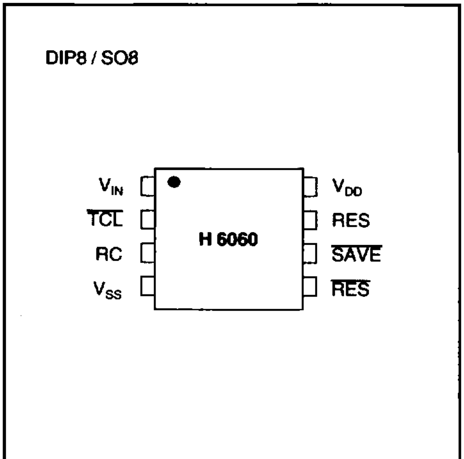


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{DD}	−0.3 to +8V
Voltage at any pin to V_{SS}	V_{MIN}	−0.3
Voltage at any pin to V_{DD} (except V_{IN})	V_{MAX}	+0.3
Voltage at V_{IN} to V_{SS}	V_{INMAX}	+15V
Current at any output	I_{MAX}	±10mA
Storage temperature	T_{STO}	−65...+150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature					
Industrial	T_{AI}	−40		+85	°C
Extended	T_{AX}	−40		+125	°C
Supply voltage	V_{DD}	1.6		5.5	V
Comparator input voltage					
Version 13, 14, 15, 16	V_{IN}	0		V_{DD}	V
Version 11, 12	V_{IN}	0		12	V
RC-oscillator programming (see Fig. 15)					
External capacitance*	C1			1	µF
External resistance	R1	10			kΩ

** Leakage < 1µA* — *Table 2*

Electrical Characteristics

V_{DD} = 5.0 V, T_A = −40 to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
V_{DD} activation threshold	V_{ON}	T_A = 25°C	3		3.5	V
V_{DD} deactivation threshold	V_{OFF}	T_A = 25°C		V_{ON}−0.3		V
Supply current	I_{DD}	RC open, TCL at V_{DD} or V_{SS}		80	140	µA
Input V_{IN}, $\overline{TCL}$						
Leakage current	I_{IP}	$V_{SS} \leq V_{IP} \leq V_{DD}$; T_A = 85°C		0.005	1	µA
Input current on pin V_{IN}	I_{IN}	Versions 11, 12; V_{IN} = 10V		100	180	µA
$\overline{TCL}$ input low level	V_{IL}				0.8	V
$\overline{TCL}$ input high level	V_{IH}		2.4			V
$\overline{SAVE}$, $\overline{RES}$, RES outputs						
Leakage current	I_{OLK}	Versions 11, 13, 15; $V_{OUT} = V_{DD}$		0.05	1	µA
Drive currents (all versions)	I_{OL}	V_{OL} = 0.4V	3.2	8		mA
	I_{OL}	V_{DD} = 3.5V; V_{OL} = 0.4V	2			mA
	I_{OL}	V_{DD} = 1.6V; V_{OL} = 0.4V	80			µA
Drive currents (versions 12, 14, 16)[1]	I_{OH}	V_{OH} = 4.0V	3.2	8		mA
	I_{OH}	V_{DD} = 3.5V; V_{OH} = 2.8V	2			mA
	I_{OH}	V_{DD} = 1.6V; V_{OH} = 1.2V	80			µA

[1] Versions: 11, 13, 15 = open drain outputs; 12, 14, 16 = push-pull outputs — Table 3

V_{IN} Surveillance

Voltage thresholds at T_A = 25°C

Version [1]	Comparator Reference	Input Resistance on V_{IN} (R_{VIN})	Thresholds V_{SH}	V_{SL}	V_{RL}	Threshold Tolerance	Ratio Tolerance [3]
11, 12	V_{DD}	100kΩ	9.00	8.00	7.00[2]	± 5%	± 2%
13, 14	V_{DD}	~100MΩ	2.25	2.00	1.75[2]	± 5%	± 2%
15, 16	Band-gap reference	~100MΩ	2.00	1.95	1.90	±10%	± 2%

[1] Versions: 11, 13, 15 = open drain outputs; 12, 14, 16 = push-pull outputs — Table 4

[2] at V_{DD} = 5V

[3] Threshold ratio tolerance is defined as the tolerance of V_{SH}/V_{SL} and V_{SL}/V_{RL}.

Timing Characteristics

V_{DD} = 5.0 V, T_A = −40°C to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays						
$\overline{TCL}$ to output pins	T_{DIDO}			250	500	ns
V_{IN} to output pins	T_{AIDO}	Excluding debounce time T_{DB}		4	10	µs
Logic transition times on all output pins	T_{TR}	Load 10kΩ, 100pF		30	100	ns
Timeout period	T_{TO}	RC open, unshielded, T_A = 25°C	60	100	160	ms
	T_{TO}	RC open, unshielded (not tested)	45		200	ms
T_{TCL} input pulse width	T_{TCL}		150			ns
Power-on reset debounce	T_{DB}			$T_{TO}/64$		ms
V_{IN} low pulse	T_{VINL}	Where debounce time T_{DB} is guaranteed	10			µs

Table 5

Timing Waveforms

Voltage reaction: V_{DD} Monitoring

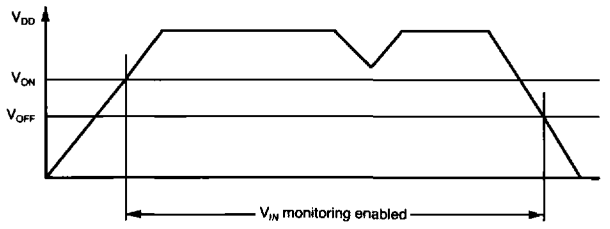


Fig. 3

Voltage Reaction: V_{IN} Monitoring

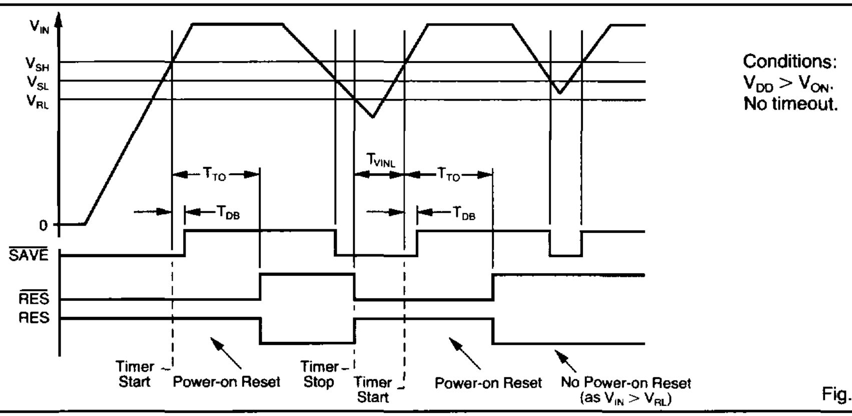
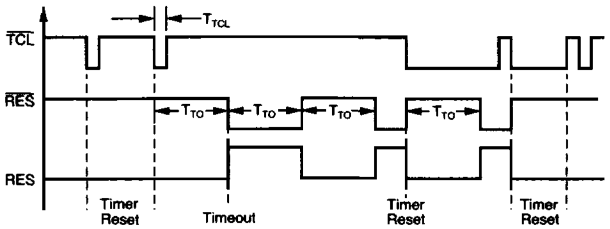


Fig. 4

Timer Reaction



Conditions:
$V_{IN} > V_{RL}$ after power-up sequence

Fig. 5

Combined Voltage and Timer Reaction

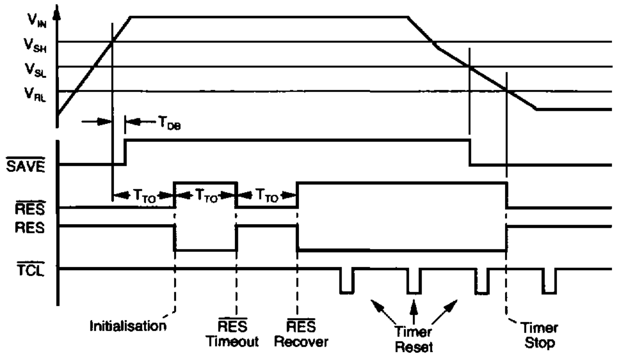
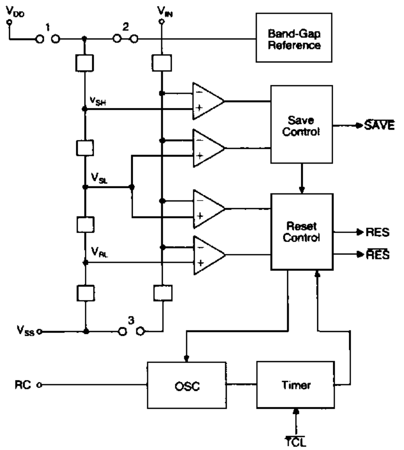


Fig. 6

Block Diagram



Version	Connections
11, 12	1 and 3
13, 14	1
15, 16	2

Fig. 7

Pin Description

Pin	Name	Function
1	V_{IN}	Voltage sense input
2	$\overline{TCL}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	V_{SS}	GND terminal
5	$\overline{RES}$	Active low reset output
6	$\overline{SAVE}$	Save output
7	RES	Active high reset output
8	V_{DD}	Positive supply voltage terminal

Table 6

Functional Description

Supply Lines

The circuit is powered through the V_{DD} and V_{SS} pins. It monitors both its own V_{DD} supply and a voltage applied to the V_{IN} input.

V_{DD} Monitoring

During power-up the V_{IN} monitoring is disabled and $\overline{RES}$, RES and $\overline{SAVE}$ stay active low as long as V_{DD} is below V_{ON} (3.5V). As soon as V_{DD} reaches the V_{ON} level, the state of the outputs depend on the watchdog timer and the voltage at V_{IN} relative to the thresholds (see Fig. 4). If the supply voltage V_{DD} falls back below V_{OFF} (V_{ON} - 0.3V) the watchdog timer and the V_{IN} monitoring are disabled and the outputs $\overline{RES}$, RES and $\overline{SAVE}$ become active. The V_{DD} line should be free of voltage spikes.

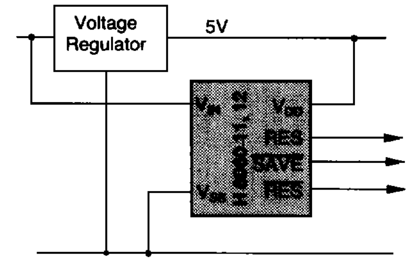
V_{IN} Monitoring

The analog voltage comparators compare the voltage applied to V_{IN} (typically connected to the input of the voltage regulator) with the stabilized supply voltage V_{DD} (versions 11, 12, 13, 14) or with the bandgap voltage (versions 15, 16) (see Fig. 7). At power-up, when V_{DD} reached V_{ON} and V_{IN} reaches the V_{SH} level, the $\overline{SAVE}$ output goes inactive, and the timer starts running, setting $\overline{RES}$ and RES inactive after the time T_{TO} (see Fig. 4). If V_{IN} falls below V_{SL}, the $\overline{SAVE}$ output goes active and stays active until V_{IN} rises again above V_{SH}. If V_{IN} falls below the voltage V_{RL}, $\overline{RES}$ and RES will become active and the on-chip timer will stop. When V_{IN} rises again above V_{SH}, the timer will initiate a power-up sequence. The $\overline{RES}$ and RES outputs may however be influenced independently of the voltage V_{IN} by the timer action, see section „Combined Voltage and Timer Action". Monitoring the rough DC side of the regulator, as shown in Fig. 12, is the only way to have advanced warning of power-down. Spikes on V_{IN} should be filtered if they are likely to exceed the value (V_{SL} - V_{RL}).
The combination of V_{IN} and V_{DD} monitoring provide high system security: if V_{IN} rises much faster than V_{DD}, then the device starts the power-on sequence only when V_{DD} reached V_{ON} (Fig. 11). Short circuits on the regulated supply voltage can be detected.

Voltage Thresholds on V_{IN}

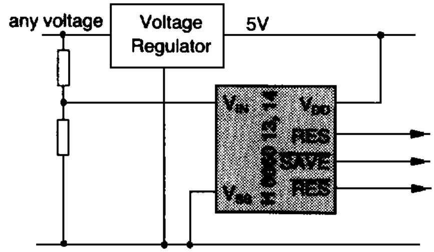
The H 6060 is available with 3 different sets of thresholds:

Version 11, 12: have an internal voltage divider for direct monitoring of the unregulated voltage without external components.



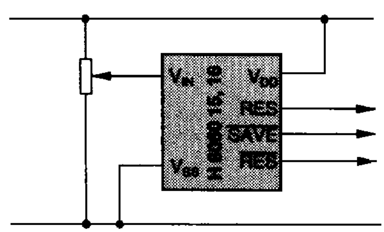
Note: internal threshold levels: 9/8/7V at V_{DD} = 5V (thresholds relative to V_{DD}, see table 4 and fig. 4) R_{VIN} = ~100kΩ Fig. 8

Version 13, 14: monitor the unregulated voltage and are ideal for programming of the V_{IN} voltage thresholds. Fixed resistor values can be used for programming.



Note: internal threshold levels: 2.25/2.00/1.75V at V_{DD} = 5V (thresholds relative to V_{DD}, see table 4 and fig. 4) R_{VIN} = ~100MΩ Fig. 9

Version 15, 16: monitor the regulated voltage. They are suited to applications where the unregulated voltage is not available. (The tolerance is ± 10%, see table 4. For tighter tolerances, trimming can be used, see fig. 10).



Note: internal threshold levels: 2.00/1.95/1.90V (thresholds relative to internal bandgap reference) R_{VIN} = ~100MΩ Fig. 10

6

Monitoring of the unregulated voltage requires versions 11, 12, 13 and 14. These versions are based on the principle that V_{DD} rises with V_{IN} on power-up and V_{DD} holds up for a certain time after V_{IN} starts dropping on power-down. The versions 11 and 12 have a 100kΩ nominal resistance from V_{IN} to V_{SS} (internal voltage divider). The versions 13, 14, 15 and 16 have high impedance V_{IN} inputs (see fig. 7 and table 4) for external threshold voltage programming by a voltage divider on pin V_{IN}. The levels obtained are proportional to the internal levels V_{SH}, V_{SL} and V_{RL} on the chip itself (see Electrical Specifications).

Timer Programming

With pin RC unconnected, the on-chip RC oscillator together with its divider chain give a timeout T_{TO} of typically 100ms. To program different T_{TO}, an approximation for calculating component values is given by the formula:

$$T_{TO} = \left[0.75 + \frac{(32 + C_1)\cdot 2}{5.5 + \frac{V_{DD} - 1}{R_1}} \right] \cdot 8.192$$

$R_{1\,min.} = 10\,k\Omega$, $C_{1\,max.} = 1\,\mu F$

If R_1 is in MΩ and C_1 in pF, T_{TO} will be in ms.

A resistor decreases and a capacitor increases the interval to timeout. Excellent temperature stability of T_{TO} can be achieved by using external components. A precise square wave of period 2 x T_{TO} is generated at the outputs $\overline{RES}$ and RES when $\overline{TCL}$ is tied to either V_{DD} or V_{SS}. The oscillator and watchdog timer start running when both V_{IN} is greater than V_{SH} (see fig. 6) and V_{DD} is greater than V_{ON} (see fig. 3). They will remain running while both V_{IN} is greater than V_{RL} and V_{DD} is greater than V_{OFF} (see fig. 3).

Timer Clearing and $\overline{RES}$/RES Action

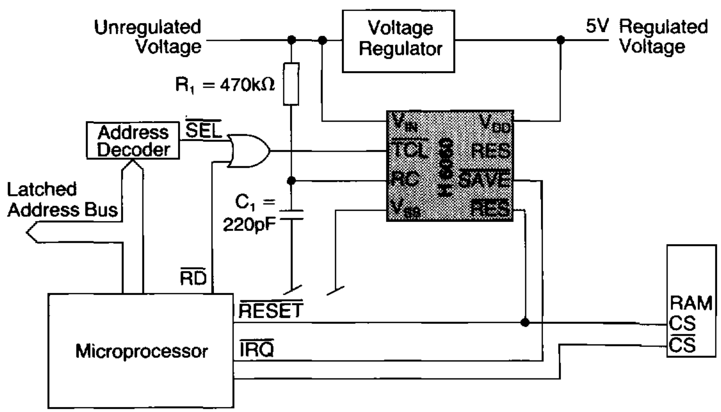
A negative edge or a negative pulse at the $\overline{TCL}$ input for longer than 150ns will reset the timer and set $\overline{RES}$ and RES inactive. If a further $\overline{TCL}$ signal edge or pulse is applied before T_{TO} timeout, $\overline{RES}$ and RES will remain inactive and the timer will again be reset to zero (see fig. 5). If no $\overline{TCL}$ signal is applied before the T_{TO} timeout, $\overline{RES}$ and RES will start to generate square waves of period 2 x T_{TO} starting with the inactive state. The watchdog will remain in this state until the next $\overline{TCL}$ signal appears, or until a fresh power-up sequence.

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in fig. 6. One timeout period after V_{IN} reaches V_{SH}, during power-up, $\overline{RES}$ and RES go inactive. A $\overline{TCL}$ pulse will have no effect until this power-on reset delay is completed. After completing the power-up sequence the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ and RES go active after one timeout period T_{TO}. After each subsequent timeout period, without a timer clear pulse at $\overline{TCL}$, $\overline{RES}$ and RES change polarity providing square wave signals. A $\overline{TCL}$ pulse clears the watchdog timer and causes $\overline{RES}$ and RES to go inactive. A voltage drop below the V_{RL} level overrides the timer and immediately forces $\overline{RES}$, RES and $\overline{SAVE}$ active. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence is completed.

Typical Applications

Microprocessor Watchdog with Power-On Reset and Voltage Monitor



$T_{TO} = \sim 300$ ms

Fig. 11

Voltage Monitor with Spike Suppression

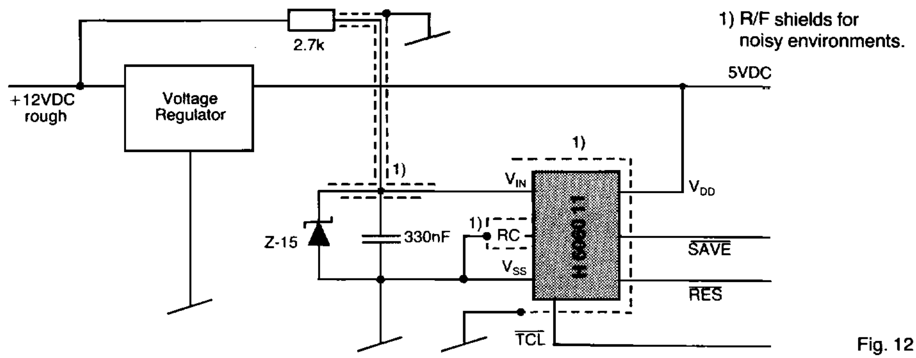
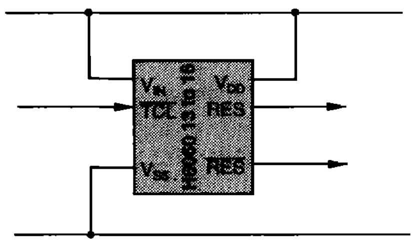


Fig. 12

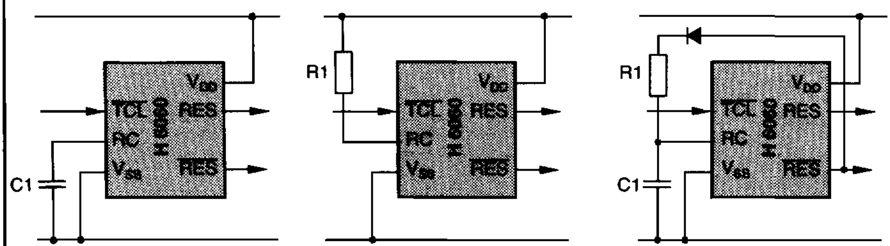
Watchdog and Power-On Reset



If precise thresholds are not required then V_{IN} monitoring on versions 13 to 16 can be disabled by tying V_{IN} to V_{DD}. The V_{DD} monitoring is still active and power-up reset occurs at V_{ON} and power-down reset at V_{OFF} threshold.

Fig. 13

External Programming of RC Oscillator



C1 increases T_{TO}

R1 shortens T_{TO}

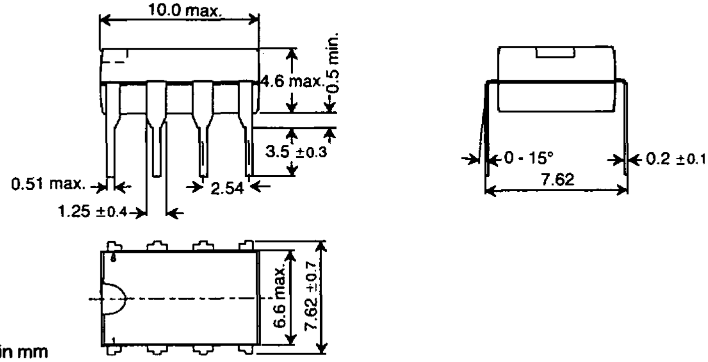
This circuit provides independent programming of both timeout period and power-on reset delay.

Note: if external components R1 and C1 are used, a tighter timeout period tolerance can be achieved.

Fig. 14

Package and Ordering Information

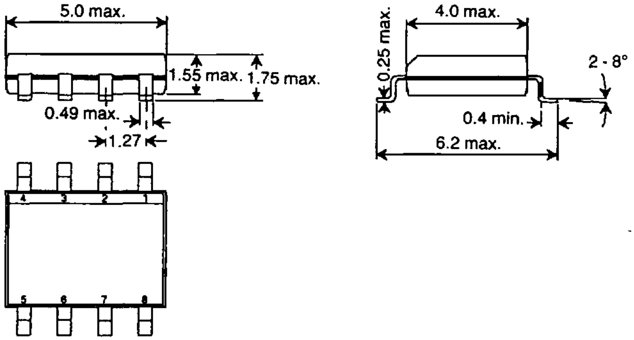
Dimensions of DIP8 Package



Dimensions in mm

Fig. 15

Dimensions of SO8 Package



Dimensions in mm

Fig. 16

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	**Package**
H 6060 nn 8P	DIP8
H 6060 nn 8S	SO8

Extended temperature range (−40 to +125°C)

Type[1]	**Package**
H 6060 nn X 8P	DIP8*
H 6060 nn X 8S	SO8*

[1] nn stands for the versions 11*, 12*, 13*, 14, 15, 16

* Non-stock items

Chip form on request

The H 6060 standard versions are as shown in the electrical specifications:

	open drain outputs	push-pull outputs
H 6060	11	12
H 6060	13	14
H 6060	15	16

When ordering please specify complete part number.