Bt630

Monolithic CMOS High Bandwidth Programmable Range 20–400 Nanoseconds 5-Tap Delay Line

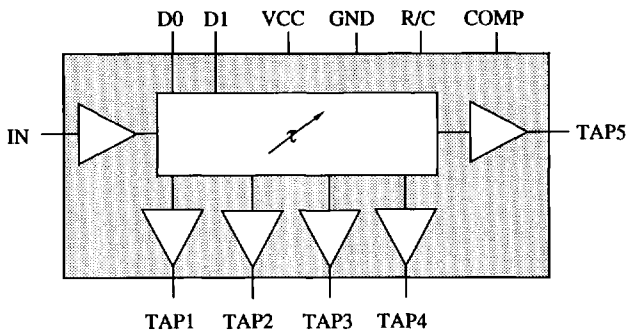
Distinguishing Features

- Up to 50 MHz Bandwidth
- 15 ns Minimum Input Pulse Width
- Monolithic CMOS Construction
- Programmable Full-scale Delays 20–400 ns
- 50 mW Typical Power
- Five Buffered Taps at 20, 40, 60, 80, and 100% of Full-scale Delay
- Output Delay Accuracies to ±10% or ±3 ns, whichever is greater

Applications

- CPU Clock Timing
- Memory Timing
- Pulse Generator Circuits
- Bus Interface Timing

Functional Block Diagram



Product Description

The Bt630 is a buffered tapped delay line with input and output compatibility to TTL logic families.

The Bt630 is useful for generating multiple edges from a clock signal at its input. The five delay taps are at the 20%, 40%, 60%, 80%, and 100% points of the programmed full-scale delay.

Unlike fixed tapped delay lines, the Bt630 is adjustable in full-scale delay from 20–400 ns. This flexibility allows the user a range of delays that would be impossible without a large inventory of different, fixed span, tapped delay lines.

Selection of the full-scale delay is performed by a coarse and fine adjustment. The coarse adjustment is set by two digital input bits. The four selectable ranges are 20–50, 40–100, 80–200, and 160–400 ns.

The fine adjustment is set by an external resistor and capacitor. Fixed value components may be used, or variable resistors can be employed to adjust delays individually.

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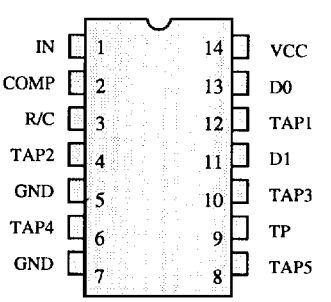
Pin Description

Pin Name	Description
D0, D1	The digital control inputs which select the operating full-scale delay range. D0 is the LSB. The truth table for range value is:
R/C	The node where a resistor and capacitor connect to set up the precise full-scale delay for a given range selected by pins D1 and D0.
COMP	A compensation pin where a 0.1 µF filter capacitor to ground is connected. The nominal voltage at this point is 3.3 V.
IN	The input to the delay line. TTL-compatible input thresholds.
TAP5	The full-scale delay output. TTL compatible.
TAP4	The 80% of full-scale delay output. TTL compatible.
TAP3	The 60% of full-scale delay output. TTL compatible.
TAP2	The 40% of full-scale delay output. TTL compatible.
TAP1	The 20% of full-scale delay output. TTL compatible.
VCC	Power input pin, 5 V nominal. A 0.1 µF ceramic capacitor to ground is recommended for bypassing.
GND	Power ground pins.
TP	This is a manufacturing test pin. No connection should be made to this pin by the user.
	(Unused outputs should be left open.)

D1	D0	RANGE
0	0	20–50 ns
0	1	40–100 ns
1	0	80–200 ns
1	1	160–400 ns

Bt630KP



Application Information

Power Supply

COMP and VCC pins should be separately decoupled to GND with 0.1 µF ceramic capacitors. The bypass capacitors should be as close as possible to the device pins.

Upon power up of the Bt630, approximately 100 milliseconds should be allowed for the device to settle on its programmed delay. After this time, the device will meet specifications of performance.

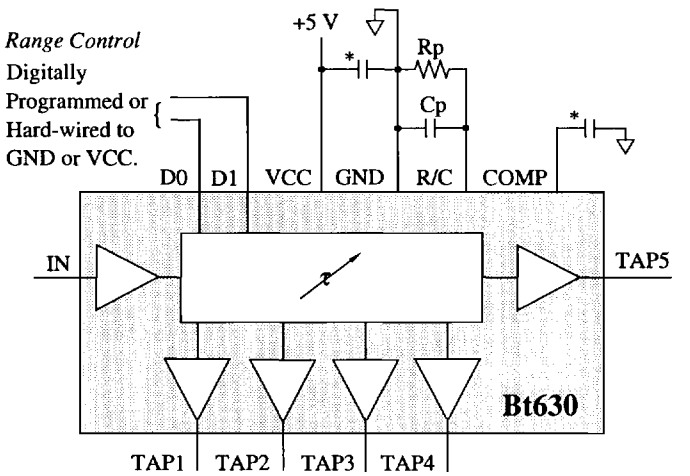
Applications

The full-scale delay of the Bt630 is set with an external resistor/capacitor combination and two digital bits of range control. The digital ranging bits offer the selection of the range in coarse increments. The resistor/capacitor combination allows the user to fine tune the selected delay within the range. Cp and Rp are the programming capacitor and resistor combination (see Figure 1). Once the range has been selected via the digital control bits and given a fixed value capacitor, the delay can be adjusted over a 2:1 range using Rp.

The ranges available using the digital control bits are indicated in Table 1. The base period, Tbase, is controlled by the digital bits. The overall delay follows the formula:

$$Tdelay = [Rp * (Cp + 1.8)]/k$$

where k varies, based on Tbase.



* = 0.1 microfarad ceramic capacitor, 10%.

Figure 1. Bt630 Typical Application.

Range	k	Tbase	Range of Delays
0	32	20 ns	20–50 ns
1	16	40 ns	40–100 ns
2	8	80 ns	80–200 ns
3	4	160 ns	160–400 ns

Table 1. Bt630 Delay Ranges.

Application Information *(continued)*

The relationship in Table 1 allow for common units to be used in the equation,

$$\text{Tdelay (ns)} = [\text{Rp(k}\Omega) * (\text{Cp(pF)} + 1.8\text{ pF})] / \text{k}$$

where 1.8 pF is attributed to package capacitance. Recommendations are to choose Cp and Rp so that Cp is a 1% mica capacitor (this is a low-cost, easily-obtained value with temperature coefficients of ±100 ppm/°C) and Rp is a metal-film type resistor (easily obtained in 100 ppm/°C, e.g., RN55D, down to ±25 ppm/°C, e.g., RN55E, and temperature coefficients with a tolerance of 1% to 0.1%).

Jitter

Preliminary characterization data taken to categorize jitter shows that the amount of jitter is directly dependent upon the combination of the programming resistance (Rp) and capacitance (Cp) used to set the full-scale delay. To a lesser extent, jitter is also dependent upon the range and tap selected to obtain the desired delay of the device.

It can be reduced substantially by using the lowest combination of Rp and Cp possible in fine tuning the desired full-scale delay of the device. Values of Rp and Cp should be chosen as close as possible to the specified minimum product of

$$\text{Rp}(\Omega) * \text{Cp(F)} \geq 400 * 10^{-9}$$

This will ensure that the delay of the device is in accordance with that specified by the Tdelay formula and will substantially reduce the amount of jitter. It is imperative to use the lowest possible RpCp combination if a reduction in the amount of jitter is desired.

The apparent jitter of the device has also been found to increase with both range (0–3) and tap (1–5). Therefore, to further minimize the jitter of the device, the lowest range along with the lowest of the 5 taps available should be used with the minimum combination of RpCp. The relationship between the combination of RpCp and range for apparent jitter of the device is shown in Figure 2 with Cp = 100 pF and Rp from 6–16 kΩ for tap 5.

Even though the relationship as shown in Figure 2 is not linear, the following formulas have been derived to assist in determining the approximate jitter (peak-to-peak) present for the chosen RpCp combination within each range of operation (shown in Figure 3).

Range	Typical Jitter (ns, peak-to-peak) where Rp (in kΩ), Cp (in pF)
0, 1	(0.0032 * Rp * Cp) – 1.8
2	(0.0036 * Rp * Cp) – 1.9
3	(0.0045 * Rp * Cp) – 2.3

In summary, to reduce the amount of jitter in the delay, the combination of RpCp should be as close as possible to the specified minimum, and the lowest range and the lowest tap should be used.

Application Information *(continued)*

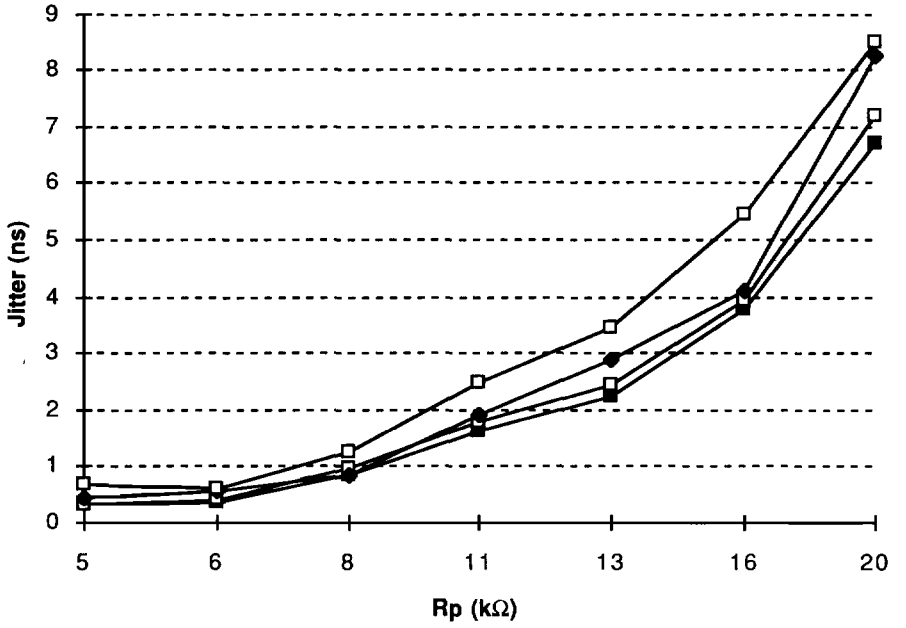


Figure 2. Typical Jitter versus Rp (at 25°C with Cp = 100 pF).

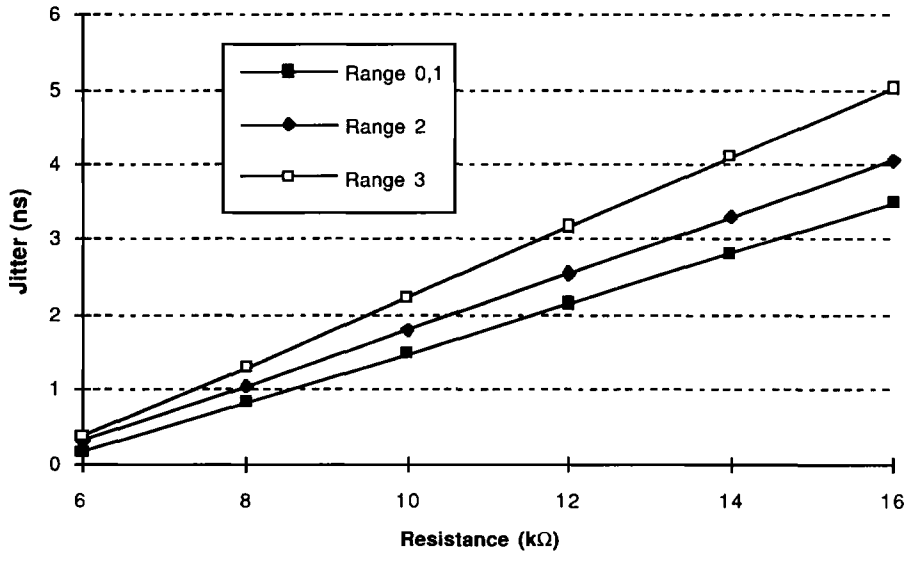


Figure 3. Typical Jitter versus Rp by Range Using Formulas (at 25°C with Cp = 100 pF).

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Recommended Operation Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive	VCC	4.75	5.0	5.25	V
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (relative to GND)				7.0	V
Voltage on any Digitial Pin		GND–0.5		VCC + 0.5	V
Output Current (any one output)				–50	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature 5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH	–10		10	µA
Input Low Current (Vin = 0.4 V)	IIL	–10		10	µA
Input Capacitance (Note 1) (f = 1 MHz, Vin = 2.4 V)	CIN			10	pF
Digital Outputs					
Output High Voltage (IOH = –0.4 mA)	VOH	2.4	3.3		V
Output Low Voltage (IOL = 16 mA)	VOL			0.4	V
VCC Power Supply Rejection (Measured at Tap5, Range = 0) (Notes 1 and 2)	PSRR		0.2		%/V
VCC Supply Current					
Static—No Input Signal	ICC (static)		10	25	mA
25 MHz Input Signal	ICC(dynamic)		30	45	mA
Output Drive /Tap				10	TTL Loads
Output Drive/ all Taps (Note 3)				20	TTL Loads
Programming Capacitance (Notes 1 and 4)	Cp			300	pF
Programming Resistance (Notes 1 and 4)	Rp	6		16	kΩ

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Cp = 100 pF, Rp = 8.0 kΩ and 16 kΩ at 25°C. All parameters specified at 0°C and 70°C are guaranteed by characterization and are not 100 percent production tested.

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Note 1: Not tested in production. Based on characterization data.
Note 2: PSRR as a percentage change in Tdelay versus supply voltage.
Note 3: More loads may be driven with degraded delay accuracy specification. See Figure 4, Output Delay versus Loading. One TTL load is defined as Vil = 0.4 V max at Iil = 1.6 mA and Vih = 2.4 V min at –40 µA.
Note 4: The product of Rp and Cp must be greater than 400×10^{-9}, $Rp(\Omega)^* Cp(F) \geq 400 \times 10^{-9}$, to ensure output delay according to the formula for Tdelay = [Rp * (Cp + 1.8)]/k.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Minimum Input Pulse Width					
at Minimum Delay					
Range 0, 1, 2	TPWH, TPWL	10			ns
Range 3	TPWH, TPWL	15			ns
at Maximum Delay					
Range 0	TPWH, TPWL	20			ns
Range 1	TPWH, TPWL	25			ns
Range 2	TPWH, TPWL	35			ns
Range 3	TPWH, TPWL	45			ns
Delay Accuracy (Note 1)	Tdelay	–10	or	+10	% of nominal
(Rising or Falling Signals)		–3		+3	ns
Delay Tempco (Note 2)					
Range 0			5	15	ps/°C
Range 1			10	20	ps/°C
Range 2			20	25	ps/°C
Range 3			40	50	ps/°C
Output Rise/Fall Time (Measured at 0.6 V and 2.4 V)	Tr, Tf		2		ns

AC characteristics test conditions (unless otherwise specified): "Recommended Operating Conditions" with all outputs loaded with 1 TTL load (plus 20 pF lumped capacitance). Input signal per timing diagram (Figure 5) with input Tr, Tf = 2 ns (20 percent to 80 percent).

Note 1: Tdelay is guaranteed at 25°C and nominal V_{CC} (5.0 V) only. Tdelay is specified for all taps from input to tap output with Cp = 100.0 pF and ideal Rp resistor value. Nominal delays are calculated using the formula Tdelay = [Rp * (Cp + 1.8)]/k. If ±10 percent of Tdelay nominal is < 3 ns, then ±3 ns is the delay accuracy. Tolerances on Cp and Rp add to the Tdelay accuracy specification.

Note 2: For optimum performance, choose low-temperature coefficient components for Rp and Cp.

AC Characteristics *(continued)*

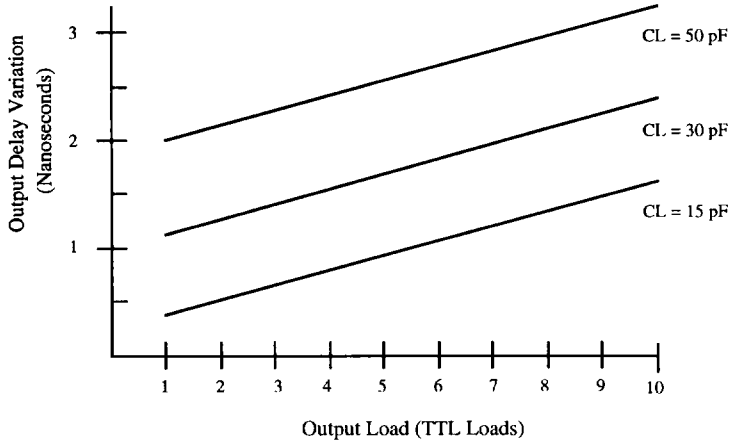

Figure 4. Output Delay versus Tap Loading.

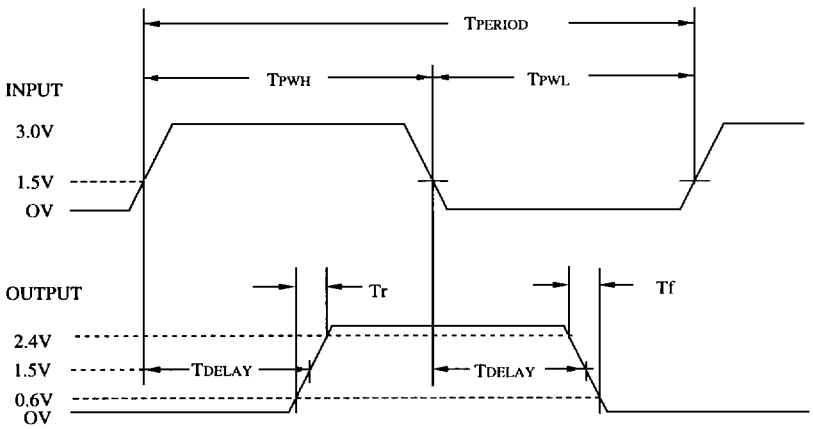

Figure 5. Timing Diagram.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt630KP	14-pin Plastic DIP	0°C to +70°C