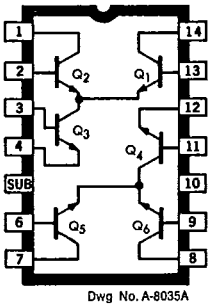
ULN-2054A TRANSISTOR ARRAY
(Dual Independent Differential Amplifiers)

THE ULN-2054A is a transistor array consisting of six silicon NPN transistors on a single monolithic chip. The transistors are internally interconnected to form two independent differential amplifiers.

The ULN-2054A is intended for a wide range of applications requiring extremely close electrical and thermal matching characteristics. Some applications are: cascade limiter circuits; balanced mixer circuits; balanced quadrature/synchronous detector circuits; balanced (push-pull) cascade/sense/IF amplifier circuits; or in almost any multifunction system requiring RF/Mixer/Oscillator, converter/IF functions.

Available in a 14-lead dual in-line plastic package the ULN-2054A is rated for operation over a −20°C to +85°C ambient temperature range.



Dwg No. A-8035A

Other features are:
- Input Offset Voltage—5 mV max.
- Input Offset Current—2 μA max.
- Voltage gain (single-stage double-ended output) −32 dB typ.
- Common-Mode Rejection Ratio (each amplifier) −100 dB typ.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
(unless otherwise noted)

Power Dissipation T_A to +55°C:	
Each Transistor	300 mW
Total Package	750 mW
Derating Factor, Total Package, $T_A \geq 55°C$	6.67 mW/°C
Collector-Base Voltage, $V_{(BR)CBO}$	20 V
Collector-Substrate Voltage, $V_{(BR)CIO}$ (See note 2)	20 V
Collector-Emitter Voltage, $V_{(BR)CEO}$	15 V
Emitter-Base Voltage, $V_{(BR)EBO}$	5 V
Collector Current, I_C	50 mA
Base Current I_B	5 mA
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−65°C to +150°C

Notes:
1. The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistor, do not attempt to measure these characteristics above the maximum ratings.
2. Pin 5 is connected to the substrate. This terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ULN-2054A TRANSISTOR ARRAY

STATIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A, I_E = 0$	20	60		V
Collector-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\ \mu A, I_{C1} = 0$	20	60		V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\ mA, I_B = 0$	15	24		V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A, I_C = 0$	5	7		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10\ V, I_E = 0$			100	nA
Base-Emitter Voltage	V_{BE}	$I_C = 50\ \mu A, V_{CB} = 3\ V$		0.630	0.700	V
		$I_C = 1\ mA, V_{CB} = 3\ V$		0.715	0.800	V
		$I_C = 3\ mA, V_{CB} = 3\ V$		0.750	0.850	V
		$I_C = 10\ mA, V_{CB} = 3\ V$		0.800	0.900	V
Temperature Coefficient of Base-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$I_C = 1\ mA, V_{CB} = 3\ V$		−1.9		mV/°C
Input Offset Voltage	V_{IO}	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA, V_{CB} = 3\ V$		0.45	5	mV
Input Offset Current	O_{IO}	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA, V_{CB} = 3\ V$		0.3	2	μA
Input Bias Current	I_I	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA, V_{CB} = 3\ V$		10	24	μA
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$	$I_{E(Q3)} = 2\ mA, V_{CB} = 3\ V$		0.98-1.02		—
	$\frac{I_{C(Q5)}}{I_{C(Q6)}}$	$I_{E(Q4)} = 2\ mA, V_{CB} = 3\ V$		0.98-1.02		—
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\Delta V_{IO}}{\Delta T}$	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA, V_{CB} = 3\ V$		1.1		μV/°C

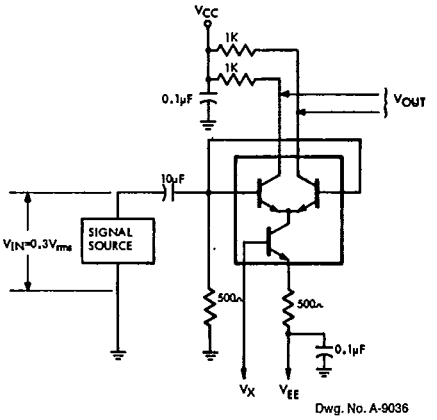
DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Common-Mode Rejection Ratio For Each Amplifier	CMR	$V_{CC} = 12\ V, V_{EE} = -6\ V, V_X = 3.3\ V,$ $f = 1\ kHz$ (See figure 1)		100		dB
AGC Range, One Stage	AGC	$V_{CC} = 12\ V, V_{EE} = -6\ V, V_X = 3.3\ V,$ $f = 1\ kHz$ (See figure 2)		75		dB
Voltage Gain, Single Stage Double Ended Output	A_v	$V_{CC} = 12\ V, V_{EE} = -6\ V, V_X = 3.3\ V,$ $f = 1\ kHz$ (See figure 2)		32		dB
AGC Range, Two Stage	AGC	$V_{CC} = 12\ V, V_{EE} = -6\ V, V_X = 3.3\ V,$ $f = 1\ kHz$ (See figure 3)		105		dB
Voltage Gain, Two Stage Double-Ended Output	A_v	$V_{CC} = 12\ V, V_{EE} = -6\ V, V_X = 3.3\ V,$ $f = 1\ kHz$ (See figure 3)		60		dB
Small-Signal Common-Emitter Forward Current Transfer Ratio	h_{fe}	$I_C = 1\ mA, V_{CE} = 3\ V, f = 1\ kHz$		110		—
Small-Signal Common-Emitter Short-Circuit Input Impedance	h_{ie}	$I_C = 1\ mA, V_{CE} = 3\ V, f = 1\ kHz$		3.5		kΩ
Small-Signal Common-Emitter Open-Circuit Output Impedance	h_{oe}	$I_C = 1\ mA, V_{CE} = 3\ V, f = 1\ kHz$		15.6		μmho
Small-Signal Common-Emitter Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}	$I_C = 1\ mA, V_{CE} = 3\ V, f = 1\ kHz$		1.8×10^{-4}		—
Gain-Bandwidth Product (for Single Transistor)	f_T	$I_C = 3\ mA, V_{CE} = 3\ V$		550		MHz
Noise Figure (for Single Transistor)	N.F.	$V_{CE} = 3\ V, f = 1\ kHz, I_C = 100\ \mu A,$ $R_g = 1\ k\Omega, BW = 15.7\ kHz$		3.25		dB
Noise Figure (for each Amplifier)	N.F.	$f = 100\ MHz$		8		dB

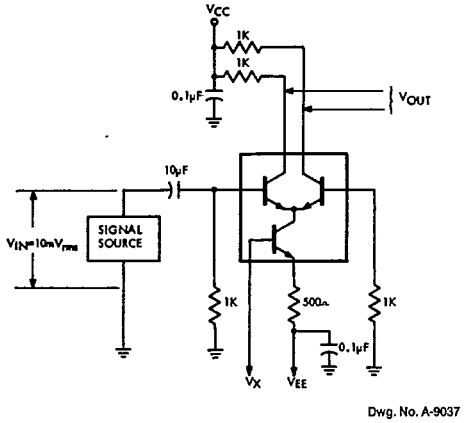
NOTE: Characteristics apply for each transistor unless otherwise specified.

ULN-2054A TRANSISTOR ARRAY

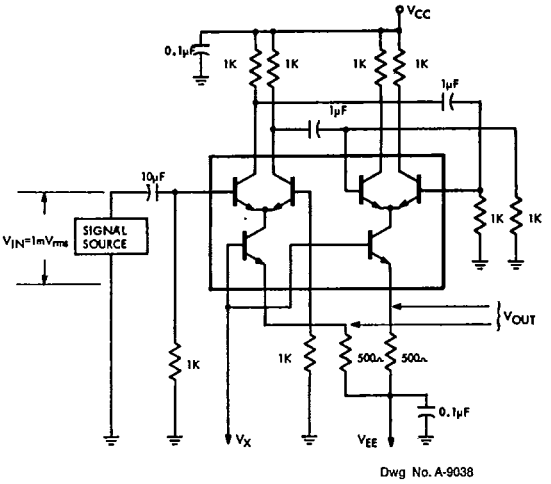
AMPLIFIER TEST CIRCUITS



COMMON MODE REJECTION RATIO
Figure 1



SINGLE-STAGE VOLTAGE GAIN
Figure 2



TWO-STAGE VOLTAGE GAIN
Figure 3

Additional information on transistor arrays ULN-2031A through ULN-2086A, ULS-2045H and ULS-2083H, is available from:

Sprague Electric Company
Integrated Circuits Division
115 Northeast Cutoff
Worcester, Massachusetts 01606
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